Design and measurements of SEU tolerant latches

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Abstract

Latches based on the Dual Interlocked storage Cell or DICE are very tolerant to Single Event Upsets (SEU). However, for highly scaled processes where the sizes continue to decrease, the data in this latch can be corrupted by an SEU due to charge sharing between adjacent nodes. Some layout considerations are used to improve the tolerance of the DICE latches to SEU and especially the influence of sensitive nodes separation is tested for DICE latches designed with a 130 nm process.

I. INTRODUCTION

The requirement for total dose tolerance for the ATLAS pixel detector has been estimated to 50 Mrad. Because of this high level of irradiation, the performance of the innermost layer of ATLAS pixel detector, the so-called b-layer, will start degrading after 2-3 years of LHC working. So, it is proposed to upgrade the b-layer detector. For this purpose, improvement in the electronic design of the pixel front end is under study and development using the 130 nm process [4].

At the time of the b-layer replacement, the level of radiation will be 3 times higher than at the start of the LHC. The total dose is estimated to reach 150 to 200 MRad and peak fluencies are close to 1×10^8 particles/cm²/sec.

In principle, the commercial 130 nm process used to design the front end chip is less sensitive than older process generations to the effect of the total ionizing dose and irradiation tests made on individual devices are very promising.

However, we have to consider carefully the SEU for this highly scaled process. In fact, the device dimensions are small and the capacitance of storage nodes becomes lower. The supply voltage needed is low (1.0 V to 1.4 V for the 130 nm process). The critical charge needed to provoke an upset becomes lower than in older processes and digital designs become less tolerant against SEU.

Traditional flip flops are not suitable to be used in the b-layer environment. D flip flops based on the dual interlocked cell (DICE) latches have redundant storage nodes and restore the cell original state when an SEU error is introduced in a single node [5]. The probability that multiple nodes are affected by an upset is low, making the DICE latch less sensitive to SEU. However, as the device size shrinks, the space between critical nodes is reduced. The redundancy becomes less efficient because of the charge sharing between sensitive nodes of the DICE latch. For this reason, some hardened by design (HBD) approaches are used to reduce the effect of charge sharing.

A 130 nm test chip has been designed in order to study the effect of some layout techniques on the tolerance to SEU. Layout considerations are based on spatial separation of critical nodes, isolation techniques like isolated wells and guard rings and cell interleaving. Some prototype layout structures have been investigated in order to develop some rules to follow in the new design of the front end IC developed for the b-layer replacement.

II. DICE LATCH STRUCTURE UNDER TEST

A. DICE Structure

The DICE latch structure is shown in Figure 1. It is based on the conventional cross coupled inverter latch structure. The 4 nodes X1 to X4 store data as 2 pairs of complementary values.

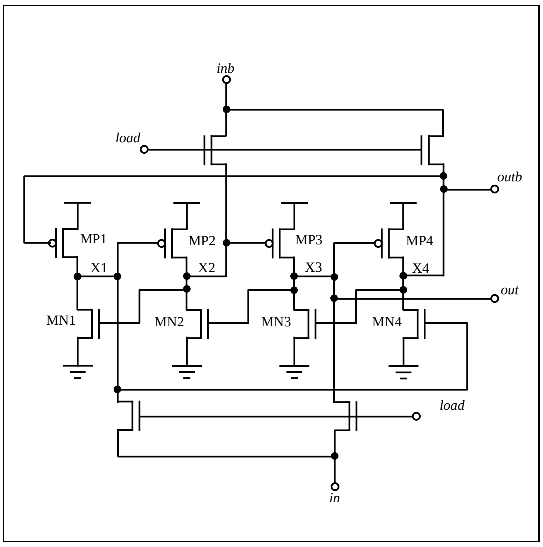

Figure 1: DICE latch structure

For example, when the stored data are 0 then X1-X2-X3-X4 = 0101 and particularly X1 is low and X4 is high. If we assume a positive upset pulse on the node X1, the transistor

MP2 is blocked avoiding the propagation of this perturbation to the node X2. At the same time the transistor MN4 will propagate a negative pulse to the node X4 blocking MN3 and avoiding X3 level corruption. The perturbation is then removed after the upset transient since the nodes X2 and X3 have conserved the true information.

However, if 2 sensitive nodes of the cell storing the same logic state (X1-X3) or (X2-X4) change the state level due to the effect of a single particle impact, the immunity is lost and the DICE latch can be upset.

In this work, we will show that the SEU probability is reduced by layout considerations and essentially if the transistors drain areas corresponding to the sensitive nodes are separated in the layout.

B. Description of the compared layouts

In order to evaluate the layout importance for the SEU tolerance, three different layouts were implemented for the same latch as shown in Figure 2. The cells are identical in schematic and use the same devices dimensions. They are based on the conventional DICE latch structure.

The main difference between the three layouts is the separation length between the drain areas of the sensitive nodes. Layout parameters are summarized in Table 1.

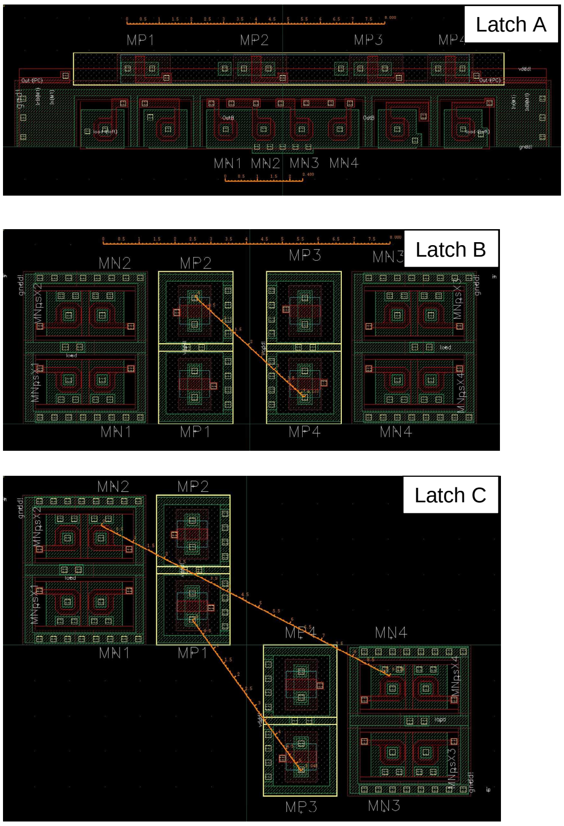

Figure 2: Implemented layouts for the DICE latch

In the latch A, considered as the baseline design, all pmos devices are located in the same nWell and don’t have guard contact separation. It is mentioned that contacted guard rings reduce the effect of parasitic bipolar transistor [6]. So, isolated nWell for sensitive pmos devices are used in the layout for latch B and latch C. Contacted guard rings are also used to isolate sensitive nmos devices.

The layout of latch C uses an interleaved layout, in order to increase the separation of sensitive nodes. This can be easily implemented in triple redundancy structure for example.

Table 1: Parameters of implemented layouts

Layout type	Size (µm)	Area (µm²)	nmos separation (µm)	pmos separation (µm)
Latch A	16×3	48	2.4	8
Latch B	12×4	48	8	4
Latch C	12×4	48	9	5.4

III. EXPERIMENTAL TEST SETUP

A. Test structure

The test structure is designed around shift registers and triple redundancy latches as illustrated in Figure 3. The shift register uses conventional flip flops and allows to load and read-back data into and from the cells under test.

Each tested cell is composed of 3 latches connected in triple redundancy structure. A circuit block based on combinatory logic generates two flags per block of register cells: the error flag and the parity flag.

The error flag signal switches from 0 to 1 when the content of one latch of the block is changed. This flag indicates a latch upset.

The parity flag at the output of the block is determined as an XOR of all parity bits coming from the cells. A majority voting circuit is implemented in each cell in order to generate the cell parity bit which is changing the state when at least 2 among the 3 latches of the same cell change the state.

The combination of the parity flag and the error flag allows to indicate if an error has occurred in the triple redundancy cell.

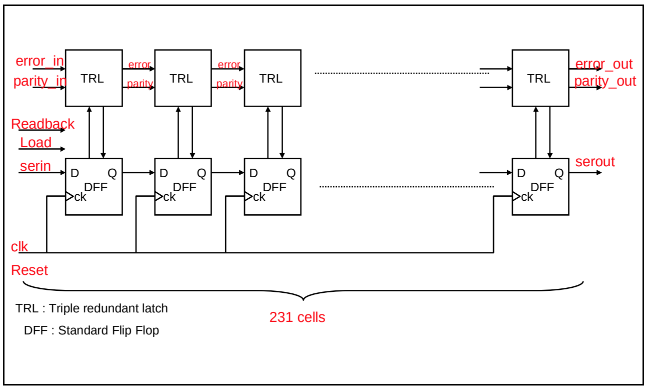

Figure 3: Block organisation

The serial output from the shift register corresponds to the effective data memorized in the triple redundancy structure. The comparison between input and output shift register data determines the upset rate of the triple redundancy cell.

B. *Test chip*

The test chip shown in Figure 4 is designed exclusively for SEU test and characterisation. It is manufactured with commercial 130 nm process. It contains different blocks of shift registers connected in parallel and using the same clock and the same control signals as reset, load and read-back. The same mask of data is applied to all blocks of memories. Each register block generates its own error flag, parity flag and output data.

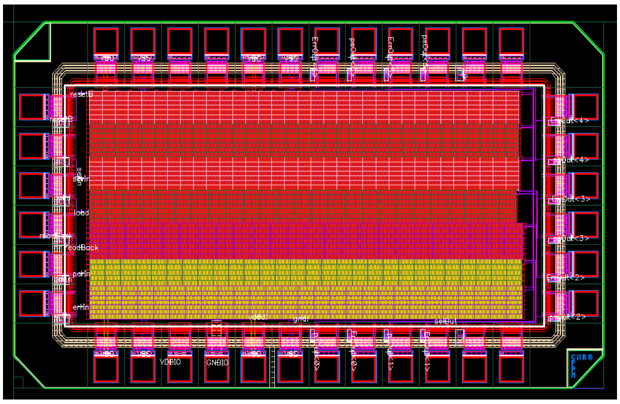

Figure 4: SEU test chip

C. *Experimental setup*

Figure 5 illustrates the test set up used for SEU evaluation. The chip under test is packaged on a PLCC44 package with 44 pins. It is controlled and read out by a DAQ system based on a PCMCIA card from National Instruments and controlled by a laptop PC. The PCMCIA card generates digital signals to control and read back the tested chip. The software to control the PCMCIA IO signals is written in C++ code using Lab-windows interface.

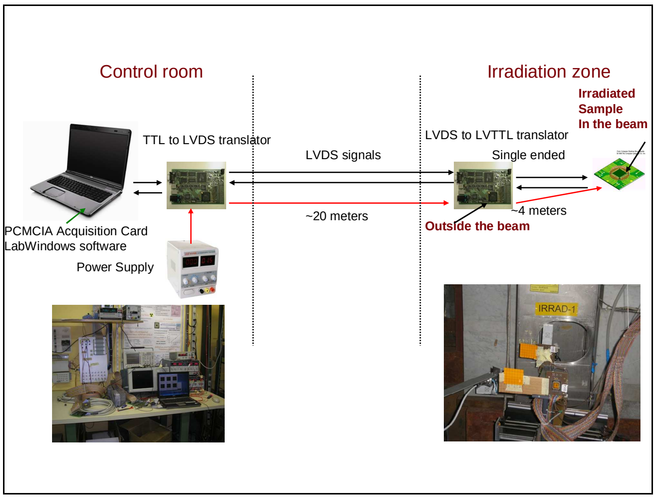

Figure 5: Experimental test setup

An interface board located in the computing area converts 5V TTL signals into LVDS signals. Those differential buffers drive a 20 meter twisted pair cable transmitting and receiving pattern and control signals in differential mode. An intermediate board located in the irradiated zone is connected with a 5 meters flat cable to the board under test. This board uses commercial devices and converts differential levels into single ended levels before arriving to the chip under test.

D. *Facility*

Irradiation tests were carried out using IRRAD3 beam line of the proton synchrotron (PS) facility at CERN. The test beam provides a beam of 24 GeV protons. The structure of the beam is defined by the operation cycle of the PS accelerator. The machine super-cycle period depends on the operation mode. It contains several spills of particles and it is distributed to the experiments sharing the beam. IRRAD3 beam line, used for the chip irradiations receives 1 to 4 spills per super-cycle.

The duration of each spill is 400 ms and the intensity can be tuned typically from $5\ 10^{10}$ to $1.5\ 10^{11}$ protons/spill. A secondary emission chamber (SEC) monitors the proton beam intensity.

However, the proton fluence is most accurately measured by irradiating thin foils of Aluminium. This method, measuring the gamma decay of ^{24}Na produced by the protons in Aluminium allows a fluence measurement with an accuracy of ~8 %.

During the irradiation test, the beam arrives to the front of the chip with an incident angle normal to the die area. For this test, total proton fluence provided to the chip is around $2\ 10^{15}/\text{cm}^2$.

IV. TEST RESULTS

A. *Irradiation procedure*

The experimental procedure consists of the following phases:

At the beginning of the machine cycle and outside the spill, a known data pattern is pushed in the shift registers and loaded in the memory cells.

The error out signal is continuously read out from the chip. If the “errout” bit of one block of latches passes from 0 to 1, all blocks of latches are read back outside the spill duration. After this, data pattern is rewritten in the shift registers and loaded in all latches blocks.

This operation is repeated every machine cycle. Since the shift registers flip flop is more sensitive to SEU than the latches under test, the write or read operations are carried out only before the spill duration.

B. *Upset rate determination*

The cross section is determined as the number of errors N_{errors} over the fluence Φ divided by the number of the latches implemented in the block .

$$\sigma = \frac{N_{errors}}{\Phi \bullet N_{latches}}$$

Figure 6 illustrates the cross section measurements for “1 to 0” upsets. It shows that the B and C latches are less sensitive to “1 to 0” upsets. Latch C is 5 times more tolerant than latch A. This is attributed to sensitive area separation and isolation techniques used for latch B and C layouts.

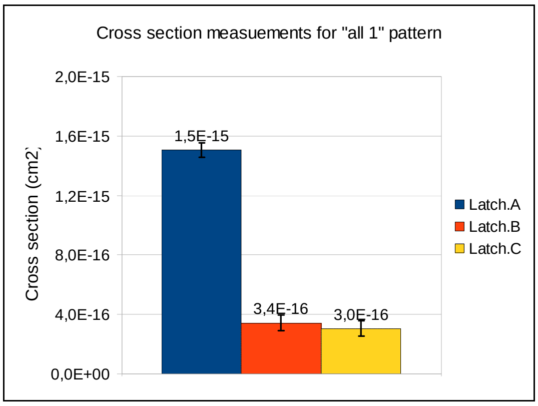

Figure 6: Cross section for “all 1” pattern

Figure 7 shows that the latch A is a little more tolerant to upsets from “0 to 1”. It shows also that the latch C which uses interleaved layout is less sensitive than the latch B because sensitive areas are more separated.

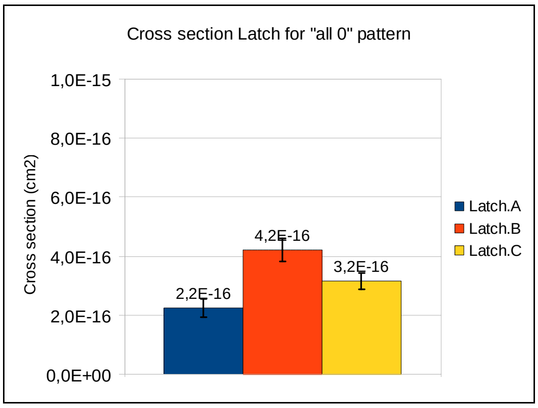

Figure 7: Cross section for “all 0” pattern

Figure 8 gives the cross section measurements with the “0101..01” pattern. Test results are obtained from a different device than the device used in previous measurements of cross sections. It shows that latches B and C are more tolerant to SEU when the stored pattern contains the same number of 0 and 1.

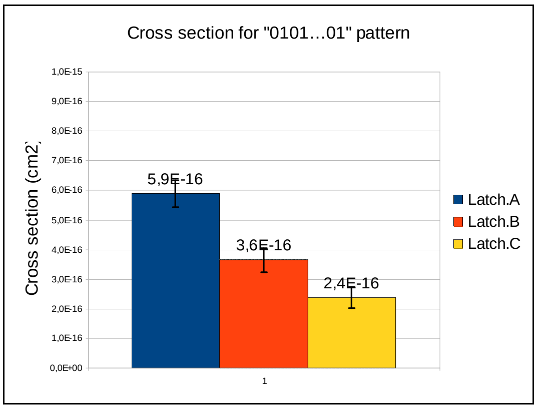

Figure 8: Cross section for “0101..01” pattern

V. CONCLUSION

It is well known that the DICE latch with redundant storage nodes makes the latch more tolerant to single event upset than a standard latch. However, the tolerance to SEU is affected by the charge sharing between sensitive nodes for DICE latches designed with highly scaled processes.

We developed in this work some layout considerations in order to improve the tolerance to SEU in the high scaled process. The influence of spatial separation of node pairs in DICE latch was measured. By reorganizing the layout of the studied latch, we obtained an improvement of a factor 3 in the SEU tolerance showing that the layout has a great importance in the charge sharing and so in the tolerance to SEU.

Some advanced simulations tools could be used to study the influence of other layout aspects like the effect of guard rings and nWell separation.

In the future, this work will be continued in order to measure the effect of the triple redundancy and the test set up will be improved in order to evaluate the sensitivity to SEU at 40 MHz.

VI. ACKNOWLEDGEMENTS

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VII. REFERENCES

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