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Design and measurements of SEU tolerant latches.

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The single event upset (SEU) tolerance of various latch designs in 0.13um CMOS technology has been studied by both measurement and simulation. The aim of this work is to optimize the design for critical registers on the next generation pixel readout chip for ATLAS upgrades (denominated FE-I4). Results form irradiations with 24 GeV protons will be presented and compared to previous values obtained with heavy ions. Layout effects will be discussed and quantified along with other design considerations.

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