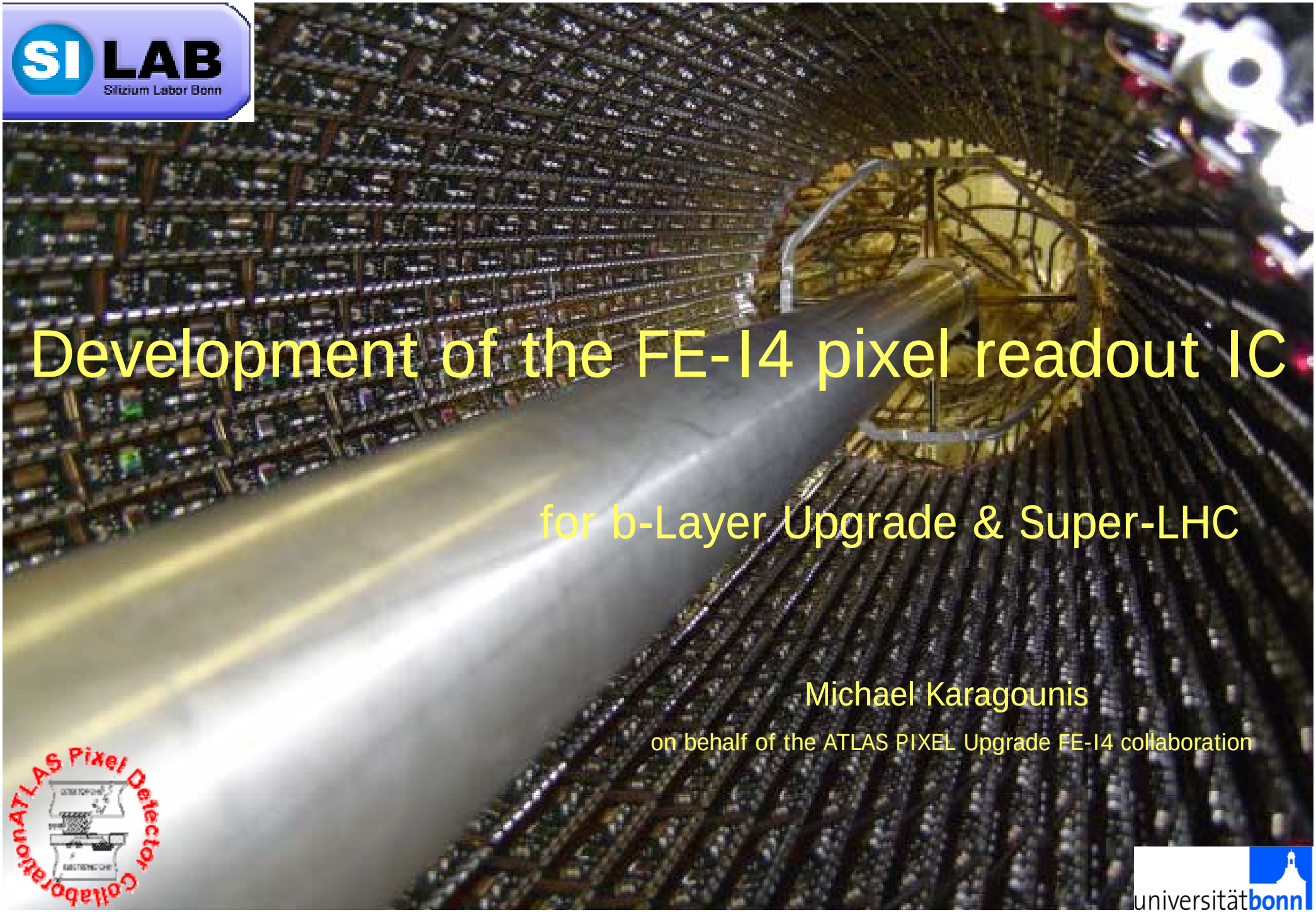


# Development of the FE-I4 pixel readout IC

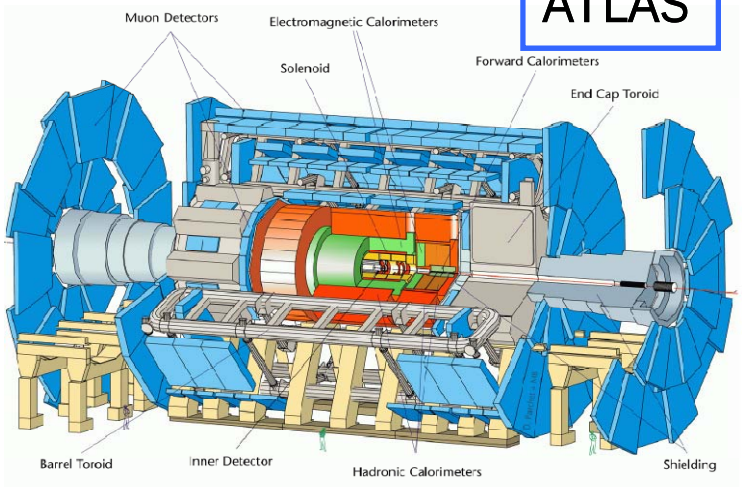
## for b-Layer Upgrade & Super-LHC

Michael Karagounis

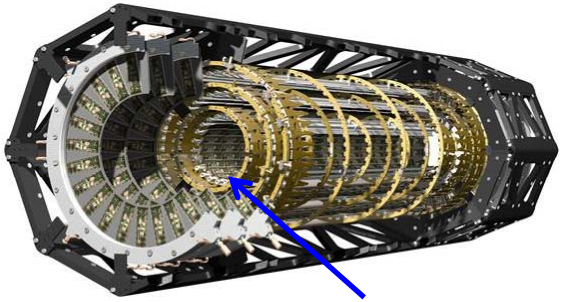
on behalf of the ATLAS PIXEL Upgrade FE-I4 collaboration

# Upgrade of the Current ATLAS Pixel Detector

ATLAS




pixel detector



b-Layer (innermost)

hybrid pixel module


**machine upgrade & consequences for the pixel detector**

~2013: b-Layer upgrade
→ expected sensor performance degradation caused by radiation
→ possible x2-3 luminosity increase at ~2013 (new triplets & injection chain)
b-layer insert at smaller radius 3.7cm

~2017: super-LHC upgrade
→ ~ x10 luminosity increase

FE-I4 targets the b-Layer upgrade in ~2013 & the outer layers at SLHC

# Motivation for FE-I4 Development

**Why a redesign** ?

- **smaller b-Layer radius & potential increased luminosity → higher hit rate**

→ **FE-I3** column-drain architecture **not able to cope** with x3 increased hit rate.

→ Smaller pixel size 50x400um → 50x250um (reduce pixel cross section)

→ New digital architecture for increased data volume

- **Material reduction & improve of active area**

→ bigger chip size 7.6x8mm → ~20.0x18.8mm

→ reduce size of peripheral chip area

→ increase cost efficiency

- **Power consumption**

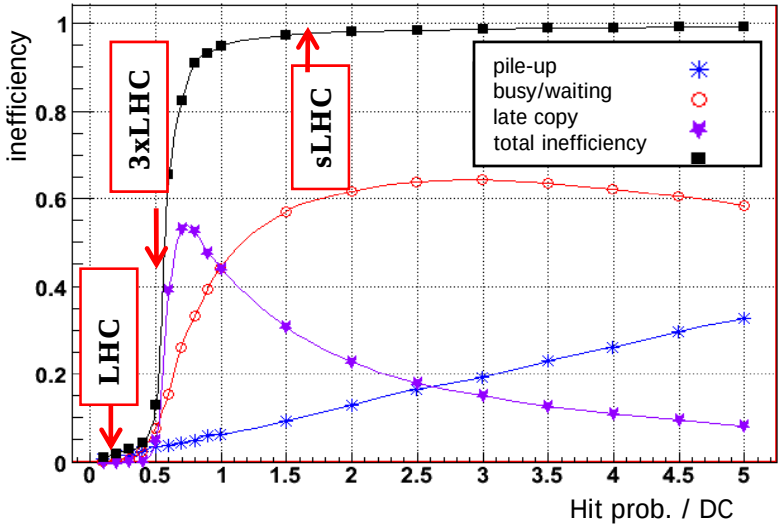
→ analog design for reduced currents

→ decrease of digital activity by sharing digital circuits with several pixels

→ Reducing cable losses by new powering scheme

- **New sensor technologies**

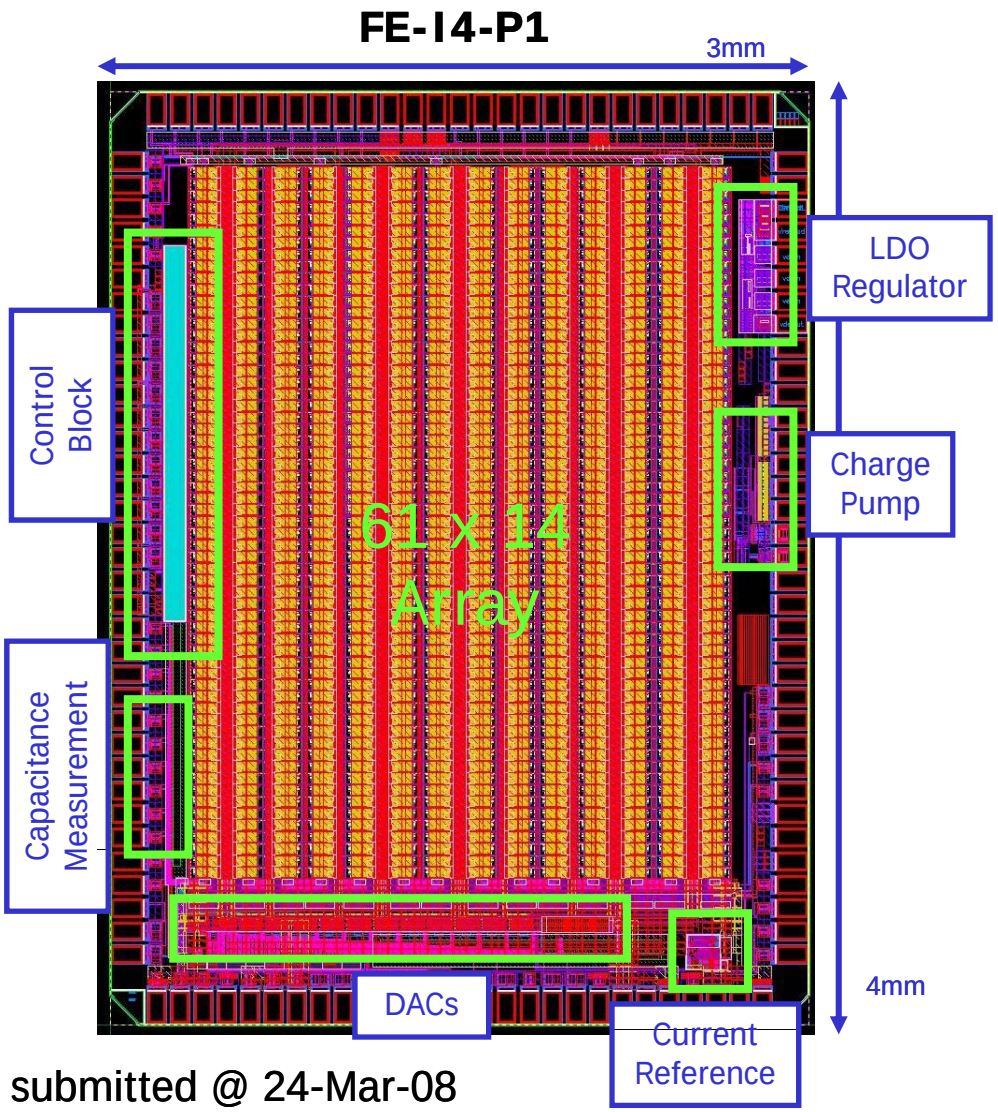
→ Adapt to several sensor types (3D,diamond, planar) with different detector cap. & leak.




**Why a new technology?**

- **Higher integration density for digital circuits**
- **Increased radiation tolerance of 130nm tech. with respect to 250nm tech.**

# Collaboration Effort




submitted @ 24-Mar-08

**institutes involved:**
Bonn, CPPM, Genova, LBNL, Nikhef

**core blocks**

- analog readout electronics
- new concept of digital pixel logic
- readout scheme of double column

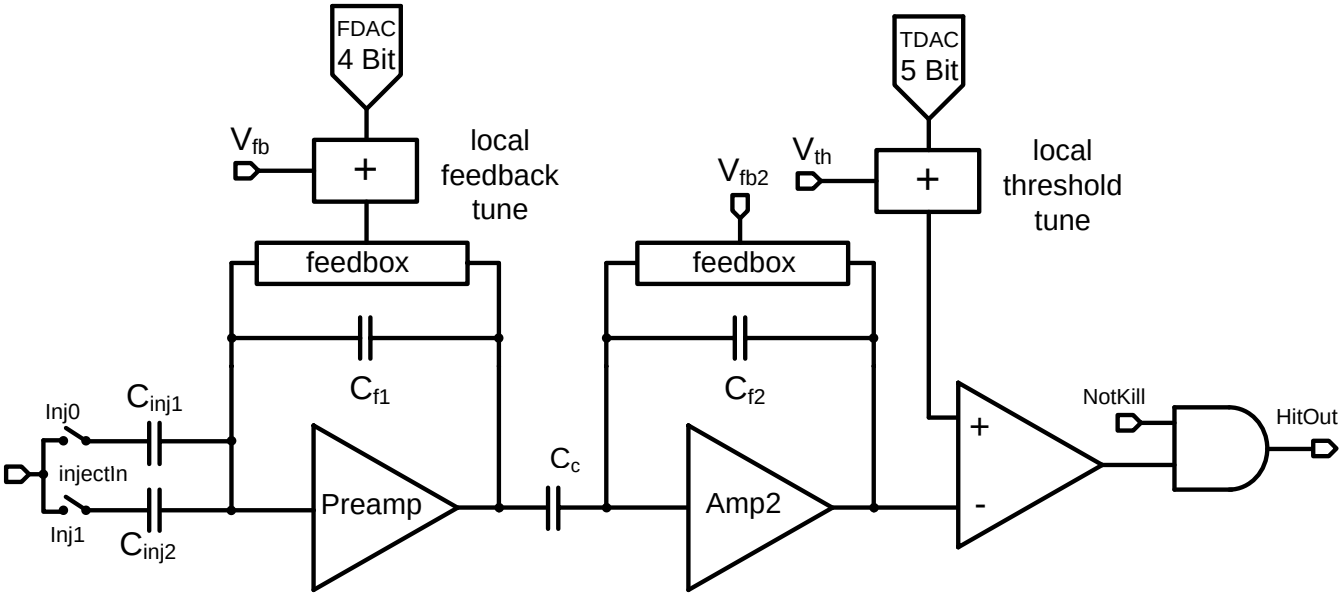
**peripheric blocks**

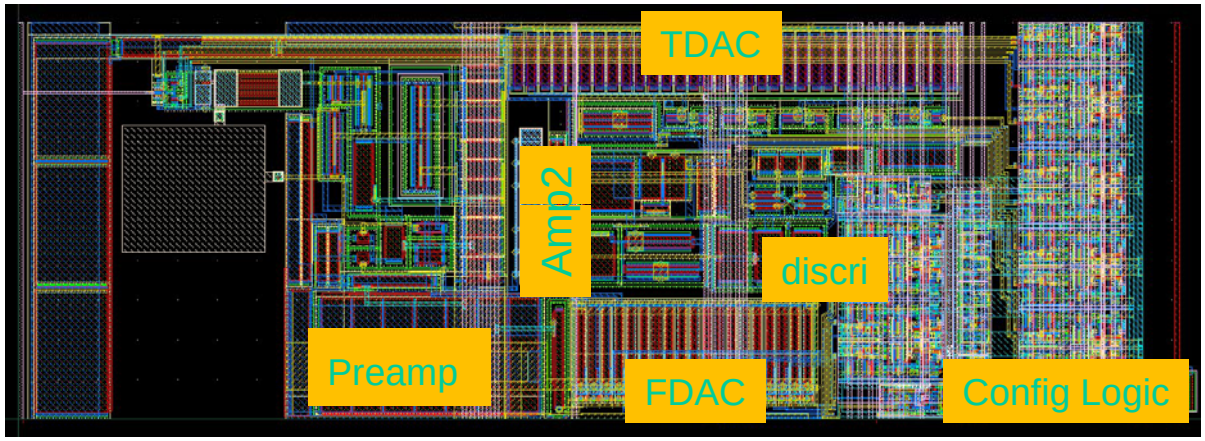
- bandgap reference & DACs → biasing & calibration
- voltage regulators → power management
- LVDS TX/RX → fast off-chip communication
- slow control

**collaborative tools**

- weekly phone meeting
- VCS shared design database based on ClioSoft tool

# Analog Readout Chain



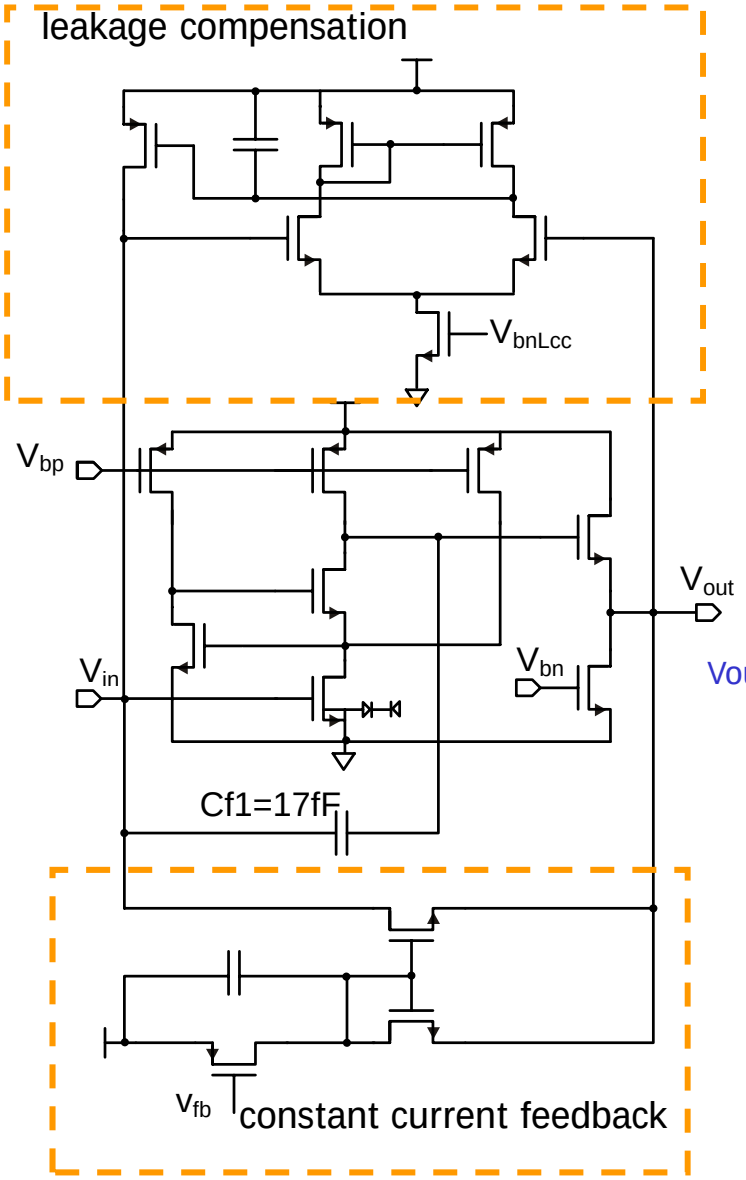




**50 µm**

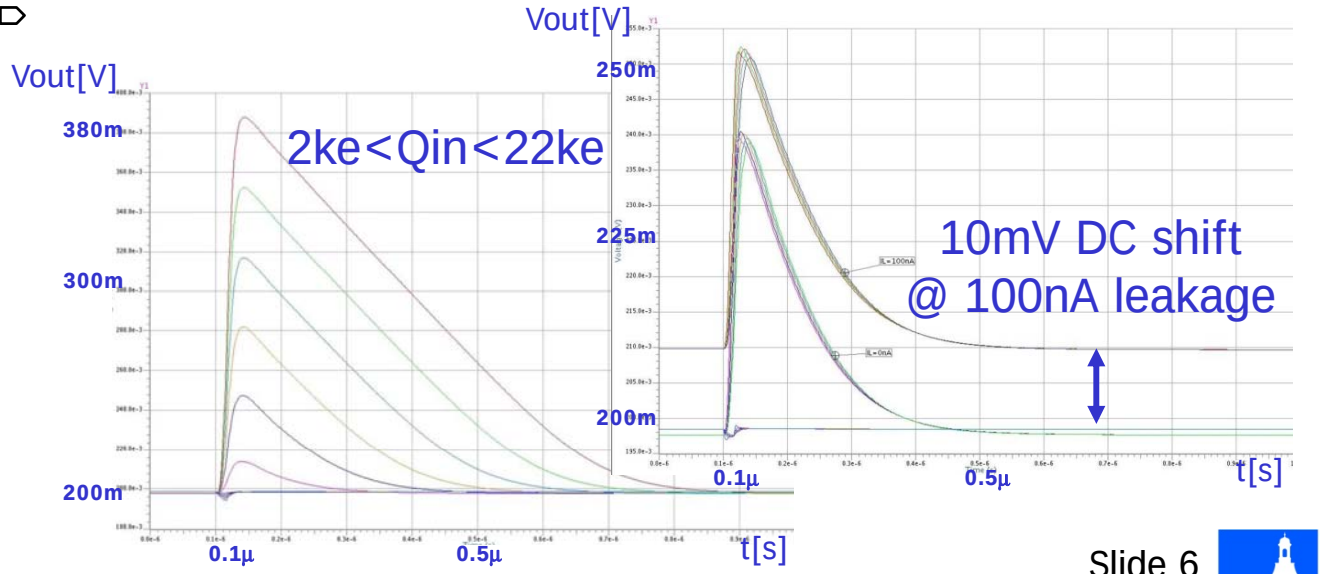
**145 µm**

- two-stage architecture optimized for low power, low noise and fast rise time
- additional gain Cc/Cf2~ 6
- more flexibility on choice of Cf1
- charge collection less dependent on detector capacitor
- decoupled from preamplifier DC potential shift caused by leakage
- Local DACs for tuning feedback current and global threshold
- charge injection circuitry

# Preamplifier Feedback & Leakage Compensation

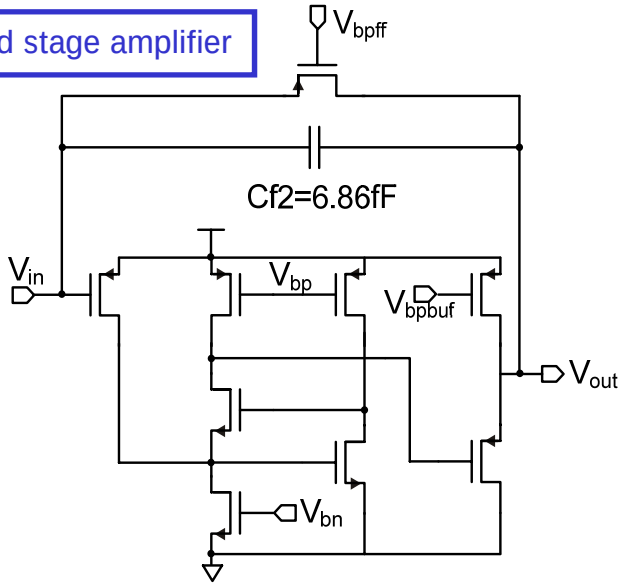



- Regulated cascode preamplifier
  → High gain
  → Less biasing voltages
  → Less crosstalk paths
- Triple Well NMOS input transistor
  → shielded from substrate noise
- NMOS feedback transistor for constant current discharge of the feedback capacitor
- Leakage current compensation based on differential amplifier

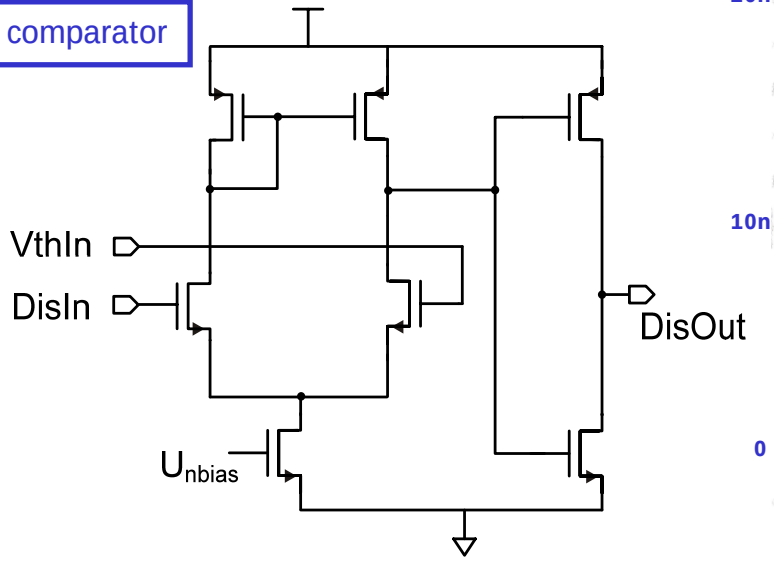


# 2-nd Stage Amplifier & Comparator

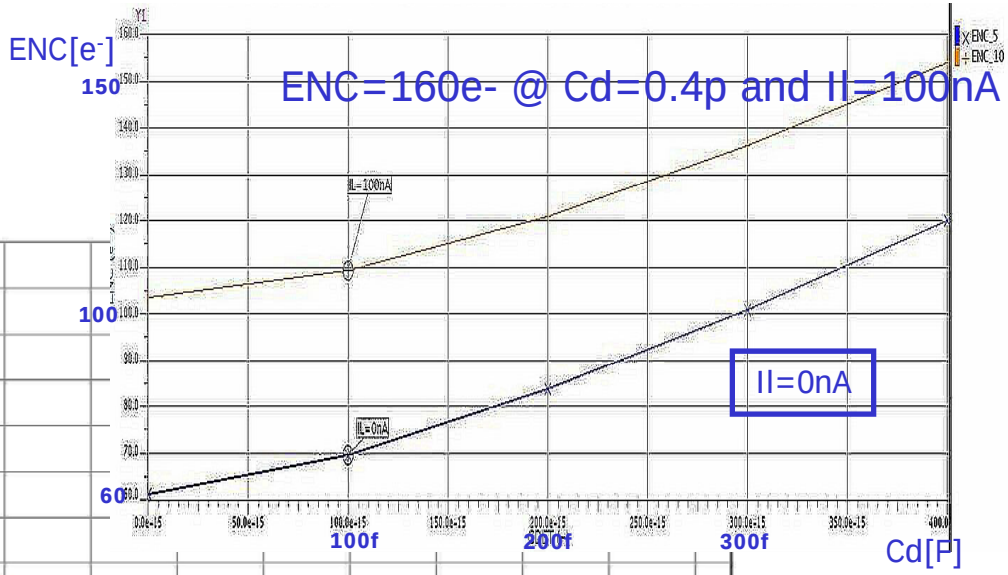
2nd stage amplifier

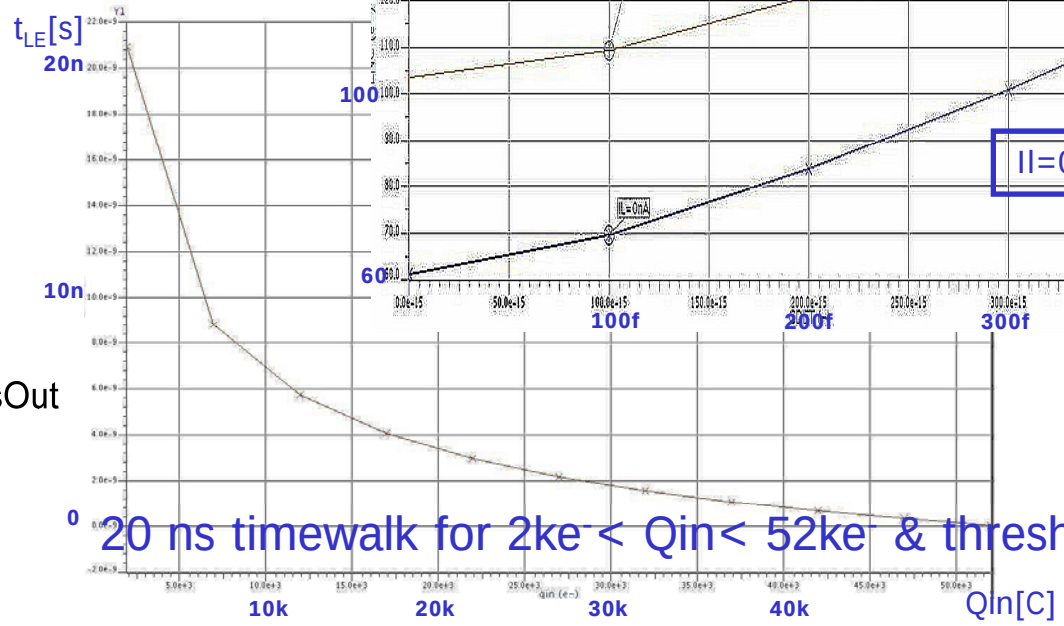



comparator




- PMOS input folded regulated cascode
- expecting negative going output
- might be changed to straight cascode
- classic 2-stage comparator design

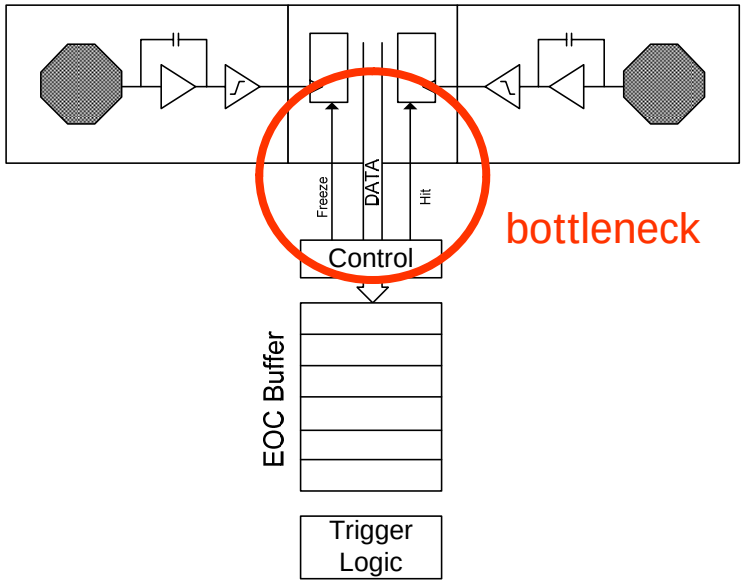


# Digital Readout Architecture

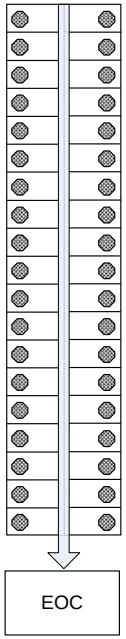
## FE-I3

Digital Part

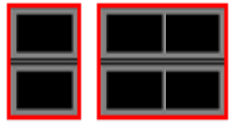



- All pixel hits are sent to the EoC buffer outside the active area at the bottom of the chip
- A hit pixel is blocked until the double column bus is free and the data has been sent out
- Every Pixel has its own digital circuitry

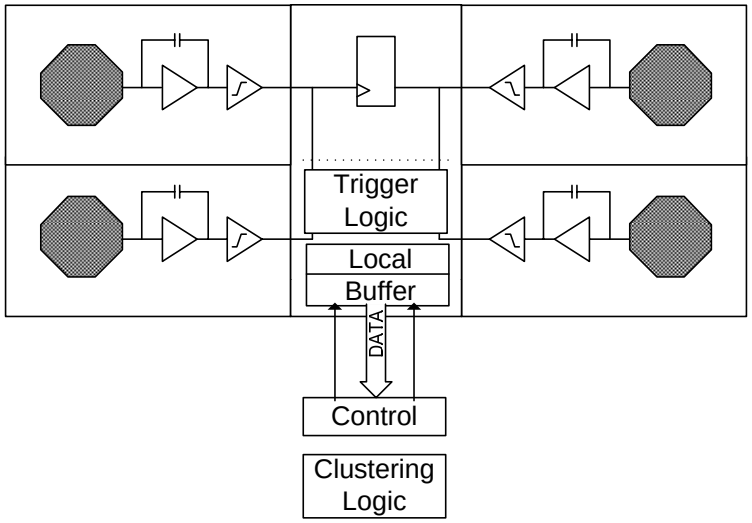
Both FE readout based on double column structure




## FE-I4



Shared Digital Part




- 99% of hits will not be triggered for off-chip transmission → no need to move hits to EoC!

→ Storage of hits in buffers at pixel level
→ Local synchronization to trigger latency

- Pixels are grouped together to logic units. Logic units are grouped to buffer regions

# Simulation of Digital Architecture

## Two sources of inefficiencies are identified in the FE-I4 architecture

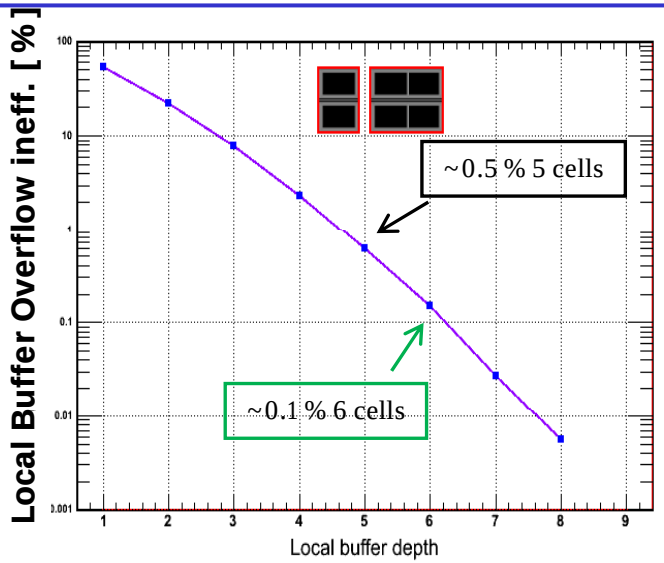
- Pile-Up Inefficiency: proportional to logic unit (pixel) area & mean ToT.

Handle: reduce cross-section (back to single pixel or truncation); aggressive return to baseline (decrease ToT)

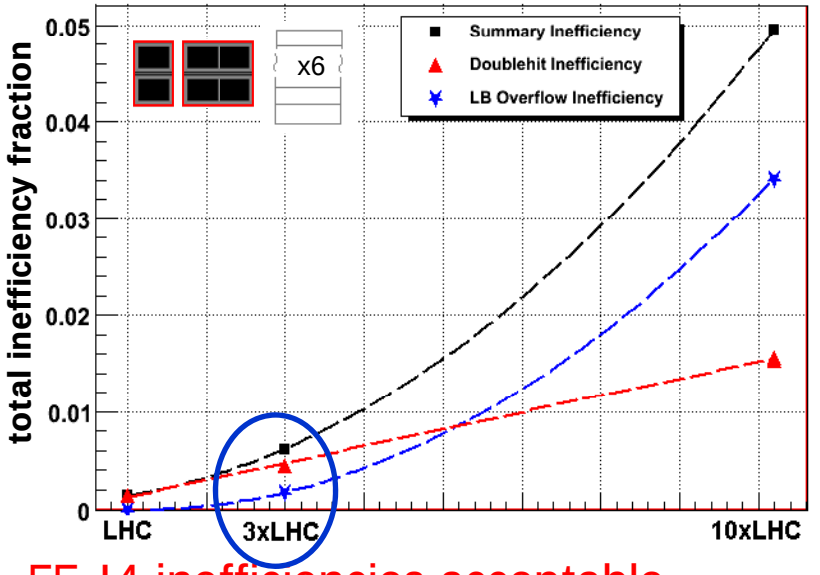
- Local Buffer Overflow Inefficiency:

Handle: increase size of Logic Unit / Local Buffer "averaging out effect"
increase # of cells per Local Buffer.

FE-I4 Local Buffer overflow ineff. as function of number of buffer cells (3xLHC)



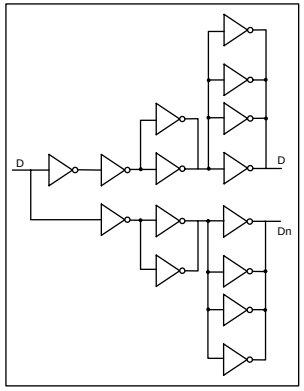

FE-I4 inefficiency as function of hit rate




At 2-3 times LHC luminosity and r~3.7cm, FE-I4 inefficiencies acceptable

Implementation at RTL & gate level (+ integration of the 2 simul. framework) is actively going on.

# LVDS Driver

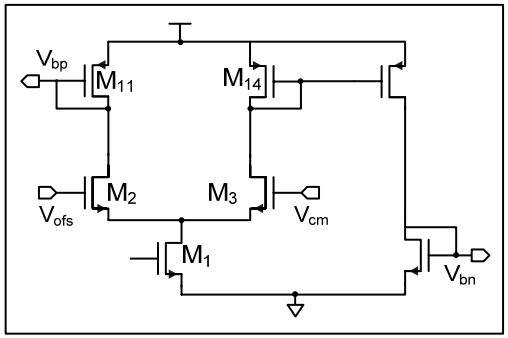






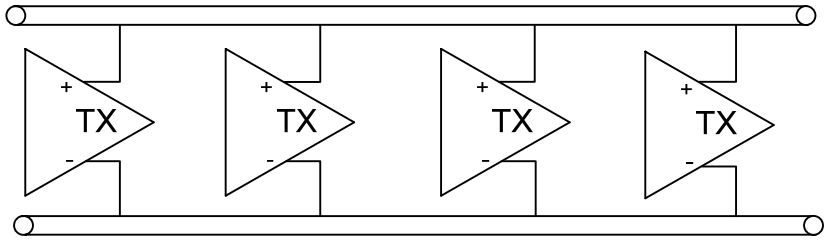


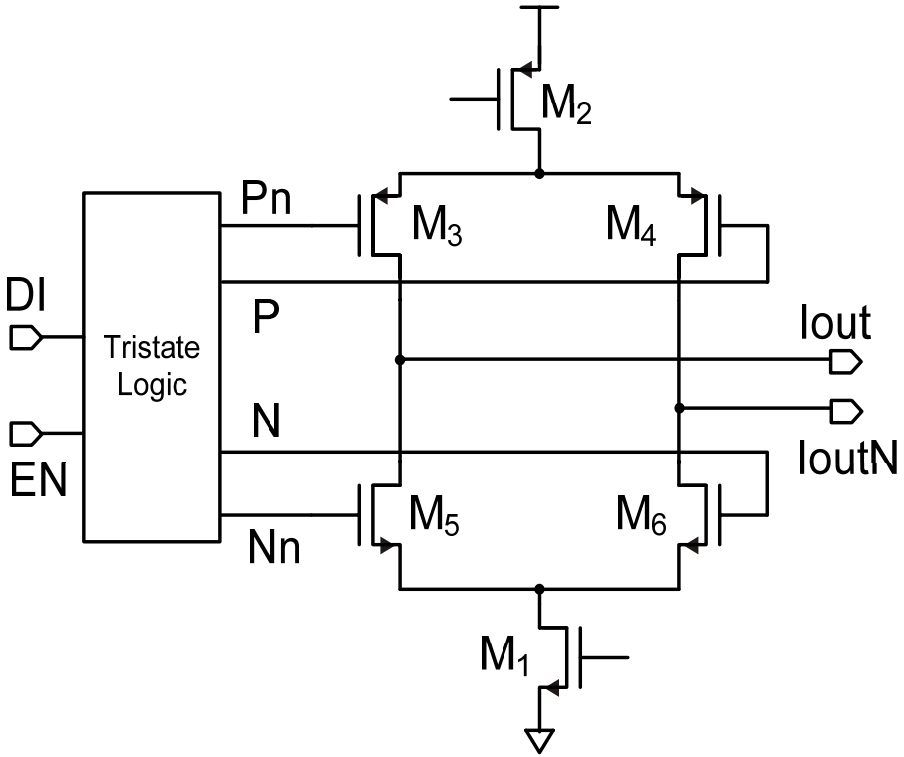

- Standard LVDS architecture for 320MHz clock rate and adapted to low supply voltage 1.5-1.2V
- Current is routed to/from the output by four switches M3-M6
- Common-mode voltage is measured by a resistive divider and controlled by a common-mode feedback circuit
- Output current is switchable between 0.6 -3mA




Boni et al., IEEE JSSC VOL. 36 NO. 4, 2001

# LVDS Driver with Tristate Option



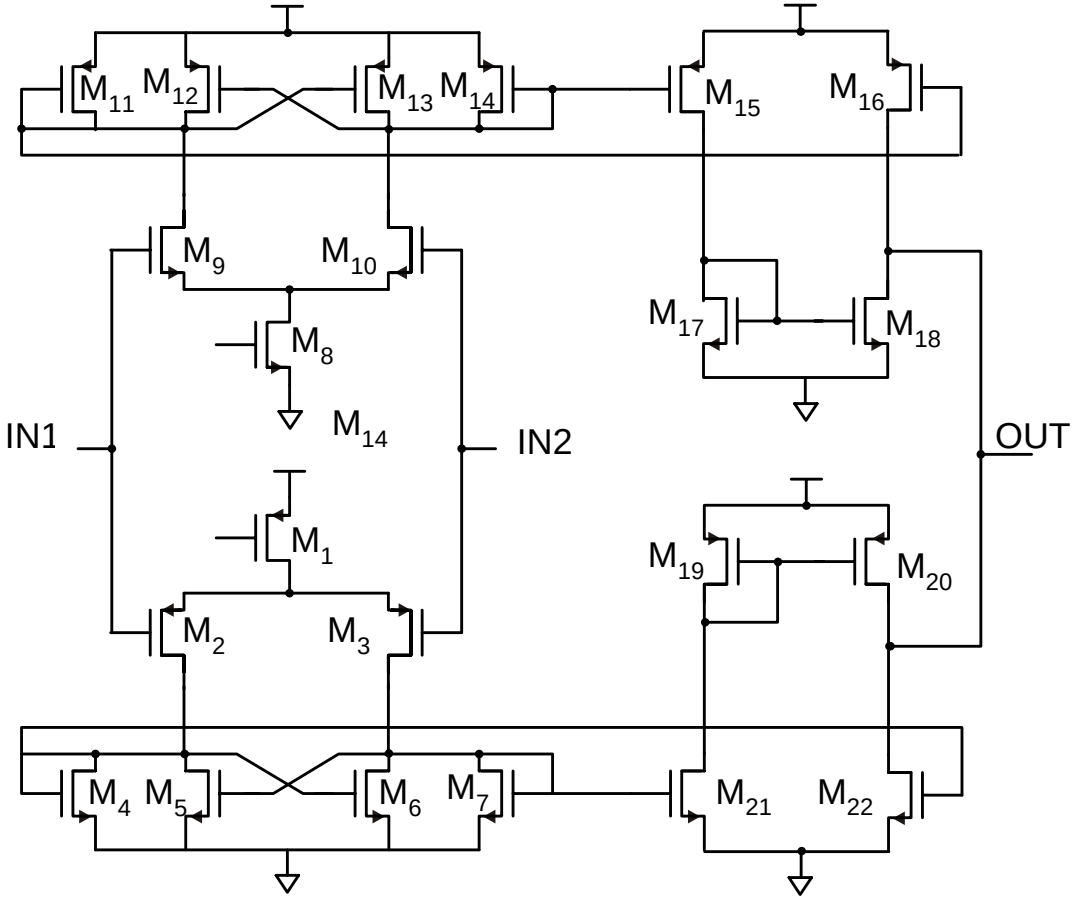




- Might be beneficial for multiplexing the output signal of several FE chips through one transmission line at the outer layers
- Switching Transistors M3 - M6 are steered by seperate signals
- All switches can be left open at the same time giving a high impedance state at the LVDS driver output
- Switching signals are set by additional tristate logic

Tristate Logic

| DI | EN | N | Nn | P | Pn | Out |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | hZ |
| 1 | 0 | 0 | 0 | 1 | 1 | hZ |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 |

# LVDS Receiver

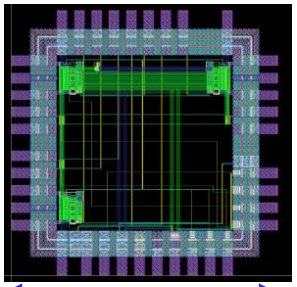



- parallel PMOS/NMOS comparator input stages allow operation in a wide range of common-mode voltages
- cross coupled positive feedback structure allows introduction of hysteresis
- second stage sums singals from both input stage and converts them to a CMOS output signal

Tyhach et al., A 90-nm FPGA I/O Buffer Design With 1.6-Gb/s Data Rate for Source-Synchronous System and 300-MHz Clock Rate for External Memory Interface, IEEE JSSC, Sept. 2005

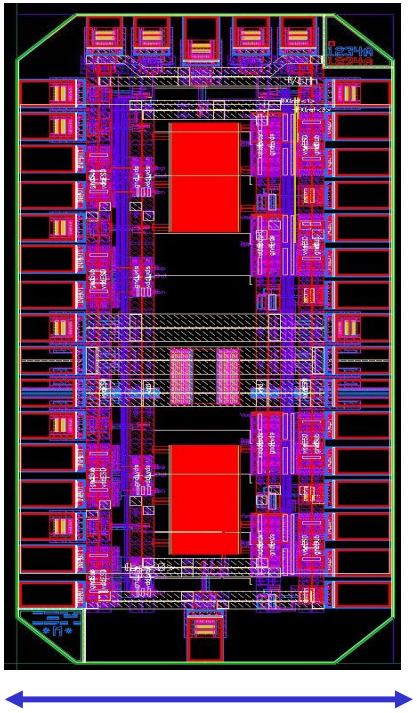
# LVDS Chip Layout & Measurements

## UMC 130nm




- **21-Jul-2007:** first test chip submitted to UMC 130nm via Europractice mini-asic run
  → real hardware test of chosen architecture for use in FE-I4
- **24-Mar-2008:** 4 channel LVDS transceiver chip submitted to IBM 130nm (LM) via CERN
  → for use in a SEU test setup
  → characterization of new cables and flex types
- **15-Sep-2008:** LVDS driver with tristate option submitted to IBM130nm (DM) via MOSIS

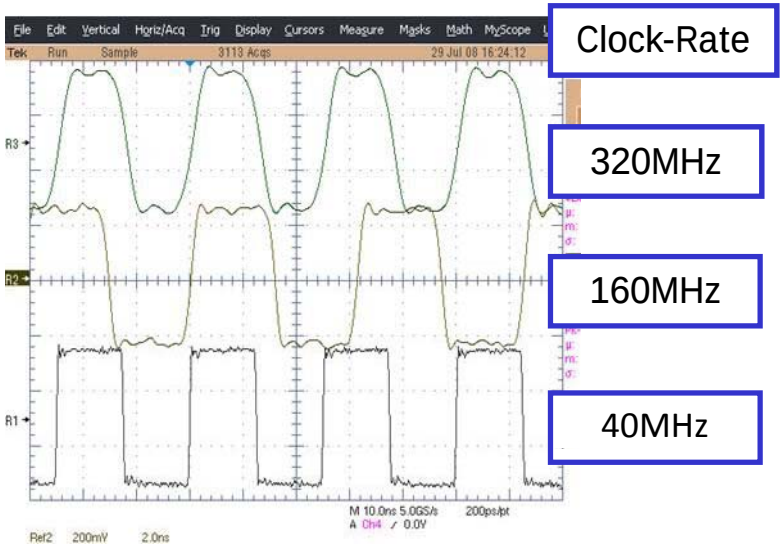
## IBM 130nm



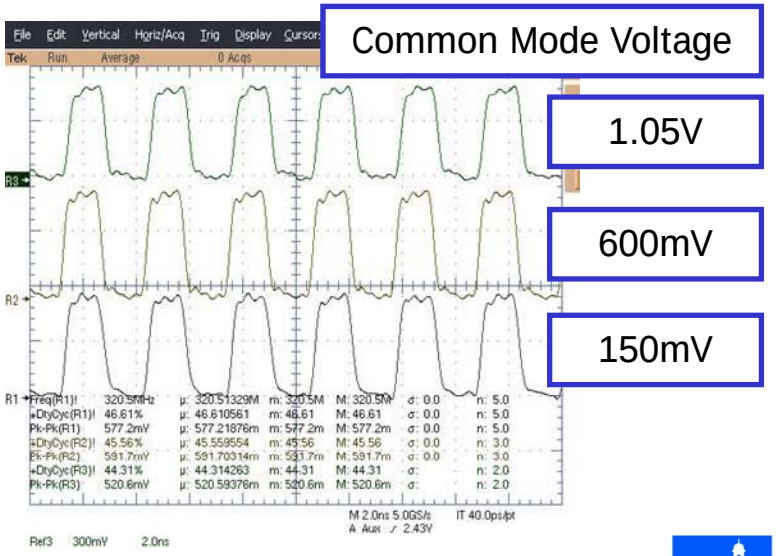

## Preliminary Measurements on the IBM 130nm Transceiver Chip

with differential probe and 100 Ohm on board termination @ 1.2V supply

### TX output




### Chained RxTx output @ 320 MHz Clock



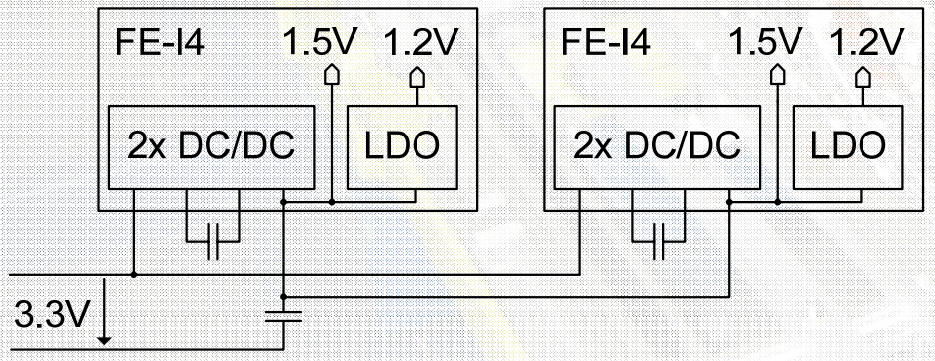
# Powering Options Under Consideration

- Reduction of cable material budget
- Limitation of cable power losses

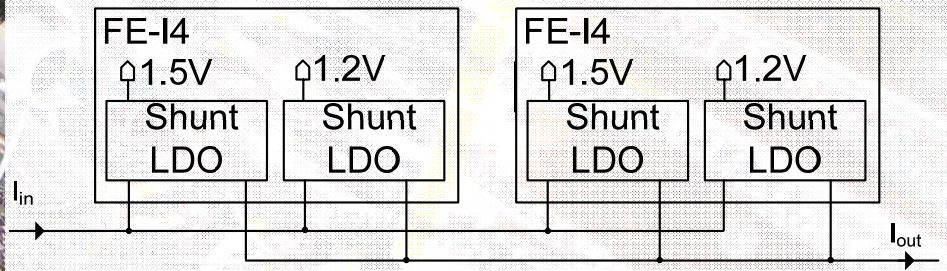
→Minimization of current flowing through supply lines

Two powering options are investigated:

x2 DC/DC switched capacitor based conversion

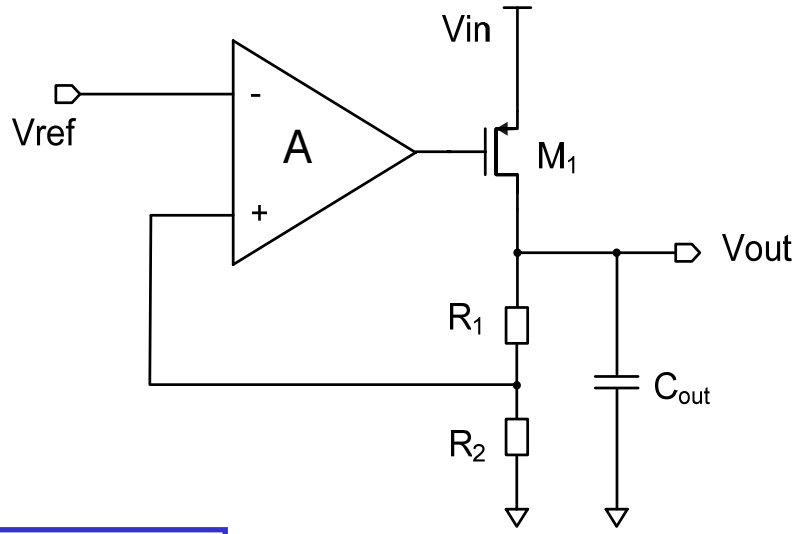



serial powered modules & „Shunt LDO“ regulation



# Low Drop Out Regulator

## LDO useful for both powering schemes




### Specification

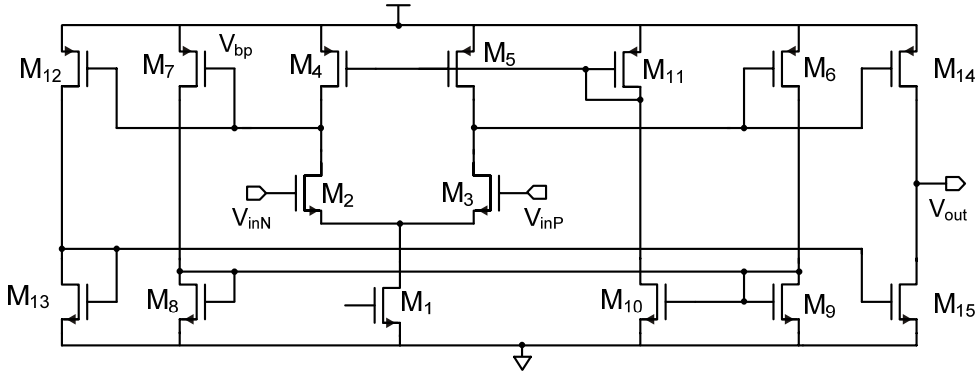
- LDO regulator for Vin=1.6V,Vout=1.5-1.2V minimun drop out voltage 100mV
- Iload=500mA
- Line Regulation :

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{g_{mpt} r_{opt}}{A\beta} = \frac{5mV}{100mV} = \frac{1}{20}$$

- Load Regulation:

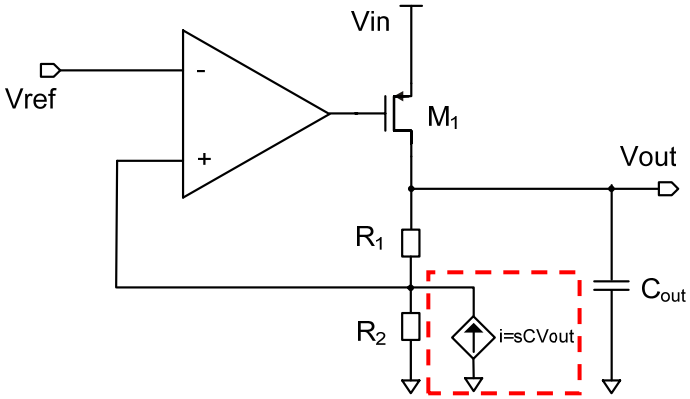
$$\frac{\Delta Vout}{\Delta I_{load}} = \frac{r_{opt}}{1 + A\beta} = \frac{5mV}{150mA} = 33m\Omega$$

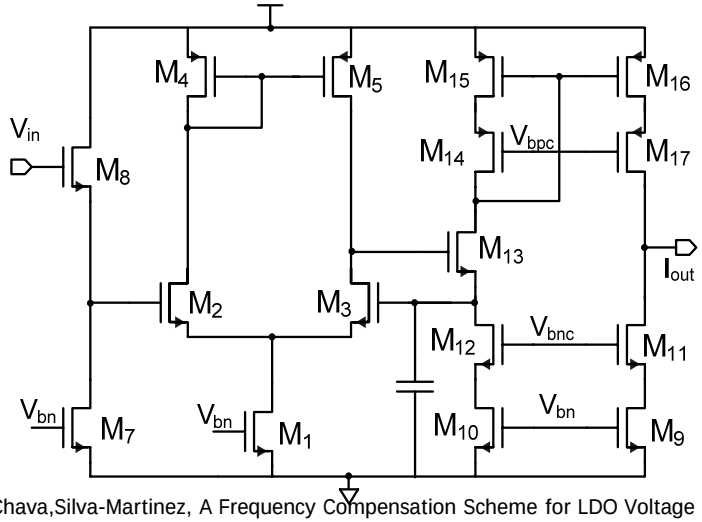
### Error Amplifier



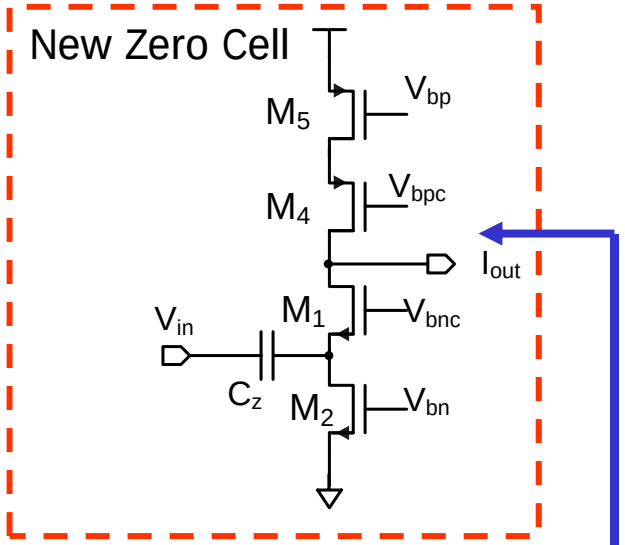

- 2 stage error amplifier with fully-differential first stage and common-mode feedback biasing
- Rail-to-rail Class-AB output
- No need for transistors M4 & M5 to be gate-drain connected which would reduce the output impedance and the gain of the first stage

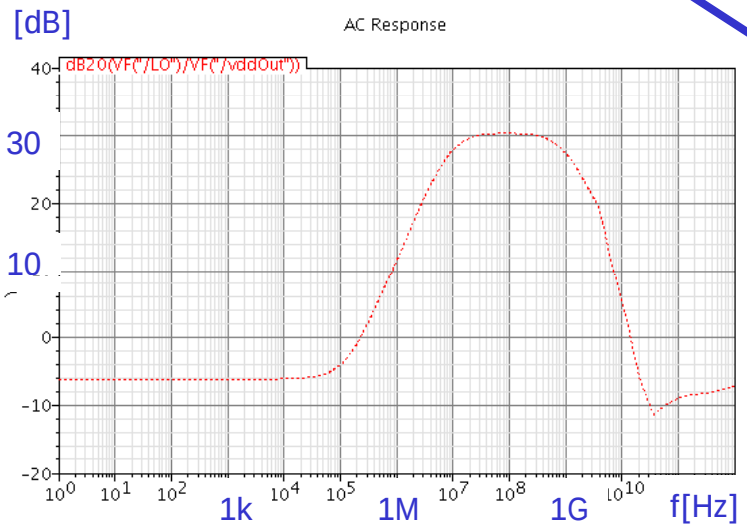
# LDO Stabilization by Zero Cell




Chava,Silva-Martinez, A Frequency Compensation Scheme for LDO Voltage Regulators, IEEE Transactions on Circuits and Systems, June 2004



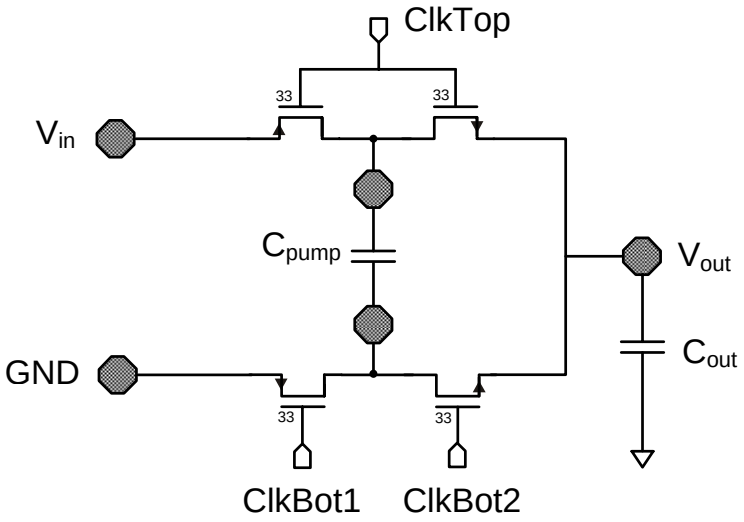




- Zero is introduced in the open loop transfer function by a frequency dependent voltage controlled current source
- Less peaking of Vout in comparison with compensation by $R_{ESR}$ of Cout
- A frequency dependent current is flowing through the capacitor at the source of M13 which is mirrored to the output.

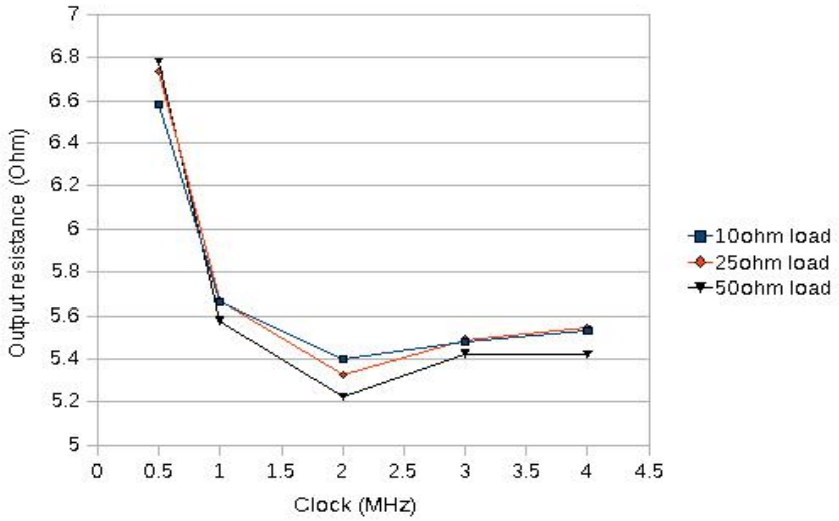
- New Zero Cell based on transimpedance amplifier input stage
- AC coupled input → No need for source follower -> No current mirror
- Only pole: Input impedance at the source of M1 → High bandwidth

submitted to IBM 130nm (DM) 15-Sep-2008 via MOSIS

# 2x DC/DC switched capacitor based conversion




Measurement with Cpump=0.22uF (0201 package)



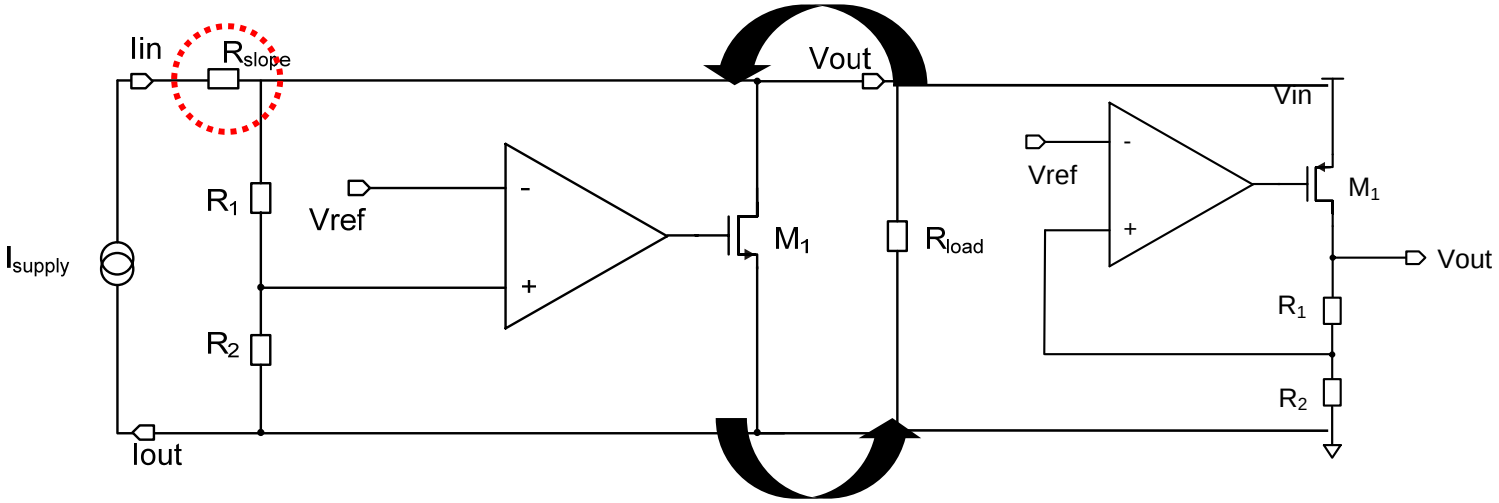

- On chip four transistor switching scheme using 3.3V thick gate oxide devices
- To avoid shorts between Vin & Vout or Vout & GND three nonoverlapping clocks are used

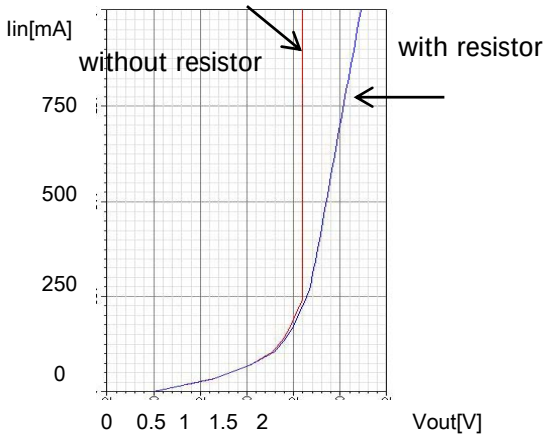
Rout includes 25mu long wire bond resistances single in- & output and cap bonds due to small pads

Good radiation performance of 3.3V ELT NMOS transistor is crucial for succesful operation

First irrradiation results are very encouraging (see spare slide)

# New Shunt Concept Basic Ideas




- Shunt regulator generates constant output voltage out of a current supply.
- Parrallel placed shunt regulatros need an input resistor $R_{slope}$ for safe operation
- Resistor $R_{slope}$ reduces the slope of the Iin=f(Vout) characteristic

→ Mismatch has less influence on current distribution and device break down is avoided

- Rslope has no regulation contribution but burns power

→ Replacement of Rslope by a regulated „resistor“

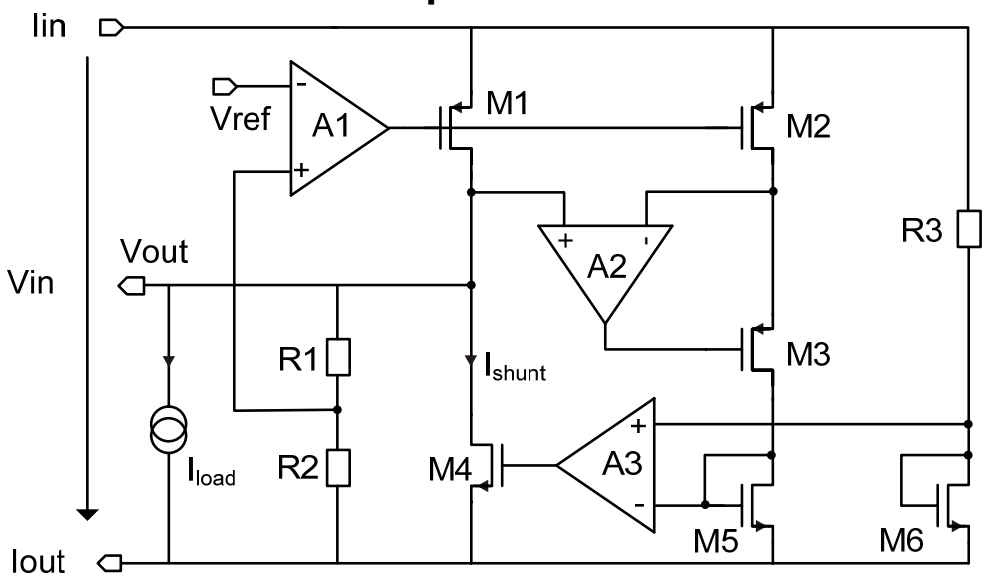
- Shunt regulator was meant to be used in combination with a LDO

→ Change chain order and place LDO before the shunt

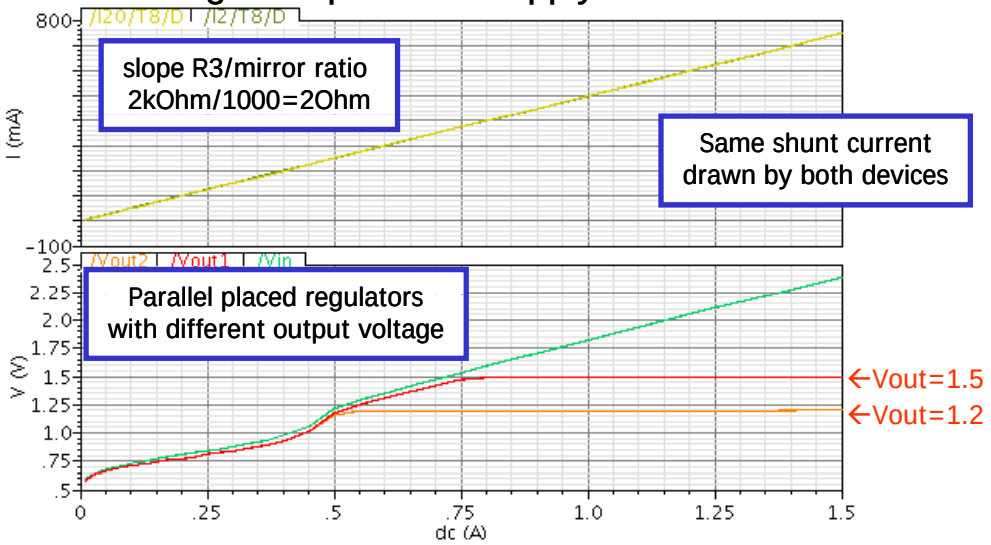
- The LDO PMOS power transistor becomes the regulated „resistor“ Rslope
- The shunt transistor becomes part of the LDO load

# LDO Regulator with Shunt Transistor

**Simplified Schematic**




- Combination of LDO and shunt transistor
- M4 shunts the current not drawn by the load
- Fraction of M1 current is mirrored & drained into M5
- Amplifier A2 & M3 improve mirroring accuracy
- Ref. current defined by resistor R3 & drained into M6
- Comparison of M5 and ref. current leads to constant current flow in M1
- Ref. current depends on voltage drop $V_{Iin}$ - $V_{out}$ which again depends on supply current Iin




- „Shunt-LDO“ regulators having completely different output voltages can be placed in parallel without any problem regarding mismatch & shunt current distribution
- Resistor R3 mismatch will lead to some variation of shunt current but will not destroy the regulator
- „Shunt-LDO“ can cope with an increased supply current if one FE-I4 does not contribute to shunt current e.g. disconnected wirebond → ref current goes up
- Can be used as an ordinary LDO when shunt is disabled

submitted to IBM 130nm (DM) 15-Sep-2008 via MOSIS

# Conclusion / Plans

- New Pixel Front-End IC targeting both b-layer upgrade and the outer layers of sLHC is being developed

- The prototype FE-I4-P1, LVDS Transceiver & SEU Test Chip returned from production

| | |
|---|---|
| Analog Pixel Array | LDO Regulator |
| Current Reference | LVDS TX/RX |
| DC/DC Charge Pump | Control Block |
| Cap. Measurement | SEU Test Structure |

- Functional test and Pre & Post irradiation characterization is beeing performed

- Digital architecture of FE-I4 is currently being defined. Implementation at RTL level has started.

- Additional blocks to study new concepts on real hardware have been developed & submitted
  LDO with shunt ability→ „SHULDO“, LDO with enhanced „Zero Cell“ compensation, LVDS tristate driver

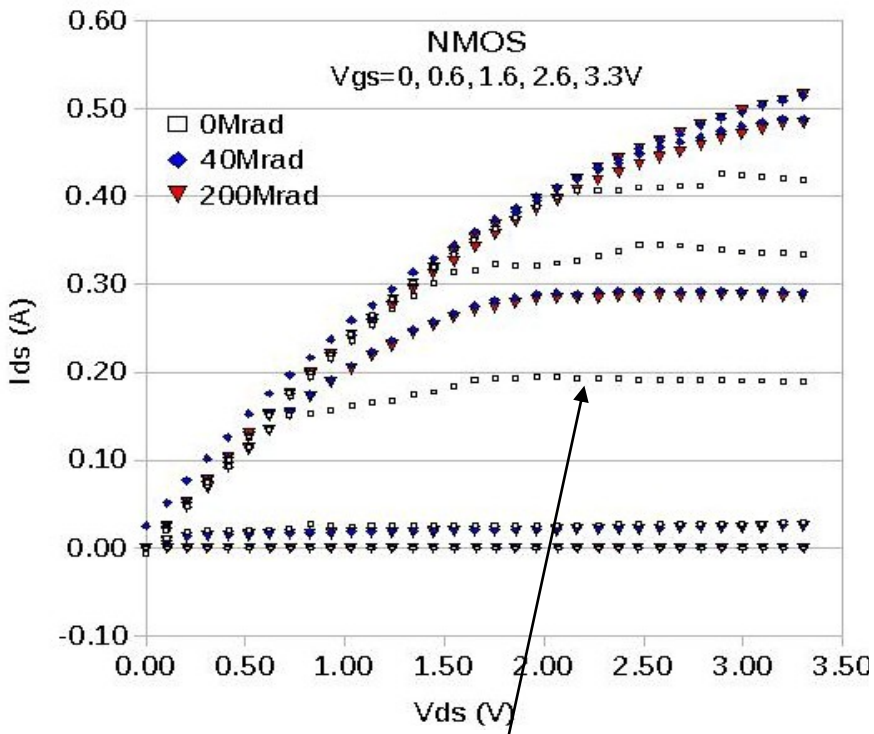
Design of a full-scale layout is foreseen for the year 2009

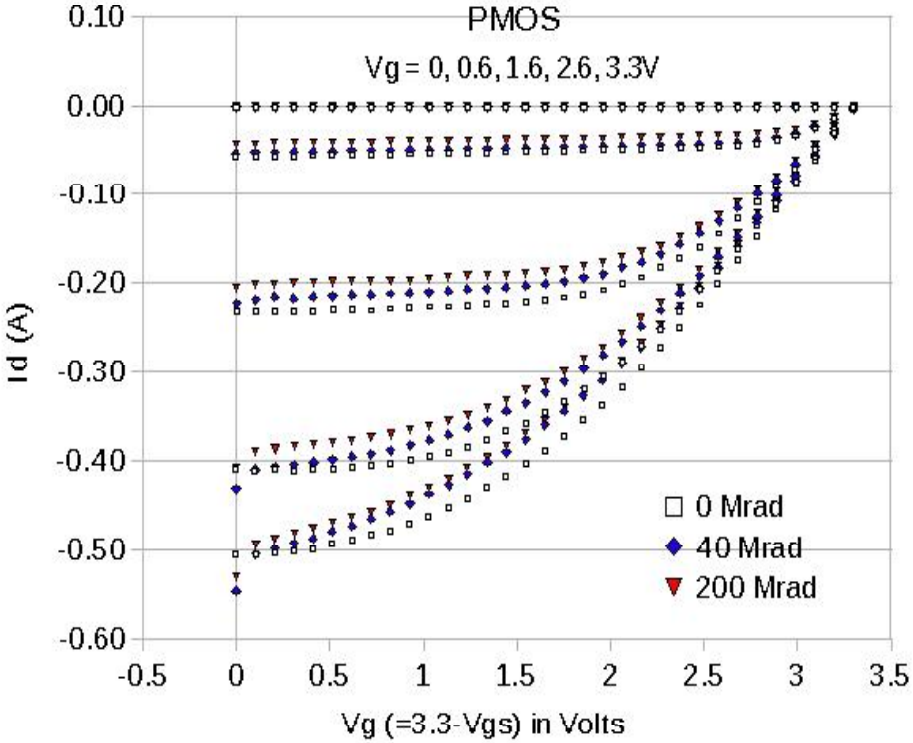
# SPARE SLIDE: FE-I4 Specification

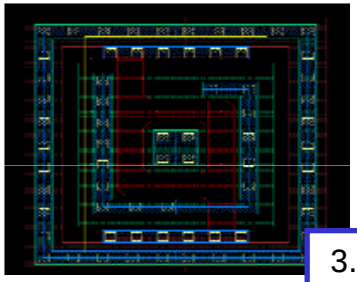
| | | |
|---|---|---|
| Pixel size | **50 x 250** | $\mu m^2$ |
| DC leakage current tolerance | 100 | nA |
| Pixel array size | **≥ 64 x 320** | Col x Row |
| Normal pixel input capacitance range | 300-500 | fF |
| Long pixel input capacitance range | 450-700 | fF |
| In-time threshold with 20ns gate (400pF)* | 4000 | e |
| Hit-trigger association resolution | 25 | ns |
| Same pixel two-hit discrimination (time) | 400 | ns |
| Single channel ENC sigma (400fF) | 300 | e |
| Tuned threshold dispersion (max) | 100 | e |
| Charge resolution | 4 | bits |
| ADC method | TOT | |
| Operating voltage range | 1.2 – 1.5 | V |
| Total analog supply current @400fF | 10 | µA / pixel |
| Radiation tolerance (specs met at this dose) | 200 | MRad |
| Average hit rate | 200 | $MHz/cm^2$ |
| Trigger latency (max) | 3.2 | µs |
| Single chip data output rate | 160 | Mb/s |
| Maximum trigger rate | 200 | KHz |
| Total digital supply current @ 100KHz | 10 | µA / pixel |

# SPARE SLIDE: Preliminary irradiation results

**First measurement of enclosed geometry 3.3V transistors in 0.13um process**



3.3V NMOS ELT

0 dose curves look funny due to some parasitic turning on. Transistor being measured is not isolated. Somehow the radiation has cured this parasitic.

# SPARE SLIDE: Chip Yield

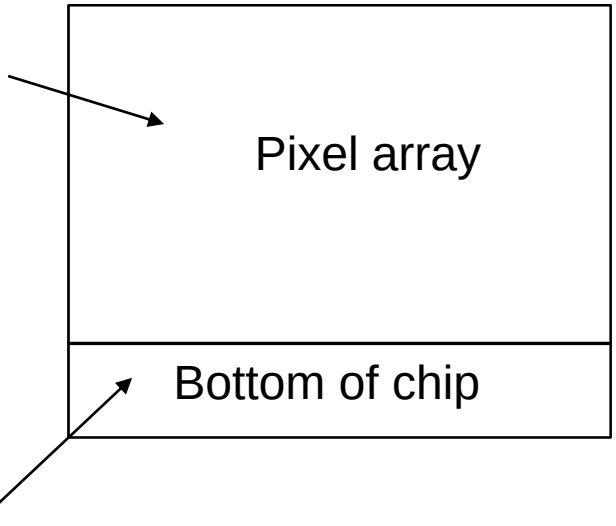
Defects in the pixel array should lead by redundant design predominantly to the loss of a single pixel or region.

A few dead pixels or regions can be tolerated for physics grade chips

Even with some dead pixels its like having 100% yield

Assuming 15% of the pixel area contains very critical circuits meaning defects there would lead to the loss of more than one pixel or region (e.g. whole column)

We get Y= 78% for array A = 20mm x 17mm




Bottom of Chip is more critical:

$$\text{Yield} = [\ (1-e^{-DA}) / DA\ ]^2,$$

A = circuit area (~independent of array size)
D = defect density ~ 0.5 / sq. cm. (from MOSIS)
for A=2mm x 20mm, Yield = 82%

Combined yield = 64% for 80x336 chip, 68% for 64x320 chip

# The ATLAS Pixel Upgrade FE-I4 collaboration

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