Development of the ATLAS FE-I4 pixel readout IC for b-layer Upgrade and Super-LHC

M. Karagounis[a], D. Arutinov[a], M. Barbero[a], R. Beccherle[c], G. Darbo[c], R. Ely[d], D. Fougeron[c], M. Garcia-Sciveres[d], D. Gnani[d], V. Gromov[e], T. Hemperek[a], H. Junker[a], M. Menouni[b], A . Mekkaoui[d], R. Kluit[e], J.D. Schipper[e]

[a] Physikalisches Institut der Universität Bonn, Nussallee 12, D - 53115 Bonn, Germany
[b] CPPM, Aix-Marseille Universit, CNRS/IN2P3, Marseille, France
[c] INFN Genova via Dodecaneso 33, IT - 16146 Genova, Italy
[d] Lawrence Berkeley National Laboratory, 1 Cyclotron Road, Berkeley, CA 94720, USA
[e] Nikhef, National Institute for Subatomic Physics, Kruislaan 409, 1098 SJ Amsterdam, Netherlands

karagounis@physik.uni-bonn.de

Abstract

Motivated by the upcoming upgrade of the ATLAS hybrid pixel detector, a new Front-End (FE) IC is being developed in a 130nm technology to face the tightened requirements of the upgraded pixel system. The main design goals are the reduction of material and a decrease in power consumption combined with the capability to handle the higher hit rates that will result from the upgraded machine. New technology features like the higher integration density for digital circuits, better radiation tolerance and Triple-Well transistors are used for optimization and the implementation of new concepts. A description of the ongoing design work is given, focusing more on the analog part and peripheral design blocks.

I. ATLAS Pixel upgrade schedule and consequences on FE-I4 specification

The development of the FE-I4 pixel chip is motivated by planned upgrades to the ATLAS [1] pixel detector [3]. While upgrade plans are evolving, two distinct upgrades are expected based on the collider luminosity projections. The first upgrade, known as b-layer upgrade, is a new inner layer mounted on the beam pipe at a smaller radius and for luminosity a factor of 2 or 3 higher than present detector specifications. The second upgrade, known as Super-LHC, is on a longer time scale and it consists in the complete replacement of the ATLAS tracking detectors [2], for a luminosity 10 times higher than specified for the present one. The FE-I4 chip is aimed at inner layer use for the first upgrade, and outer layer use for the second upgrade, which is a natural fit because the hit rates for these two cases are comparable. The total area to be covered in the outer layers of the Super-LHC upgrade is about 4 times the total area of the present detector, and so reduction of manufacturing cost is an important requirement for FE-I4.

With a potential smaller b-layer radius and a 2-3 times higher luminosity, the hit rate the FE-I4 will have to deal with will rise significantly. Simulations performed on the current FE-I3 architecture to study the influence of the increased hit rate, show that an unacceptable high number of relevant hits get lost because of pile up effects in the pixels and congestion in the double column data bus [5]. Hence a smaller pixel geometry of $50 \times 250 \mu m^2$ has been chosen to reduce the pixel cross section, having also a benefit on tracking resolution. In addition the digital pixel logic and the double column bus scheme have to be reorganized in a new architecture that is able to process the higher hit data volume. Serial links operating at 160MHz are needed for sending triggered hit data off-chip.

Driven by the need to reduce material and bump-bonding cost, the overall chip size will be increased close to the technology's limits to approximately $20.0 \times 18.6 mm^2$. In addition, the higher integration density the new technology offers allows to go to smaller peripheral chip area sizes which increases the active fraction from 74% in FE-I3 to almost 90% in FE-I4. Since bump bonding costs scale with the number of parts that have to be handled during the bonding process, both the bigger chip size and the use of fewer chips per module lower the manufacturing cost.

Material reduction is also correlated to power consumption. To reduce the cable budget and at the same time limit the power losses in the cable, the current flowing through the supply lines has to be minimized. On that account $10 \mu A$ current target for the analog readout chain has been defined per pixel. The same amount of current is dedicated to the digital pixel logic which is sufficient because with the new FE-I4 digital architecture concept the digital activity is much reduced (see section III.). Moreover different powering schemes like serial powering or divide-by-two DC/DC conversion are under consideration to improve efficiency with respect to the conventional parallel powering approach. A comparison between some of the specifications of FE-I3 and FE-I4 is given in table 1.

In the following sections the analog circuits that have been

Table 1: Specification comparison between FE-I3 & FE-I4 target [3, 4]

	FE-I3	FE-I4
Pixel Size	$50 \times 400 \mu m^2$	$50 \times 250 \mu m^2$
Pixel Array	18×160	80×336
Chip Size	$7.6 \times 10.8 mm^2$	$20.0 \times 18.6 mm^2$
Active Fraction	74%	89%
Analog Current	$16 \mu A$/pixel	$10 \mu A$/pixel
Digital Current	$10 \mu A$/pixel	$10 \mu A$/pixel
Analog Supply Voltage	1.6V	1.5V
Digital Supply Voltage	2.0V	1.2V
Data Rate	40Mb/s	160Mb/s

submitted in 2008 on a FE-I4 prototype and on additional test chips are described and a short introduction to the digital architecture is given.

II. Analog Readout Chain

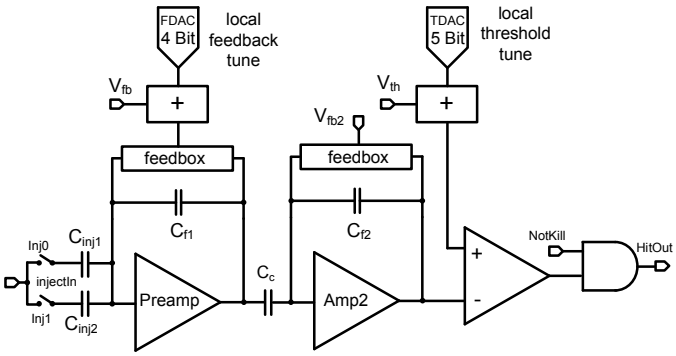

Figure 1: Analog Readout Architecture

The analog pixel readout chain shown in Figure 1 has been implemented as a two-stage architecture, optimized for low noise, low power and fast rise time. The output signal of the second stage is coupled to a discriminator for comparison with a global threshold. Threshold tuning and trimming of the preamplifier's feedback current is applied by dedicated local DACs. Calibration of the analog pixel electronics is performed by a local charge injection circuitry.

The two-stage approach offers more options for optimization than an ordinary single-stage. The second stage gives an additional amplification factor that is defined by the ratio of the coupling capacitor C_c to the feedback capacitor C_{f2} of the second stage. This extra gain allows to increase the preamplifier feedback capacitance C_{f1} about the same factor without reducing for a given charge input signal the signal pulse magnitude arising at the comparator's input.

A higher preamplifier feedback capacitance is advantageous for charge collection efficiency, signal rise time and power consumption. To have a high charge collection efficiency, the effective collection capacitance of the charge sensitive amplifier (CSA) which is defined as the product of the preamplifier gain times the feedback capacitor has to be much higher than the detector capacitance. Going to higher feedback capacitances has the benefit that a good charge collection efficiency independent of detector capacitance can be achieved with less preamplifier gain and as a result less power. Signal rise time scales inverse proportional to the transconductance of the preamplifier's input transistor and the feedback capacitance. With a high feedback capacitance a specific signal rise time can be met with less transconductance of the preamplifier's input transistor which again means less current and less power.

Furthermore the AC-coupling between first and second stage has the advantage that the rear part of the analog readout chain is decoupled from any DC-shift that could arise because of detector leakage current. Although the pixel is equipped with a leakage current compensation circuit, still the non ideal behavior of the compensation circuit gives rise to small DC-shifts which without AC-coupling would influence the system and would lead to threshold dispersion.

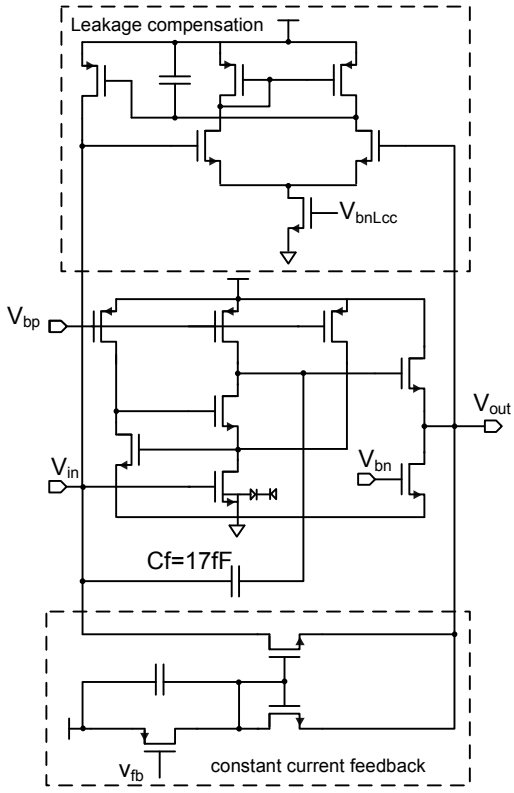

Figure 2: leakage compensated CSA with constant current feedback

The schematic of the leakage current compensated CSA with constant current feedback that forms the first stage is shown in Figure 2. The preamplifier is implemented as a regulated telescopic cascode with a Triple-Well NMOS input transistor. The availability of Triple-Well transistors allows to exploit the higher transconductance of NMOS transistors with respect to PMOS due to higher mobility and still be shielded from substrate noise. Furthermore the NMOS input transistor gives a low DC output potential that introduces a high dynamic range for the expected positive going output signals. The regulated cascode has a high output impedance and hence a high gain. Moreover the regulated scheme needs less biasing voltages and thus has less crosstalk paths and eases routing. The telescopic structure has the advantage that the highest current in the amplifier flows through the input transistor and not through any biasing transistor which reduces the noise contribution from the biasing.

Continuous reset is applied by a NMOS feedback transistor which is biased by a current mirror topology. For high output signals, the NMOS feedback transistor gets saturated and drains a constant current. A nearly linear return to baseline and as a result a pulse width proportional to the input charge is obtained.

A slow differential amplifier monitors the DC shift between input and output of the preamplifier caused by the detector leakage current. If a leakage current is drawn out of the input, the

rising output potential is sensed and a dedicated PMOS transistor connected to the input is steered to compensate for the leakage current flow. Simulations show that for a leakage current of about 100nA, the resulting DC shift is limited by the compensation circuit to 10mV.

The second stage is a PMOS folded cascode. A PMOS input transistor has been chosen due to the well suited output potential that gives a high dynamic range for the expected negative going output signal. Finally the comparator is made out of a classic two stage architecture. The overall analog readout chain performance has been simulated and the results show an ENC dependence on the detector capacitance of $70e^- + 0.15e^-/fF$. The timewalk with a threshold of $1.5ke^-$ and the charge input signal varying between $2ke^-$ and $52ke^-$ is about 20ns.

III. Digital Architecture

As seen in section I a digital architecture different than in FE-I3 has to be designed to increase the hit rate capability and reduce the digital activity for power saving. First it is crucial to identify the limitations and restrictions of the currently used FE-I3 architecture. The readout of both FE-I3 and FE-I4 is organized in double columns. In FE-I3 (see Figure 3) every pixel that is hit transfers its data through the double column bus to the end of column (EoC) which is outside the active region at the bottom of the chip. A hit pixel is blocked until the double column bus is free and the data has been stored in the EoC buffer. Simulations show that at $\sim$3x LHC luminosity the double column bus starts to saturate leading to a steep increase in hit losses up to an unacceptable level.

The FE-I4 architecture exploits the fact that 99.75% of the hits will not be triggered and therefore will not be transmitted off-chip. With the higher integration density the new technology offers, it is now possible to store all hits in local pixel buffers inside the double-column bus and to synchronize them by local logic to the trigger. As a consequence the double-column bus is now used only for the transmission of triggered hits and data traffic is drastically reduced. This has the side effect that power is saved because unnecessary digital activity is avoided.

Another new concept of the FE-I4 architecture is the sharing of timing information between several pixels which suits the clustered nature of real hits. In Figure 4, a possible architecture configuration is shown where two adjacent pixels lying one above the other are grouped together in one Regional Logic Unit (RLU) to share the same digital logic. In the same Figure two RLUs store their data locally in the same Local Buffer (LB) of a certain depth. Simulations show that this specific configuration with a Local Buffer depth of six cells at 2-3 times LHC luminosity and 3.7cm b-layer radius can cope with the expected hit rate with an acceptable level of inefficency (for more details see [5]).

Apart from abstract high level C++ simulations the different architecture options are investigated at Verilog Register Transfer Level (RTL), post synthesis and place & route gate level to estimate power consumption and required implementation space.

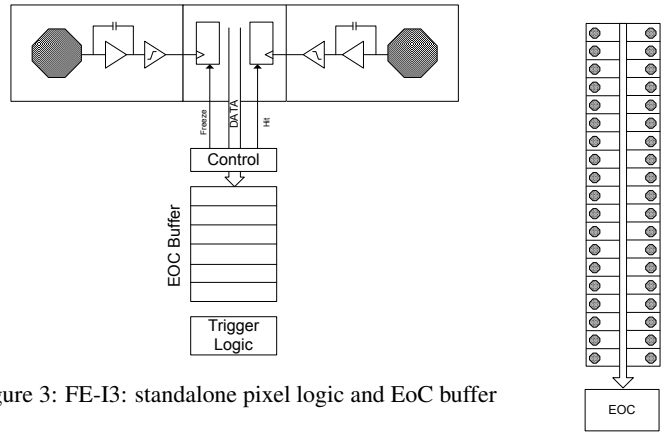

Figure 3: FE-I3: standalone pixel logic and EoC buffer

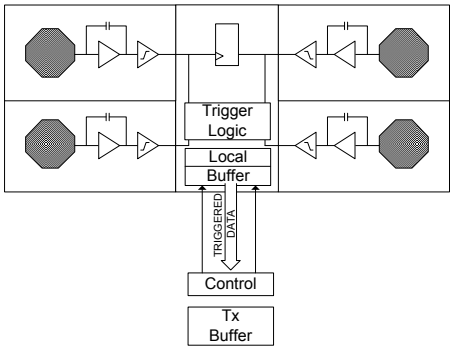

Figure 4: FE-I4: shared pixel logic and local buffer

IV. Peripheral Blocks

As a result of the technology change, the full peripheral chip infrastructure needed for the proper operation of the chip has to be redesigned as well, using radiation-hardening techniques. DACs and reference circuits are needed to bias and calibrate the chip. LVDS transmitters and receivers are used for fast off-chip communication. To improve the powering efficiency, a shunt type regulator for the serial powering approach, a divide-by-two charge pump DC-DC converter and a low drop out (LDO) regulator useful for both powering schemes have been implemented. Various latch designs for use in single event upset (SEU) tolerance studies [6] and a control block for command decoding have been developed . Some of the above mentioned blocks are covered in more detail in the next subsections.

A. LVDS circuits

As has been mentioned in section I, a data transmission rate of 160 Mb/s has been specified for the FE-I4. To have some margin and as a first step towards designing LVDS communication blocks for the needs at super-LHC, LVDS circuits have

been developed to reach a maximum clock rate of 320 MHz. The LVDS circuits have to operate in a supply voltage range of 1.2-1.5V so that the use of thick gate oxide transistors can be avoided and the amount of necessary supply rails is reduced.

As the supply voltage is reduced, these LVDS blocks do not use the usual IEEE LVDS 1.2V offset standard but a reduced offset to the half of the FE-I4 power supply. Note that FE-I4 type pseudo-LVDS driver is still able to communicate with commercial LVDS receivers as the standard stipulates a wide common-mode input voltage range at the receiver side [7], and the offset voltage of a commercial LVDS driver can be adapted to smaller values by added external circuitry so that driving a FE-I4 type pseudo-LVDS receiver for test purposes is also possible.

Regarding the LVDS driver, a standard architecture has been chosen and adapted to the smaller supply voltage range [8]. The output signal current is configurable in a range of 0.6-3.0mA. In a later iteration, a tristate output option has been added to the LVDS driver which might be beneficial for use in combination with a token pass method to multiplex the signal outputs of several FE-I4 chips through one transmission line at the outer pixel layers for SLHC.

In Figure 5, a simplified schematic of the LVDS driver with tristate option is shown. In a standard architecture transistors M3 and M5 or respectively M4 and M6 are connected to the same control signal because either the upper transistor switch is closed and the lower is open or vice versa. In the shown schematic, all switching transistors M3-M6 are steered by separate control signals. Hence it is possible to keep all switches open at the same time which gives a high impedance state at the output and decouples the LVDS driver from the transmission line. Additional logic is needed to control the state of the transistor switches with respect to the data and enable input signal.

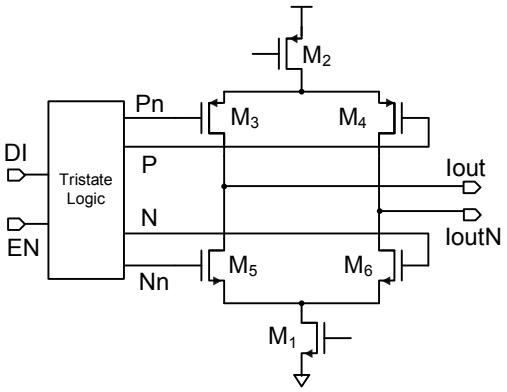

Figure 5: Simplified schematic of LVDS driver with tristate option

Because of the very low supply voltages, it is not possible to use conventional rail-to-rail input stages for the LVDS receiver. An approach with two completely independent comparator input stages has instead been chosen, one having an NMOS differential input pair that is covering high common-mode input voltages, the other having a PMOS differential input pair covering low common-mode input voltages [9]. The two signals paths are combined in a second stage and converted to a full-swing CMOS signal. Although this scheme fits better to the low supply voltage environment, the transistor threshold-voltages still have to be carefully chosen and fine-tuned to obtain rail-to-rail operation.

B. LDO regulator

The Low Drop Out (LDO) regulator is used to down convert an unregulated input voltage of 1.6V to a configurable output voltage in the range of 1.5-1.2V, providing a maximum load current of 500mA at a minimum drop out of 100mV. Line regulation, defined as the percentage of change of the regulator's output voltage relative to the change in input voltage is specified to be 0.3-0.4% for an input voltage ripple of 100mV whereas load regulation which is defined as the percentage of change in output voltage for a specific current load change has been specified to be 0.3-0.4% for a load variation of 150mA.

The implemented LDO shown in Figure 6 is composed of a wide PMOS power transistor, an error amplifier that senses the output voltage through a resistive divider and compares it with a reference voltage and additional circuitry that is employed to allow stable operation even with ceramic output capacitors with low equivalent series resistor (ESR).

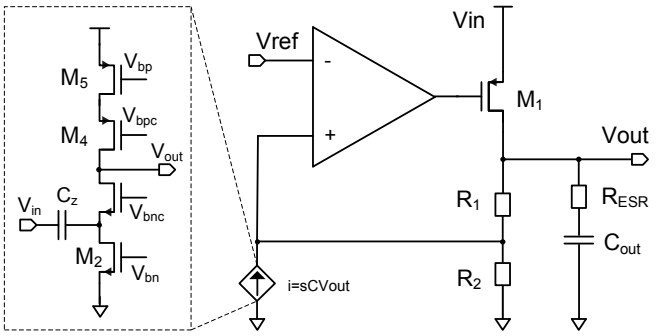

Figure 6: LDO with ESR and ZeroCell compensation

Calculations and simulations show that an error amplifier with a DC gain of about 60dB is sufficient to meet the regulation specifications. Therefore the error amplifier has been designed as an two-stage amplifier (Figure 7) avoiding poles located below the gain-bandwidth product (GBW) of the regulators open loop. For a symmetric slew-rate behavior a Class-AB output stage is required which has been realized by a fully-differential first stage combined with a common-mode feedback circuit (M6-M11). Conventional circuits use gate-drain connected transistors in the first stage (transistors M4 and M5 in Figure 7) but this lowers the output impedance and hence the gain of the first stage. Thus the proposed circuit implements a Class-AB output stage in an innovative and power efficient way.

LDO regulators are inherently unstable and therefore special attention has to be given to stabilization. Typically the ESR of the output capacitor is used to introduce a zero into the open loop transfer function which leads to compensation by pole-zero

cancellation [10]. Unfortunately a very small ESR is necessary for a good fast transient response of the LDO [11], which limits the frequency location of the introduced zero to high frequencies. Hence an alternative compensation method has been applied which allows the use of high quality low value ESR ceramic output capacitors.

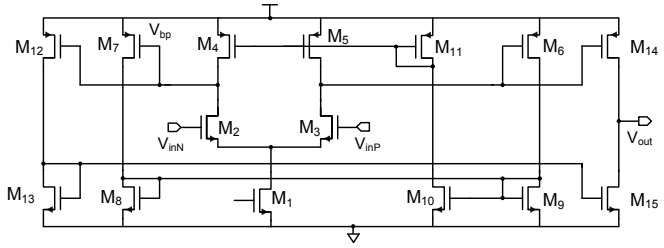

Figure 7: Error amplifier with Class-AB ouput stage

As shown in Figure 6, a frequency dependent voltage-controlled current source is used which is steered by the LDO output voltage and feeds its output current into the resistive divider [12]. At high load currents and small drop out voltages, the output impedance of the LDO regulator becomes very small. Combined with the fact that the material budget limits the maximum value of output capacitance, the LDO bandwidth has an untypically high value. As a result the compensation circuit implementing the frequency dependent voltage controlled current source has also to be high bandwidth.

The compensation circuit proposed in the literature [12] has a bandwidth restriction caused by nondominant poles related to the circuit's complexity. Hence a new compensation circuit (Figure 6 left) based on a transimpedance amplifier input stage has been developed. The output signal of the LDO is AC-coupled to the circuits input which gives a rising AC current flow with frequency. The introduced excess current is flowing out of the circuit into the resistive divider creating a zero in the open loop transfer function which can be used for the cancellation of the pole related to the error amplifier output impedance and the parasitic capacitances of the power transistor. The input impedance and the coupling capacitor define the bandwidth of the compensation circuit. For high frequencies, compensation is taken over by the small ESR of the output capacitor. Simulations show that the LDO regulator is stable in the whole region of operation having a phase margin above 60 degrees.

C. Divide by two charge pump DC-DC converter

A divide-by-two charge pump DC-DC converter has been prototyped to explore the viability of this option to reduce system current consumption, without the mass penalty of external DC-DC converters, deemed too great for pixel detectors [13]. The converter uses 4 switches to alternate an external "flying" capacitor between parallel and series connection to an external output capacitor. The circuit uses the 3.3V transistors of the process so that no special precautions are needed to accept input voltages of slightly more than twice the internal supplies (1.2V-1.5V). The main issue being addressed with this prototype is whether the 3.3V transistors maintain adequate performance after radiation damage. The transistors have been built with enclosed geometry and preliminary results of 200MRad proton irradiation are encouraging.

D. New shunt regulation concept (SHULDO)

In the serial powering approach, modules are placed in series and supplied with a constant current. The current flowing through the supply line is then reduced to the needs of a single module which decreases the cable losses and affords to reduce the cable material budget.

A shunt regulator is then required to generate a constant output voltage from the current supply. An approach followed with FE-I3 is to have a shunt regulator integrated in each FE chip, which are then placed in parallel at module level [14]. This scheme brings extra redundancy to the powering scheme, and a better load distribution on the module.

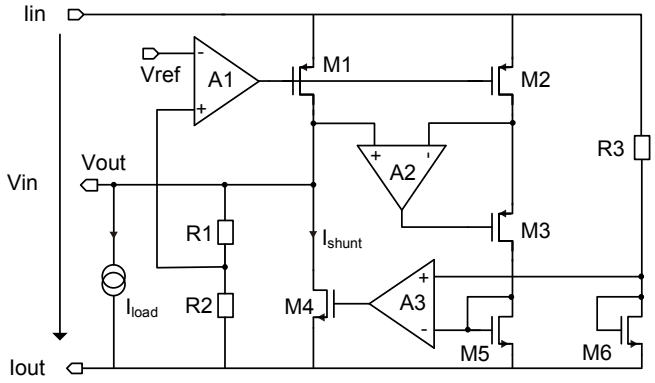

Figure 8: LDO with shunt capability (SHULDO)

Because of the very steep current to voltage characteristic, the parallel operation of shunt regulators is challenging. If one regulator is affected by mismatch or process variation and generates a smaller output voltage than the others, all module current is shunted through this single regulator at turn on which might lead to device break down. Therefore an additional "slope" resistor is placed at the current input of the shunt regulators which smooths out the current to voltage characteristic and helps distributing the shunt current between the regulators.

Although this additional slope resistor is needed for safe operation, it does not contribute to the regulation performance and consumes additional power. Hence a scheme where this constant resistor could be replaced by a regulated resistor of variable size would be very beneficial. The functionality of the PMOS power device used in LDO regulators is that of a regulated resistor. Therefore the regulator architecture shown in Figure 8 has been developed that combines a LDO type regulation scheme with the shunt capability known from shunt regulators.

The LDO part in Figure 8 is composed of the power transistor M1, the error amplifier A1 and the resistive divider R1 and R2 which is used to sense the output voltage. The LDO is responsible for the regulation of the output voltage Vout. To this

scheme an integrated shunt transistor M4 has been added that is steered to draw all the current that is not flowing through the load connected at the voltage output port of the regulator.

For the control of the shunt transistor, a fraction of the current flowing through the power transistor M1 is mirrored to transistor M2 and drained into the gate-drain connected transistor M5. The amplifier A2 and the cascode transistor M3 are added to improve the mirroring accuracy. Amplifier A3 compares the mirrored current to a reference current flowing into the gate-drain connected transistor M6 which is defined by the resistor R3 and the voltage drop Vin across the current input and output of the regulator. In this manner, a constant current flow through the regulator is assured which is either drawn by the load or shunted by transistor M4.

With the proposed regulation scheme a robust parallel operation of regulators generating completely different output voltages is possible without problems rising regarding the distribution of the shunt current. In Figure 9, simulation of the parallel operation of two regulators is shown, having an output voltage of 1.5V and 1.2V respectively. As can be seen in the lower part of the plot the currents flowing through the regulators are exactly the same.

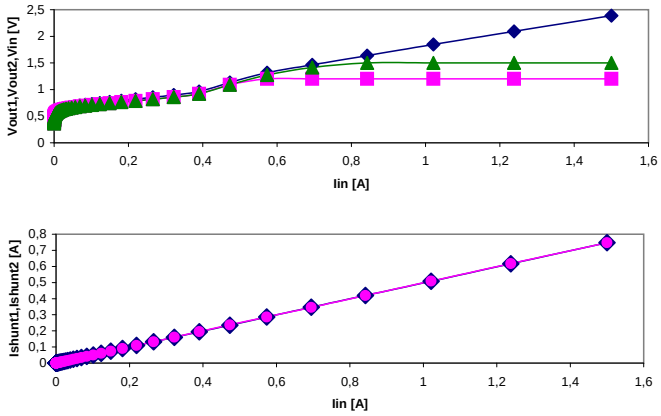

Figure 9: Parallel operation of two shunt LDOs

In reality mismatch of the integrated resistor R3 might lead to a shunt current variation of about 10% but this will not cause device break down. In addition, an on-chip resistor trimming mechanism can be applied or an external high-precision resistor can be used if necessary. As can be seen in Figure 9, the shunt current depends on the supply current which has the advantage that the regulator can cope with an abrupt increase in supply current which can happen if one FE-I4 chip does not contribute to the shunt current any more e.g. because of disconnected wire bonds. Finally this scheme is also very flexible. For use in a normal voltage based powering scheme, the shunt part of the regulator can be switched off and the regulator can be used as an ordinary LDO.

V. Conclusion

An overview of the ongoing development effort for the FE-I4 readout chip in 130 nm technology targeting ATLAS pixel b-layer upgrade and the outer layers at super-LHC has been given. Prototypes of the pixel analog array and some of the peripheral structures (DACs, current reference, LDO, LVDS circuits, command decoder, SEU-tolerant latches) are available and functional test as well as pre and post irradiation studies are under way. In parallel new concepts for the FE-I4 digital architecture are refined and investigated by parallel high level C++ modeling, RTL and backannotated gate level based timing simulations. The design of a full-scale FE-I4 IC is foreseen for the year 2009.

References

[1] ATLAS collaboration, The ATLAS Experiment at the CERN Large Hadron Collider, *JINST* 3 **S08003** (2008)

[2] ATLAS collaboration, Inner Tracker: Technical Design Report, 1, CERN-LHCC-97-016; Inner Tracker: Technical Design Report, 2, CERN-LHCC-97-017

[3] G. Aad *et al.*, ATLAS pixel detector electronics and sensors, *JINST* 3 **P07007** (2008)

[4] I. Peric *et al.*, The FE-I3 readout chip for the ATLAS pixel detector, *Nucl. Instrum. Methods Phys. Res.*, **A565** (2006)

[5] M. Barbero *et al.*, A New ATLAS Front-End IC for Upgraded LHC Luminosity, submitted to *Nucl. Instrum. Methods Phys. Res. A* August (2008)

[6] M. Menouni *et al.*, Design and measurements of SEU tolerant latches, submitted to TWEPP proceedings (2008)

[7] IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), 1596.3 SCI-LVDS Standard, *IEEE Std.* 1596.3-1996 (1994)

[8] A. Boni *et al.*, LVDS I/O interface for Gb/s-per-pin operation in 0.35-μm CMOS, *IEEE JSSC* VOL. 36 NO. 4 (2001)

[9] J. Tyhach *et al.*, A 90-nm FPGA I/O Buffer Design With 1.6-Gb/s Data Rate for Source-Synchronous System and 300-MHz Clock Rate for External Memory Interface, *IEEE JSSC* VOL. 40 NO. 9 (2005)

[10] G.A. Rincon-Mora *et al.*, A low-voltage, low quiescent current, low drop-out regulator, *IEEE JSSC* VOL. 33 NO.1 (1998)

[11] B.M. King, Understanding the load-transient response of LDOs, *Analog Applications Journal* Sept. (2000)

[12] C. K. Chava *et al.*, A frequency compensation scheme for LDO voltage regulators, *Trans. on Circ. & Syst.* VOL. 51 NO. 6 (2004)

[13] P. Denes *et al.*, A Capacitor Charge Pump DC-DC Converter for Physics Instrumentation, submitted to *IEEE Trans. Nucl. Sci.* (2008)

[14] D.B. Ta *et al.*, Serial powering: Proof of principle demonstration of a scheme for the operation of a large pixel detector at the LHC, *Nucl. Instrum. Methods Phys Res.* **A557** (2006)