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Development of FE-I4 pixel readout IC

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A new hybrid pixel readout integrated circuit denominated FE-I4 is being developed for use in ATLAS upgrades. The design goals include 4 times higher rate capability, 4 times the active area (full reticule), and 38% smaller pixels than the presently used FE-I3 IC. The target applications are a possible smaller radius replacement of the present inner layer and/or outer layers or disks of a super-LHC detector. For the innermost layer of a super-LHC detector a further design generation will be needed, and the present effort serves as a stepping stone towards this ultimate goal. Small size analog/digital prototype blocks have been fabricated in 0.13um feature size bulk CMOS technology. An overview of the full chip design-in-progress is presented, along with status and test results from various test chip prototypes.

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