Custom DC-DC converters for distributing power in SLHC trackers

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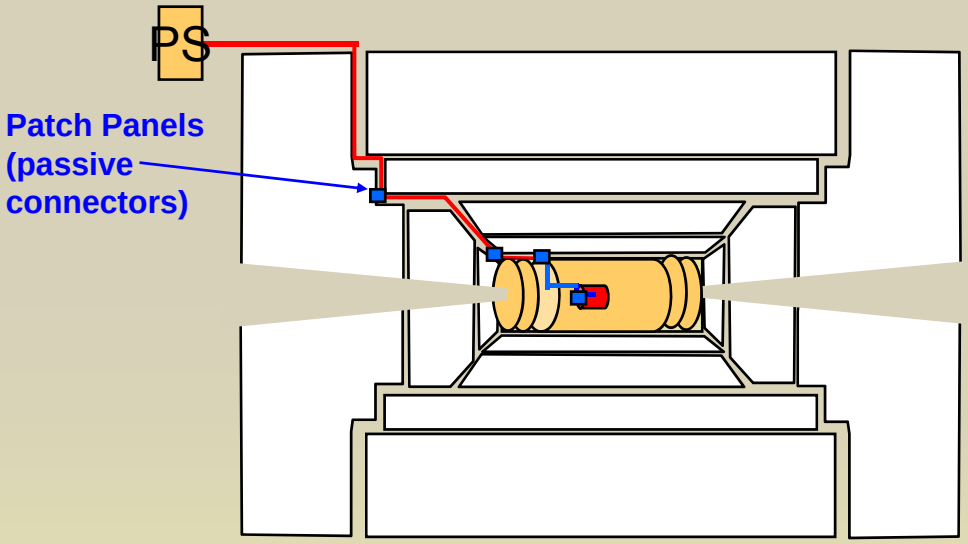
Outline

- Power distribution in the trackers
  - In LHC trackers and projection to SLHC
- DC-DC converters based solution
  - Power losses on cables
  - Main challenges in HEP experiments
- Proposed power distribution scheme
- Implementation
  - Different converter topologies
  - 1st stage
  - 2nd stage
- Conclusions

Distributing power in LHC-SLHC

Typical low-voltage power distribution in LHC trackers:

No on-detector conversion. Low-voltage (2.5-5V) required by electronics provided directly from off-detector. Sense wire necessary for PS to provide correct voltage to electronics. Cables get thinner when approaching the collision point (strict material budget).



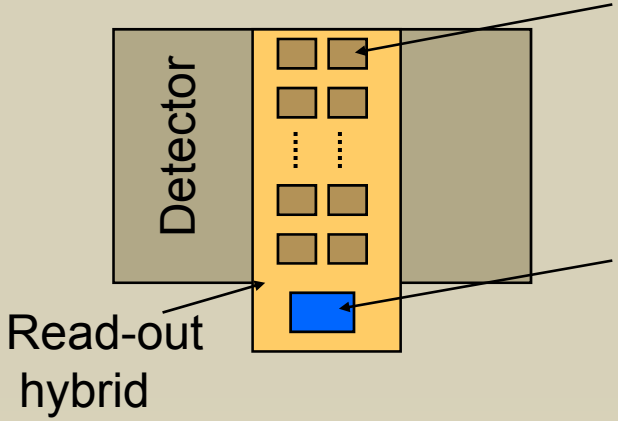
In view of SLHC:

-Scheme not easily scalable to the larger currents expected (see next slides)

What needs to be powered? (1)

All ASICs will be manufactured in an advanced CMOS (or BiCMOS) process, 130nm generation or below. Here we consider only CMOS ASICs.

Detector module



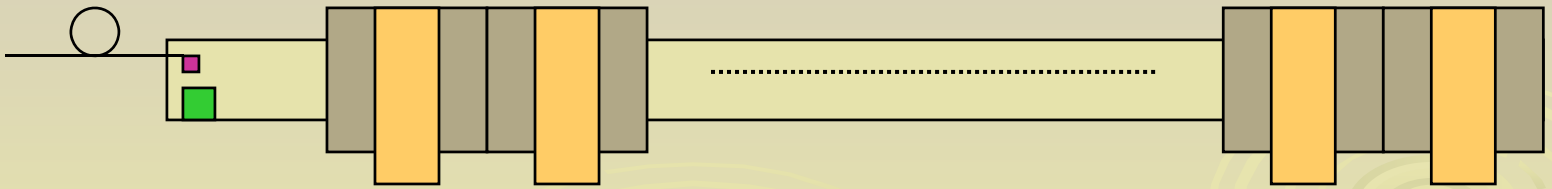
Front-End readout ASIC

- $I_{digital} \geq I_{analog}$ (for instance, current projection for ATLAS Short Strip readout is I_{analog} ~ 20mA, $I_{digital}$ ~ 60-100mA)
- 2 power domains: V_{an}=1.2V, V_{dig}=0.9-0.8V (as low as possible)
- Clock gating might be used => switching load

Hybrid/Module controller

- Ensures communication (data, timing, trigger, possibly DCS)
- Digital functions only
- It might require I/Os at 2.5V

Rod/stave



Other than the **rod/stave controller**, **optoelectronics components** will also have to be used, requiring an additional power domain (2.5-3V)

What needs to be powered? (2)

Summary

- 3 Voltages to be provided to minimize power consumption:
  - 2.5V for optoelectronics and (maybe) control/communication ASICs
  - 1.2V for analog circuitry in FE ASICs
  - 0.8-0.9V for digital circuitry in FE ASICs. This domain uses most of the current!
- Digital current might be switching in time (to really minimize the power)

Power and Current in LHC/SLHC

- Projection based on current estimate for ATLAS upgrade
- Only accounting barrel detector, power from Readout ASICs only
- SCT is LHC ATLAS Silicon Tracker detector, to be replaced (grossly) by Short Strip layers in present upgrade layout (strawman design)

	N of layers	Min and Max R (cm)	Barrel length (cm)	N of chips	N of hybrids	Active power (KW)	Load current (KA)
SCT barrel	4	30, 51	153	25,000	2100	11.6	2.75 (@3.5-4V)
SLHC SS layers, barrel	3	38, 60	200	173,000	8600	16.2 (@0.9-1.2V) 20.3 (@1.2V)	17.2 (@0.9-1.2V)

Large waste of power if $V_{an}=V_{dig}=1.2V$

Large current increase (Power on cables = RI^2)

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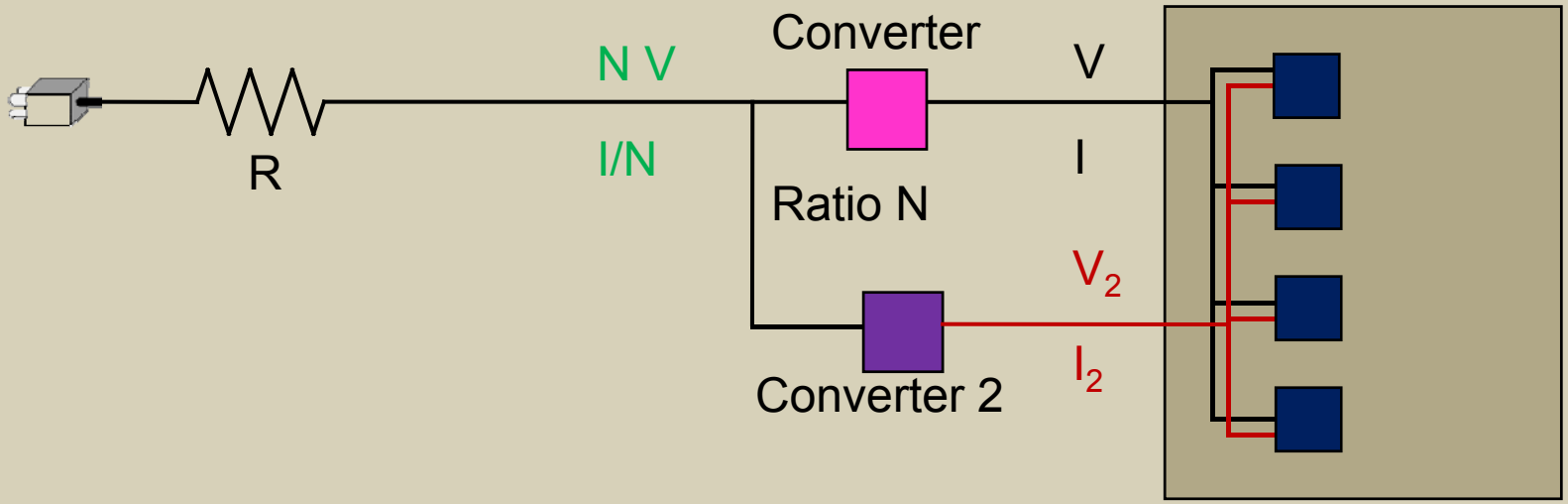
Reduction of cables power losses



Solution without converter: ↓ Power losses on cable = RI^2

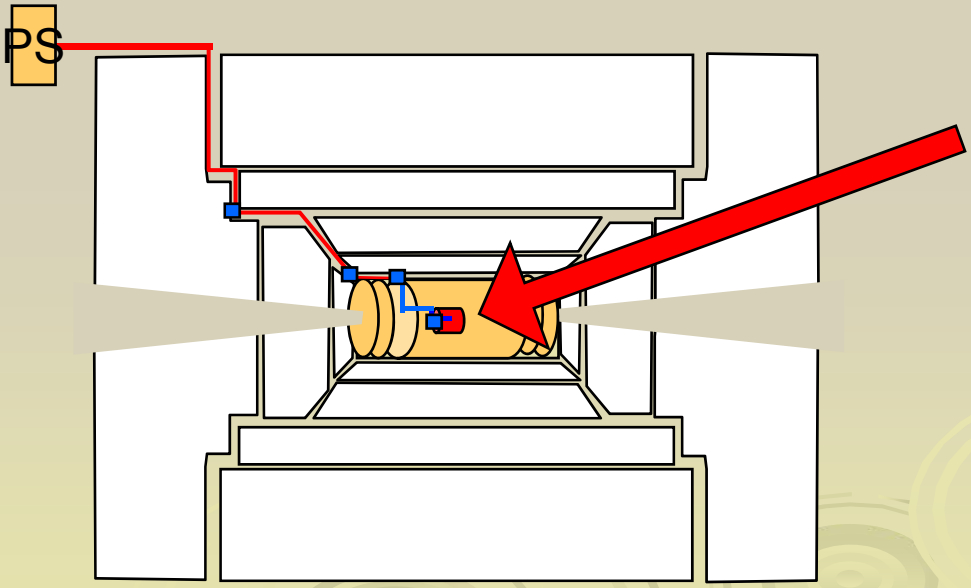
Solution with converter: ↑ Power losses on cable = $R\left(\frac{I}{N}\right)^2 = \frac{RI^2}{N^2}$

Custom converter for SLHC

- The converters will be placed inside the tracker, therefore they will be embedded in
  - **radiation** (>100Mrd)
  - **magnetic** (2T-4T) fields

- Commercial converters do not target this environment because they are not radiation tolerant and use ferromagnetic material that saturate at this external magnetic field.

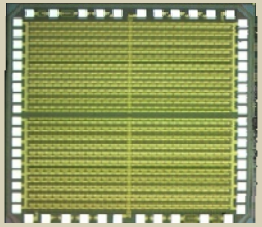
- It is therefore necessary to develop custom converters that meet the HEP requirements

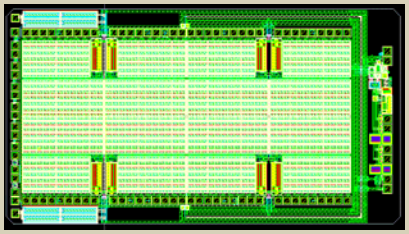


Tolerance to experiment environment

- **Radiation tolerance**

  the converter requires the use of a technology able to work up to at least 15-20V. This high voltage technology are typically tailored for automotive applications. More information on the talk during the power working group meeting.





- **Magnetic field tolerance**

  We are obliged to use coreless (air-core) inductors because all the ferromagnetic material are not usable with an external magnetic field of 2-4T and at a switching frequency of 1Mhz

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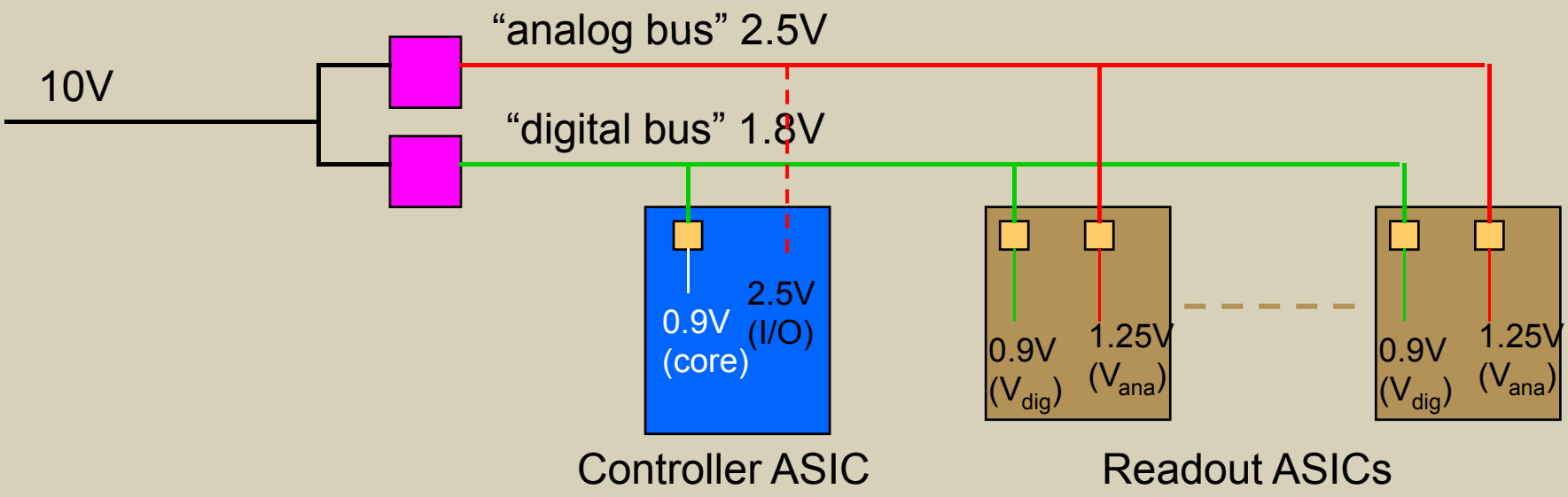
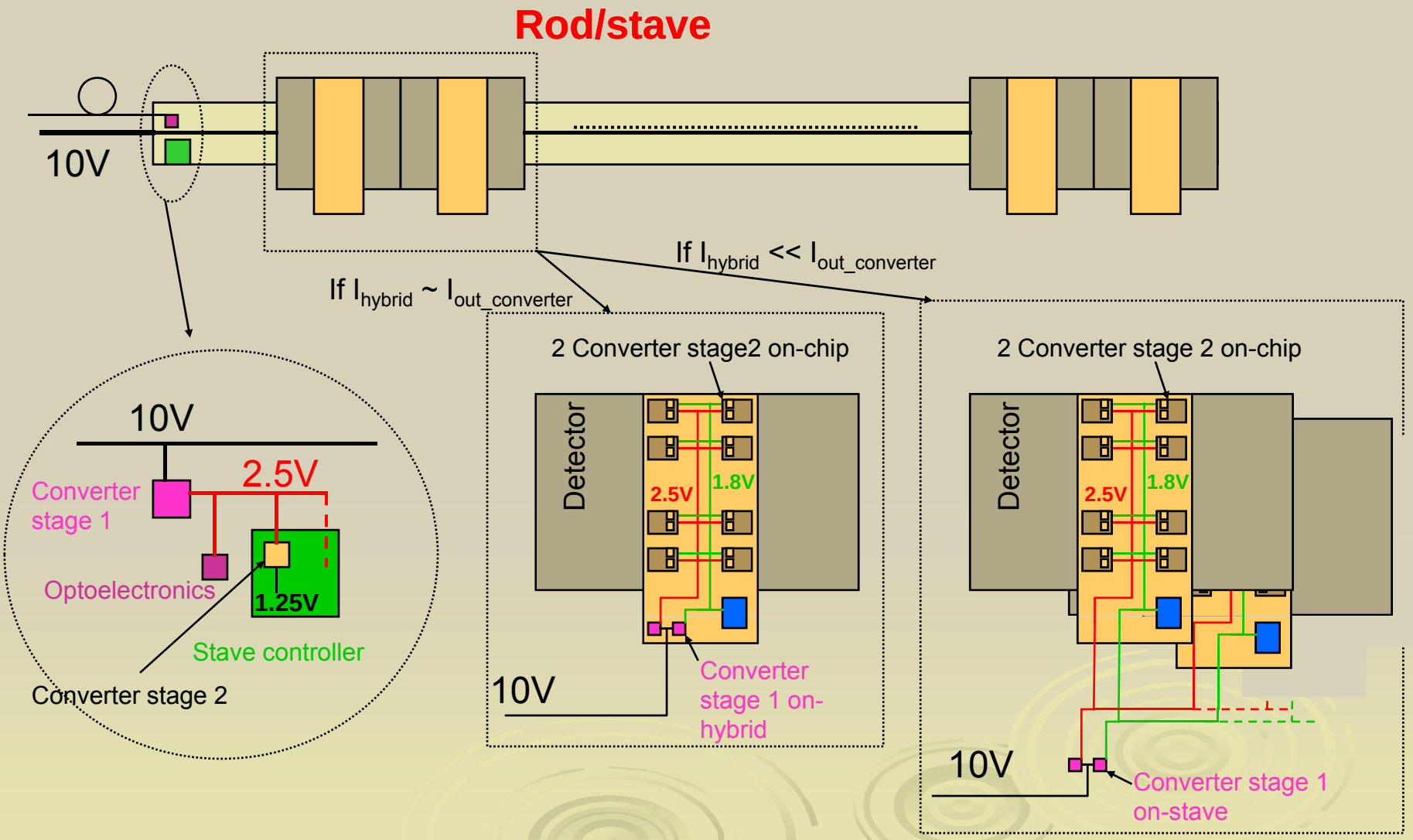
Proposed power distribution scheme



Conversion stage 1 (ratio 4-5.5)
-Vin=10V => high-V technology
-Same ASIC development for analog and digital, only feedback resistive bridge is different

Conversion stage 2 (ratio 2)
- Embedded in controller or readout ASIC
- Closely same converter for analog and digital (different current, hence different size of switching transistors): macros (IP blocks) in same technology

Implementation example



Summarizing proposed scheme

- **Components needed:**
  - ASIC for conversion stage 1 (10V in, hence “high-V” technology)
  - ASIC macro (IP) for conversion stage 2 (in the FE ASIC technology)
  - Air-core inductor(s)
  - SMD Capacitances
- **Features**
  - Conversion ratio close to 10 allows for considerably decreasing power loss on cables
  - Only 1 power line (10V) from off-detector, all other voltages generated locally
  - Capability to power both analog and digital domains with required voltage to minimize power – even in the event of switching loads
    - Only inefficiency due to conversion losses
  - High modularity
    - On-chip conversion stage allows in principle each ASIC to be turned on/off independently (power groups can also be envisaged):
      - Controller ASICs can be turned on first and alone – easy start-up condition
      - Depending on the modularity, defective FE ASICs (or groups) can be turned off to prevent the rest of the hybrid to be affected

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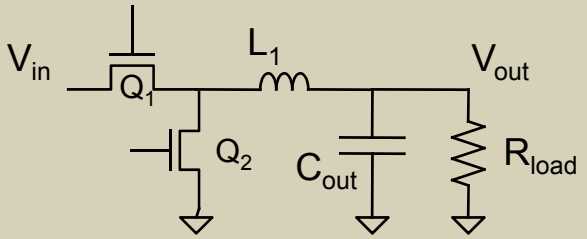
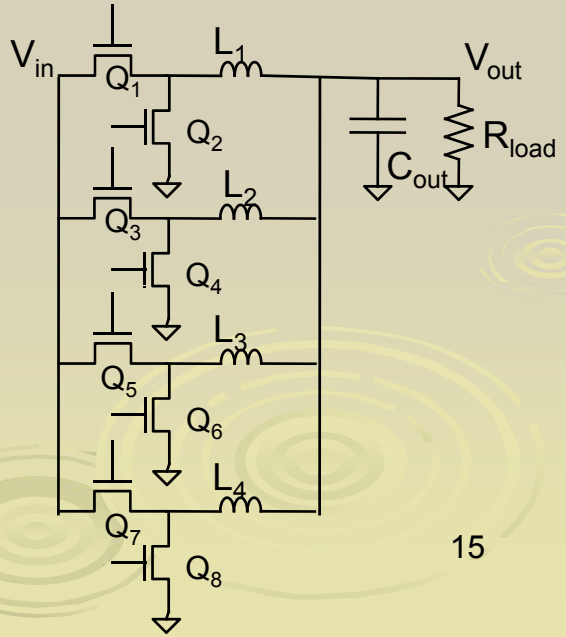
Different converter topologies (1/3)

The following DC/DC step down converter topologies have been evaluated and compared in view of our specific application.

1. **Single phase synchronous buck converter**
   - ↑ Simple, small number of passive components
   - ↓ Larger output ripple for same C_{out}
   - ↓ RMS current limitation for inductor are output capacitance

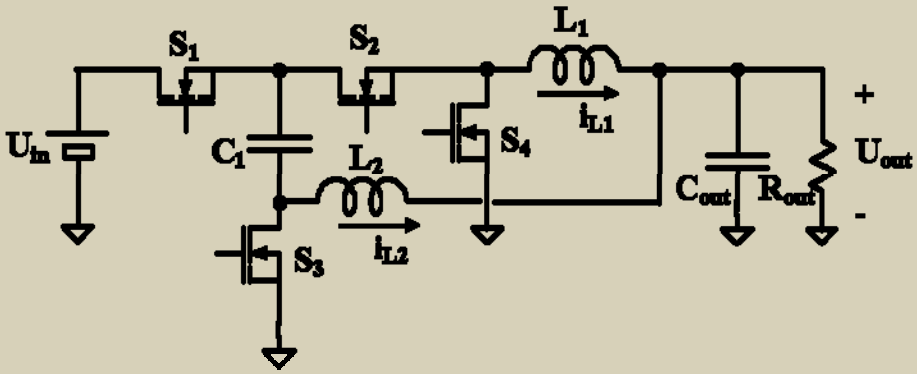


2. **4 phase interleaved synchronous buck converter**
   - ↑ Complete cancellation of output ripple for a conversion ratio of 4 (with small C_{out})
   - ↑ Smaller current in each inductor (compatible with available commercial inductors)
   - ↓ Large number of passive components
   - ↓ More complex control circuitry

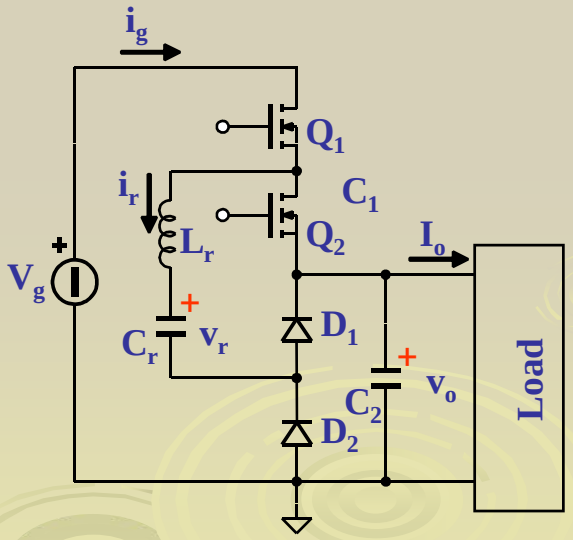


Different converter topologies (2/3)

3. **Two phase interleaved synchronous buck converter with integral voltage divider**
   - ↑ Complete cancellation of output ripple for a conversion ration of 4 (with small C_{out})
   - ↑ Simpler control and smaller number of passive components than 4 phase interleaved

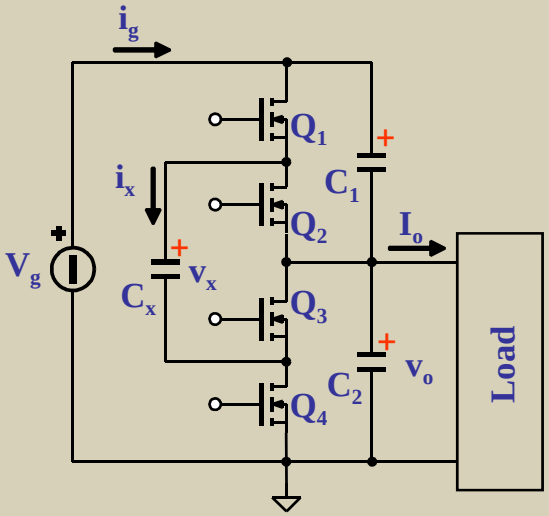


4. **Multi-resonant buck converter**
   - ↑ Very small switching losses (zero voltage and zero current switching)
   - ↓ To achieve resonance:
     - Current waveforms have high RMS value => large conductive losses => lower efficiency
     - Voltage waveforms have high peaks, possibly stressing the technology beyond max Vdd
   - ↓ Different loads require complete re-tuning of converter parameters



Different converter topologies (3/3)

5. **switched capacitor voltage divider**
   - ↑ rather simple, limited number of passive components
   - ↑ lack of inductor => good for radiated noise and for compact design
   - ↓ No regulation of the output voltage, only integer division of the input voltage
   - ↓ Efficiency decreases with conversion ratio (larger number of switches)
   - ↑ Good solution for ratio = 2, for which high efficiency can be achieved



Conversion stage 1: topology

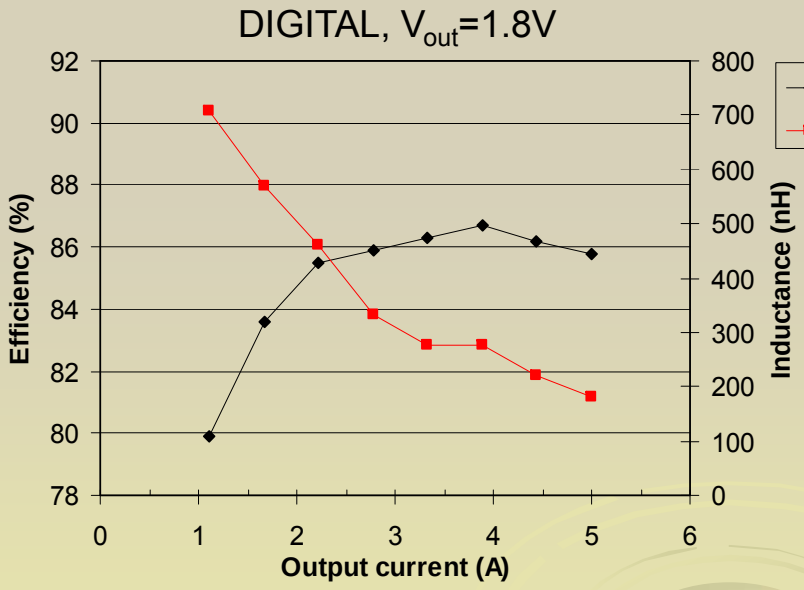
Waveforms of the different topologies have been computed with Mathcad, and conversion losses have been estimated for each of them in the same conditions:
V_{in}= 10V, P_{out}= 6W, V_{out}= 2.5V (step down ratio = 4), use of AMS 0.18um technology with approximate formula to account for switching losses

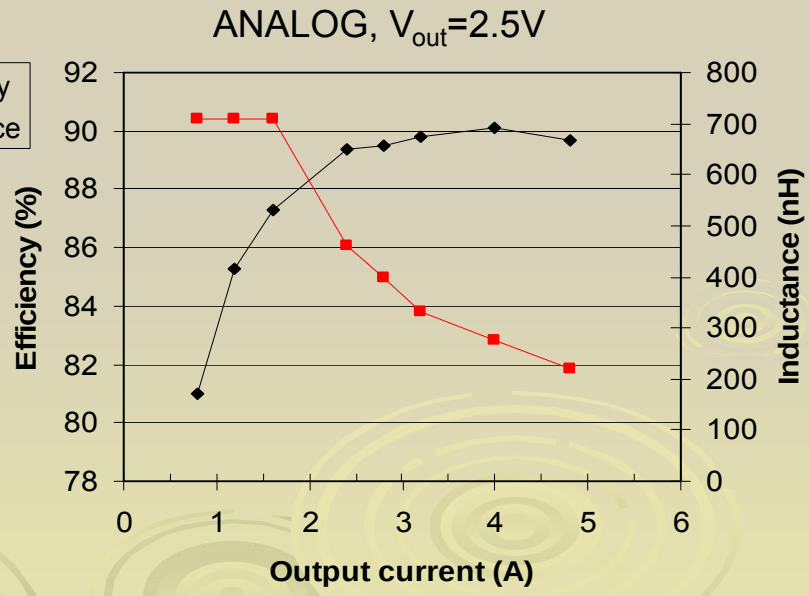
Topologies	Efficiency	Components needed		
		Number of Switches	Number of Capacitors	Number of Inductors
Buck converter	86	2	2	1
4 phase Interleaved Buck	88.3	8	2	4
2 phase Interleaved Buck + VD	89.7	4	3	2
Multiresonant Buck	82.5	1	4	2
2 Cascaded Switched Capacitor	87.3	8	7	0

The best compromise in terms of efficiency, number of components required, complexity and output ripple is the 2 phase interleaved buck with integrated voltage divider.

Implementation: conversion stage 1

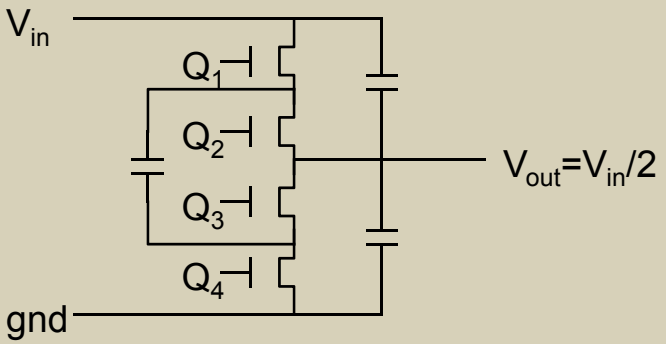
- The final result of our study is that, for the development of a unique ASIC conversion stage 1 for both analog and digital power distribution, the best solution is:
  - 2-phase interleaved buck with integrated voltage divider
  - Switching frequency = 1 MHz
  - On-resistance of switching transistors = 30 mΩ
- The inductor can be chosen for the specific output current wished in the application, achieving the efficiency estimated in the graphs below for the AMS 0.18 technology (Coilcraft RF 132 series inductors are used)



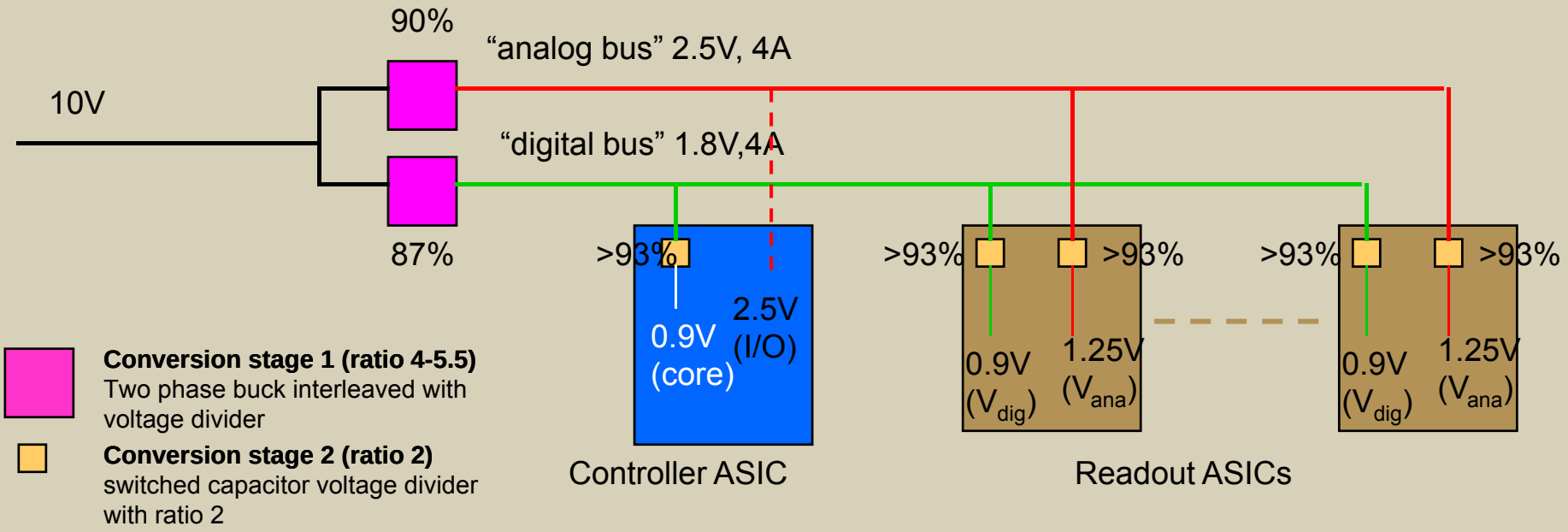


Implementation: conversion stage 2

- Two converters to be embedded on each chip
  - Output current rather modest (20-200 mA)
  - Inductor-based converters not envisageable:
    - With on-chip inductors (high ESR) the efficiency would be extremely low
    - The use of several discrete inductors per ASIC is not desirable – already only for system integration purposes
  - Switched capacitor converters more suitable
    - Acting as voltage divider (÷2)
    - They unfortunately do not provide regulation, which must be relied on from conversion stage 1
    - Achievable efficiency has been estimated, then refined with a quick simulation in a 130nm technology (use of I/O transistors)
      - Efficiency (Vin=1.8V, Vout=0.9V, Iload=166mA, f=20MHz) = **93%**
      - It should be pointed out that no study on the optimization of this converter has been made – one only topology, with one fixed frequency has been studied (efficiency can be improved further by decreasing the frequency, for instance).



Efficiency of the two stages



The efficiency of the two stages is equal to the multiplication of the efficiency of each stage:

- Analog: 90%*93%=84%
- Digital: 87%*93%=81%

Projection for total power

Projection to SLHC ATLAS SS tracker

- Comparison of SCT (present ATLAS strip tracker) and Short Strip strawman design for SLHC
- Power loss in cables only for last Patch-Panel – at the edge of the tracker, in the hypothesis of 1Ω resistance on the return path per cable
- For DC-DC conversion, we assume 10V input voltage to the stave/rod

	N of modules	N of power cables	Active power (KW)	Load current (KA)	Power loss in cables (KW)	Total power in detector (KW)
SCT barrel	2100	2100	11.6	2.75	3.6	15.2
SLHC SS layers, barrel	8600			17.2		
Parallel powering	"	8600	16.2 (@0.9-1.2V)	"	34.4	50.6
DC-DC converters (80% efficiency)	"	2000	16.2 (@0.9-1.2V)	"	1	21.2
		1000	"		4	25.2

Conclusions

Summary

- We presented a DC-DC based power distribution architecture that:
  - Provides different on-module voltage level. This allows a minimization of the active power
  - local voltage regulation and capability of switching on/off independently each FE-chip or groups of FE-chips
  - reduction of on-cable power losses
- DC-DC converter topologies are being selected:
  - Two phase interleaved with voltage divider or simple buck for the first stage
  - Switched capacitor with ratio 2 for the second stage

Working plan

- Radiation tolerance studies on different technologies
- Design of a prototype of the converter with the selected topology for stage 1:
  - with discrete components
  - in the AMIS technology
- Further studies on noise coupling will be carried out.

More information

Other aspects very relevant for a successful implementation can be found on:

- **Noise**
  - **measurement**

    Noise Susceptibility Measurements of F-E Electronics Systems (indico link)

    on the talk of G. Blanchot this afternoon at 15:55
  - **characterization**

    Characterization of the noise properties of DC to DC converters (indico link)

    during the poster session
- **Progress on prototypes**

  Progress on DC/DC Converters Prototypes (indico link)

  talk during the power working group
- **Radiation test results**

  Radiation measurement on AMIS 0.35 technology (indico link)

  talk during the power working group
- **First prototype**

  A prototype ASIC buck converter for LHC upgrades (indico link)

  during the poster session

DC/DC Converter basics

A power converter comprises at least

- two switch devices

  They need to have low resistance

- a control system

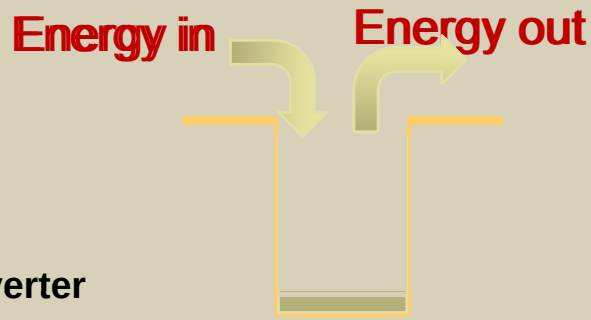
  It needs to provide switching signals and

  (if regulation is present) stabilize the output voltage

- an energy storage device

  it can be implemented in different ways:

Technology must be radiation tolerant

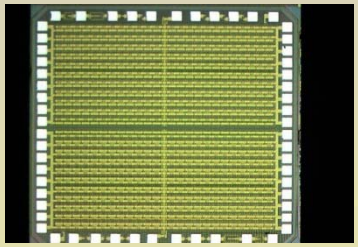


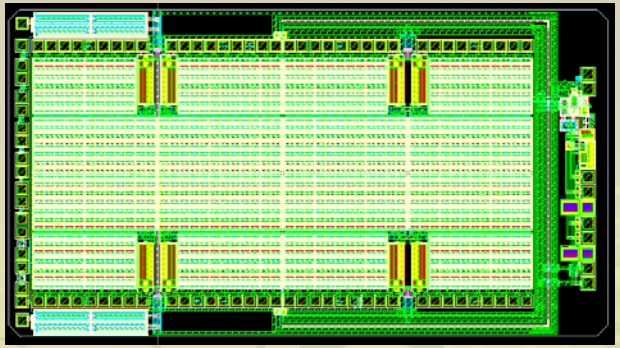
- Magnetic components ⇒ **Inductor based converter**
  - By far the most commonly used type of converter

    Inductor must be tolerant to experiment's high magnetic field
- Capacitive components ⇒ **Switched capacitors converters**
  - Mostly used to step-up the voltage (charge pumps), but step-down solutions are also found

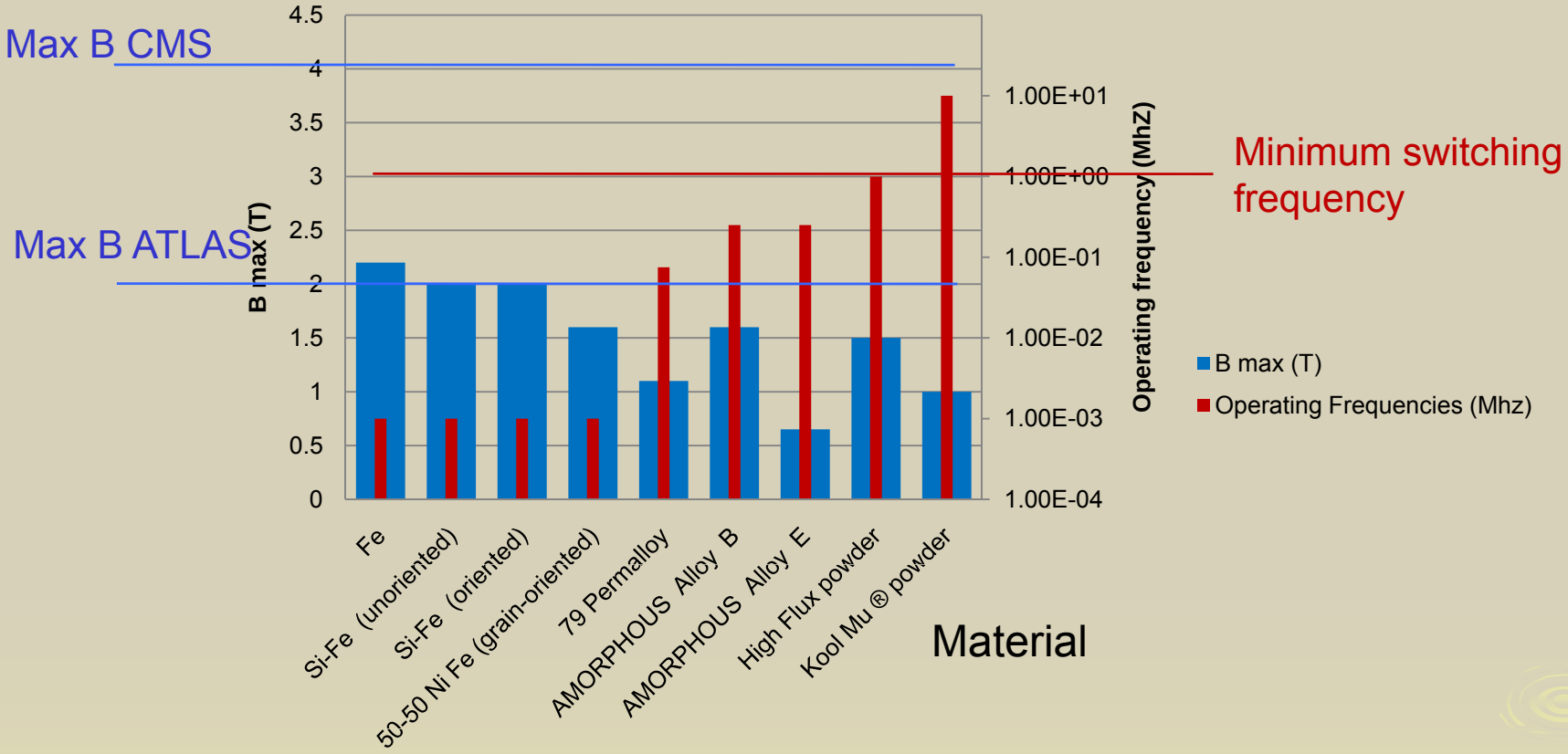
Radiation tolerance

- For our purposes, the converter requires the use of a technology able to work up to at least 15-20V
  - Such technology is very different from the advanced low-voltage (1-2.5V) CMOS processes used for readout and control electronics, for which we know well the radiation performance and how to improve it
- High-voltage technologies are typically tailored for automotive applications
  - Need to survey the market and develop radiation-tolerant design techniques enabling the converter to survive the SLHC radiation environment (> 10Mrd)
  - Extensive tests carried on the AMIS I3T80 technology. Results will be presented at the Working Group meeting. This technology is used in the first prototyping phase.
  - More advanced technologies are getting accessible and will be studied (AMS 0.18, STM 0.18 and 0.13)





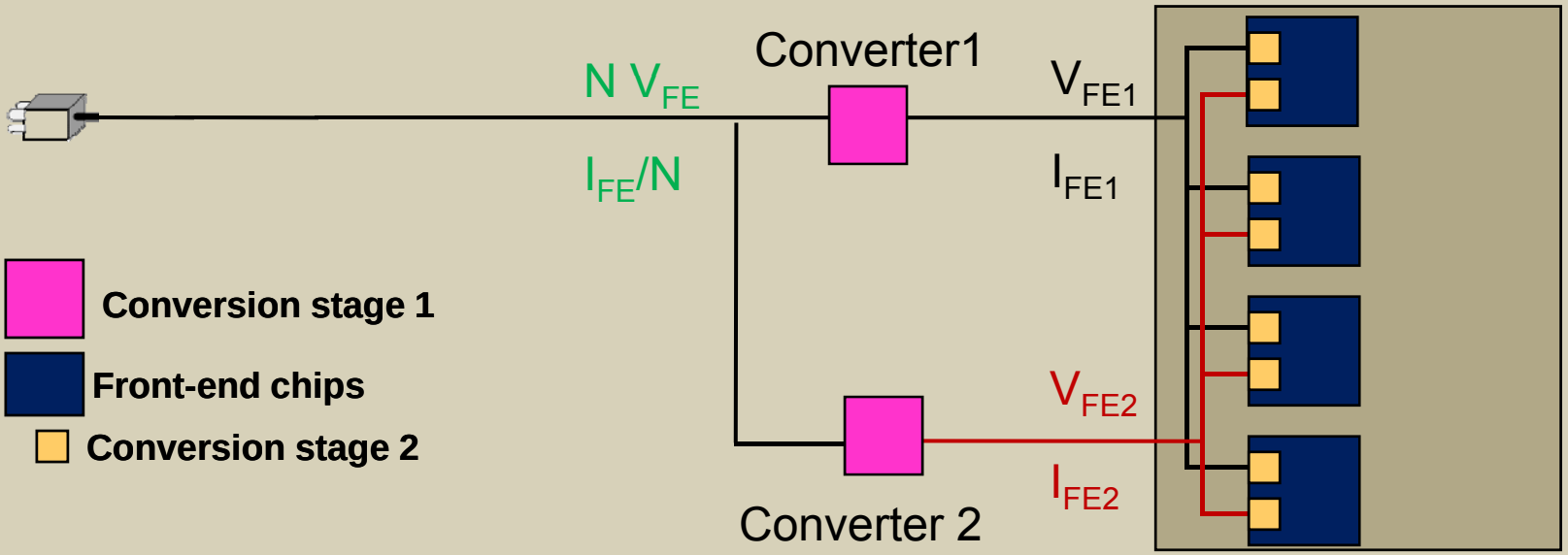
Magnetic field tolerance



We are obliged to use coreless (air-core) inductors

- This has a big impact on the available inductance magnitude, hence on the design of the converter
- Air-core inductors can be manufactured in different configurations (planar, solenoidal, thoroidal, ….) and a choice should be made

How many conversion stages



One conversion stage:

- ↑ Only one component (lower complexity and development cost)
- ↓ The converter has to provide all the current => problems in case of high currents
- ↓ Power distribution on module can be difficult

Two conversion stages:

- ↑ Less current in both first and second stages
- ↑ Possibility to switch off only parts of the load
- ↓ Several converters are needed

Conversion stage 1: frequency

- For the chosen topology, more accurate calculations in different technologies (AMIS 0.35, AMS 0.18) have been carried out. This time switching losses have been estimated with dedicated simulation runs.
- Best results obtained with AMS 0.18 => all following calculations refer to this technology
- Quasi-Square-Wave (QSW) operation, where inductor current goes slightly negative at each cycle, turned out to be give higher efficiency in all cases (all switching but one are done in either zero-voltage or zero-current conditions)
- Note that Inductor value changes at each frequency and load condition to keep QSW operation. Inductor parameters taken from Coilcraft RF 132 Series
- For both "analog" (V_{out}= 2.5V) and "digital" (V_{out}= 1.8V) conversion stages, the highest efficiency is found for a working frequency of 1MHz. The curves below are for P_{out}= 6W.