Custom DC-DC converters for distributing power in SLHC trackers

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Abstract

A power distribution scheme based on the use of on-board DC-DC converters is proposed to efficiently distribute power to the on-detector electronics of SLHC trackers. A comparative analysis of different promising converter topologies is presented, leading to the choice of a magnetic-based buck converter as a first conversion stage followed by an on-chip switched capacitors converter. An overall efficiency above 80% is estimated for the practical implementation proposed.

I. SLHC POWER DISTRIBUTION NEEDS

In the design of upgraded trackers for SLHC, the required increase in the number of readout channels should not lead to a heavier tracker. Since cables and cooling are amongst the main contributors to the material budget, and they are both dependent on the amount of power burnt in the tracker, on-detector power management is necessary. It is important to both decreasing the power per function ratio of Front-End (FE) electronics, and to distributing the power efficiently.

The first objective can be reached in a straightforward manner by decreasing the voltage supply. This is not possible for the analog readout circuitry, whose design will already be challenging in the low-voltage CMOS processes in the 130nm node or below (typical maximum V_{dd} around 1.2V). On the contrary, the supply voltage of the digital circuitry can be sensibly decreased below 1.2V, since standard cells in these advanced technologies are capable to run – at nominal V_{dd} – much faster than the 40-160MHz required for the FE ASICs.

The above considerations lead to separate analog and digital power domains to be provided to SLHC tracker's staves[1]. In fact an additional domain will be needed, because optoelectronics components at the end(s) of the stave will require a voltage of at least 2.5V. The 2.5V will possibly be needed also by the stave and hybrid controller ASICs, in particular for the Input/Output (I/O) circuitry. The presence of 2 voltages on-chip, 2.5V for the I/O and 1.2V (or less) for the core, is a normal feature of advanced commercial digital circuits, and is commonly supported by CMOS technologies.

The number of power domains is not sufficient to draw a specification for the power distribution system without an estimate of the required current. Although the design of FE readout circuits for SLHC trackers is still in a very preliminary phase, a projection based on available estimates can be very useful. The following projection refers to the ATLAS tracker, for which a strawman design [1] and estimates for both analog [2] and digital [3] power consumptions exist. In Table 1, the projected needs for a portion of the tracker, the Short Strips barrel detector, is compared to the barrel SCT detector which is currently installed at comparable radius. In the table, we call "active power" the total power actually consumed by the electronics. The basic assumptions for the projection are:

- Current for the analog readout circuit: 130µA/channel
- Total current for the on-chip digital circuitry: 80mA
- 128 channels in each FE ASIC
- 20 FE ASICs per hybrid
- Only FE readout ASICs are considered.

There are two fundamental concepts emerging from the comparison of the two systems. First, the current to be provided to the load increases by a factor of 6. Since the power lost in a cable is proportional to the square of the current, this implies a 36-fold increase in losses if the power distribution system remains the same as today. Second, a large amount of power is wasted (about 4kW out of 16kW, or 25%) if the distribution system is unable to provide different voltage domains for analog and digital circuitry, and the whole of every FE ASIC is biased at 1.2V. It clearly appears that, to be efficient, the new distribution system has to achieve a large decrease of the current in the cables from the power supplies (off-detector) to the hybrids, and has to support the distribution of different voltage domains.

Table 1: Comparison of the power requirements for the current ATLAS SCT barrel tracker and the Short Strip barrel layers of the SLHC ATLAS tracker in the present strawman design. For the SLHC two scenarios are compared: identical (1.2V) or different voltage distributed to analog and digital circuitry in the FE ASICs.

	SCT barrel	SLHC SS barrel
N of layers	4	3
Min and max R [cm]	30, 51	38, 60
Barrel length [cm]	153	200
N of FE ASICs	25000	173000
N of readout hybrids	2100	8600
Active power [kW]	11.6	16.2 (1.2 & 0.9V) 20.3 (1.2V only)
Load current [kA]	2.75	17.2

[1] We call stave a tracker detector assembly of several modules, each module being a silicon strip detector read-out by 1 or 2 hybrids. Each hybrid contains several FE ASICs and a controller ASIC.

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II. Distributing power with DC-DC converters

In commercial applications such as computing and networking, power is typically distributed using AC-DC and DC-DC converters [4]. A first AC-DC converter takes power from the mains and produces a regulated and filtered main bus voltage, which is distributed to a number of DC-DC Intermediate Bus Converters (IBC). Each of them supplies a power domain with an Intermediate Bus Voltage, where Point of Load converters take power to provide the loads with a regulated voltage. The low voltage required by the load is hence produced close to it, the required power being distributed at higher voltage (P=V·I).

A similar but simpler scheme could be used to distribute power in SLHC trackers, since on-stave and/or on-hybrid voltage conversion would indeed enable the desired reduction in current along the cables connecting the power supplies to the stave/hybrid. Such scheme is also capable of locally providing different voltage levels through the integration of different converters on the hybrid. This principle is shown schematically in Figure 1, where 2 step-down converter stages (thus named because $V_{out}<V_{in}$) are used. First, a conversion stage 1 on stave or hybrid provides two intermediate bus voltages: an "analog" 2.5V and a "digital" 1.8V. These buses locally run across one hybrid or a few neighbour hybrids. A second conversion stage, integrated on-chip, acts as a divider by 2 to supply the required voltage to the analog and digital circuitry on both the controller and readout ASICs. The overall conversion ratio achieved is closed to 10, for a comparable decrease in the current on the 10V line coming from the off-detector power supplies.

A possible implementation of this scheme is shown in Figure 2, where a full stave is powered via a unique 10V line (the other line at the left of the stave is the optical link for communication purposes). At the left of the stave, one converter (stage 1) supplies 2.5V to the optoelectronics and the stave controller, where the required core voltage of 1.2V is generated on-chip by a conversion stage 2. In both Figure 1 and 2 the intermediate bus voltage is ideally divided by 2 on-chip, hence producing a 1.25V analog voltage, whilst in reality unavoidable losses will decrease it a little below this nominal value, making it closer to 1.2V. The same applies for the digital line.

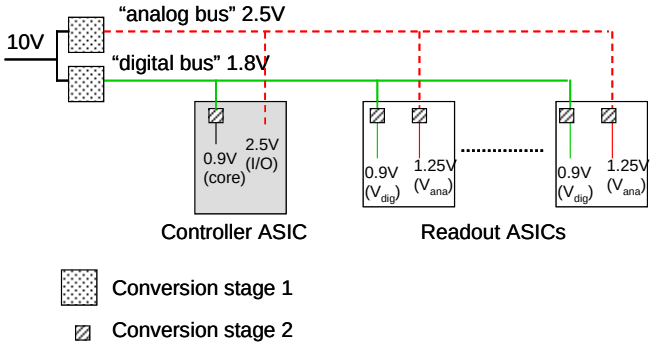

Figure 1: Power distribution scheme providing multiple voltage domains to the controller and readout ASICs from a single 10V line.

The main features of this implementation can be summarized as follows:

– Different voltage domains are generated locally from a unique 10V line. FE analog and digital circuitry can be efficiently powered at the required V_{dd}
– The current along the 10V line is decreased by a ratio of about 10 with respect to the load current. Power losses on this line are minimized ($P= R·I^2$)
– Load current does not need to be constant in time. This is compatible with the presence of switching loads (for instance, for clock gating)
– High modularity in the distribution of power allows for individual or grouped turning on/off of ASICs, greatly facilitating system start-up. In case of FE ASIC failures, only individual groups can be turned off without loosing full hybrids.

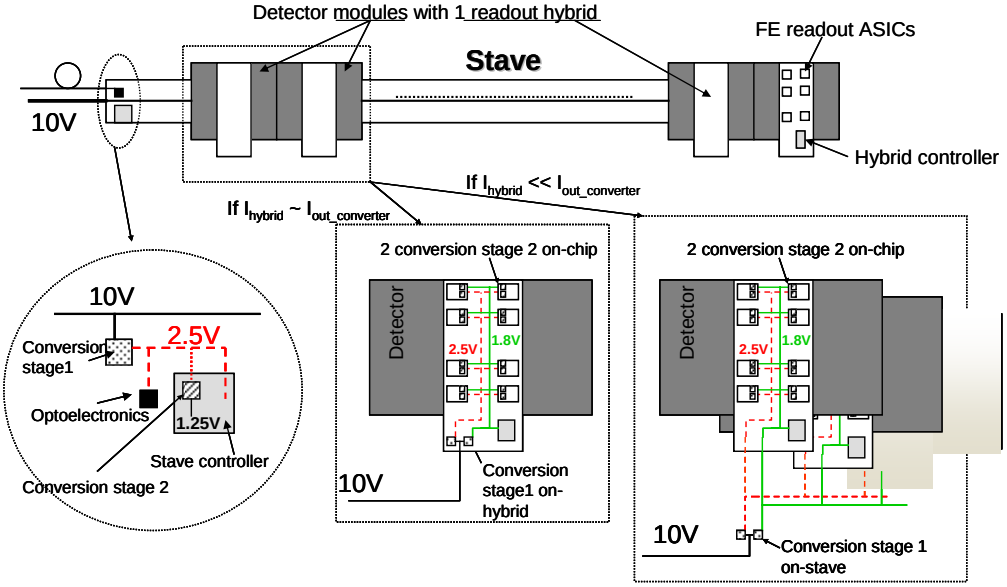

Figure 2: Possible implementation of the proposed distribution scheme. The choice on whether to have the conversion stage 1 on-hybrid or on-stave (to serve several neighbour hybrids) depends on the power rating of the converter and hybrid and on available space.

All these attractive features require some fundamental problems to be solved for a successful implementation. In the first place, both conversion stages being embedded on stave, each converter needs to be tolerant to both the radiation and magnetic field present in the tracker. Commercial step-down converters being designed to use ferromagnetic inductors that saturate in the 2-4 T magnetic field, and not being engineered to reliably tolerate high levels of radiation, are not usable. Therefore a dedicate development is needed (ASIC). An additional concern is the integration of switching converters at close proximity to the very sensitive readout ASICs and silicon detectors. Due to their switching nature, these converters introduce noise sources that might affect the system's performance. This last aspect is discussed in more detail in [5], [6].

III. PRACTICAL IMPLEMENTATION

The practical implementation of the distribution scheme proposed in II requires the analysis and comparison of different converter topologies in order to select the most appropriate for each conversion stage. The following five step-down topologies have been identified as the most attractive for our applications and have been evaluated:

- Buck converter (Figure 3). This is the simplest topology and the one making use of the smallest number of components, but at the same time it requires a large output capacitance for ripple cancellation and it functions with the larger RMS current in the inductor – not ideal for electromagnetic noise. A first prototype of this topology for our applications has already been designed [7] and tested [8].

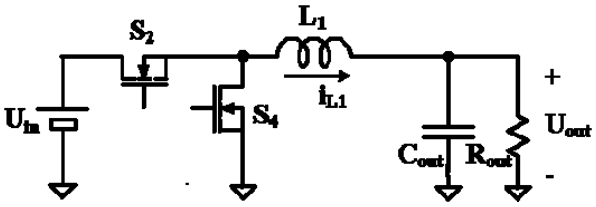

Figure 3: Schematic of the buck converter. S2 and S4 are the power switches, and the control circuitry is not shown.

- Four-phase interleaved buck converter. In this topology, the power switches and inductor of Figure 3 are divided into 4 parallel branches each switching with a delay of ¼ of the period. In this way, it is possible to reduce the RMS current in each branch and to achieve a reduction of the output ripple (actually, for a conversion ratio of 4 the ripple is ideally cancelled). This topology requires a large number of components – amongst which 4 inductors – and a complicated control circuit.
- Two-phase interleaved buck with integrated voltage divider (Figure 4). This topology, inspired by a similar step-up implementation [9], allows a conversion ratio of 4 with the use of only 2 interleaved branches, still achieving ripple cancellation. With respect to the four-phase interleaved, it minimizes the number of components and greatly simplifies the control circuitry.

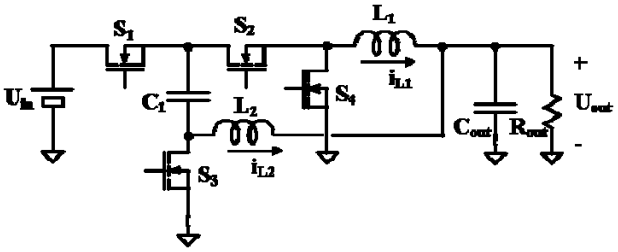

Figure 4: Schematic of the two-phase interleaved buck with integrated voltage divider.

- Multi-resonant buck converter. This topology, originally proposed in [10], has the interest of reducing the switching losses because all switching takes place in either Zero-Voltage or Zero-Current conditions. Nevertheless, this comes to the price of having large RMS currents, hence large conductive losses, and large V_{ds} across transistors – increasing the V_{dd} requirements on the technology. Additionally, the resonance is found for a specific load condition only, and re-tuning is necessary for different loads.
- Switched capacitor voltage divider. This is the only topology that does not require inductances, which is an attractive feature given the limitations imposed to inductors by our application. The simpler implementations of this topology are easy to integrate but do not provide regulation to the output. Overall, this is a good topology to be used as a divide-by-2 in a multi-stage distribution solution.

A. Conversion stage 1

This converter decreases the 10V input voltage to an intermediate bus voltage of 2.5 or 1.8V, which implies that the technology used for its fabrication must be capable of sustaining 10V with some safety headroom. At the same time, the full integration of both the power switches and the control circuitry on a single chip is a desirable feature to reduce component footprint, parasitic capacitance and inductance, and to simplify packaging and qualification tests. The best solution is therefore the use of a technology offering both high-voltage and low-voltage transistors. Several such technologies, mainly aimed at the automotive market, are available today, and a market survey completed by irradiation tests is currently on-going. A technology in the 0.35µm node is currently been used for a first prototyping phase [8], and irradiation tests are scheduled for 0.18 and 0.13µm technologies.

Since ferromagnetic materials can not be used in the tracker's magnetic field, the converter has to rely on air-core (or 'coreless') inductors [11]. These can be manufactured in very different topologies, but in this paper we will assume all inductors to be commercial and taken from the Coilcraft RF 132 series. These components are solenoid copper coils of reasonably small size (9.6x5.8x6.6

mm^3) and very low DC resistance – 2 to 83 mΩ depending on the inductor value (maximum = 709nH). This latter property has a large impact on the converter efficiency.

To select the most appropriate topology for conversion stage 1, the five topologies listed above have been compared for a conversion ratio of 4 (V_{in}=10V, V_{out}=2.5V) and an output power of 6W. For each topology we have determined the current and voltage waveforms and estimated the main losses to eventually computing the efficiency. Calculations were carried out with Mathcad worksheets for each topology, making it easy to change the converter requirements (voltages, power) and the parameters of the inductor. Results are summarized in Table 2, where parameters for a 0.18µm high-voltage technology have been used. For the switched capacitor solutions, 2 stages in series – each divide-by-2 – were used. It has to be pointed out that the results in Table 2 have been obtained without modelling in detail the switching losses; hence the obtained efficiency is optimistic for all topologies and should be used in a relative fashion to compare them.

Table2: Relative comparison of different converter topologies for V_{in}=10V, V_{out}=2.5V, P=6W. Figures of merit are efficiency and number of components required (power switches, capacitors and inductors). NB: the multi-resonant requires an additional diode.

Topology	Efficiency (%)	Freq. (MHz)	N. of switches	N. of caps.	N. of induct.
Buck converter	86	5	2	2	1
4-phase interleaved	88.3	5	8	2	4
2-phase interleaved with voltage divider	89.7	5	4	3	2
Multi-resonant	82.5	8.8	1	4	2
2 cascaded SW Cap	87.3	2	8	7	0

From the comparison table, and from the generic properties of each configuration listed above, it appears that the most appealing topologies are the buck converter (for its small number of components) and the 2-phase interleaved with voltage divider (for its efficiency, relative small number of components and complexity). Although a final choice between the two topologies has been delayed until a more thorough comparison can be made, a detailed parametric calculation for the 2-phase interleaved has been used in the following to estimate the system's efficiency. In this exercise, we refined our model to more precisely take into account the switching losses by including simulation results from the 0.18µm technology.

At first, we concentrated on the choice of the optimum switching frequency of operation. The typical picture is that at low frequency, where a larger inductance is needed, conduction losses in the larger ESR of the inductor decrease the efficiency. At high frequency, more energy is dissipated in the switching. The highest efficiency is therefore found at some "intermediate" frequency, in our case about 1MHz. This is shown in Figure 5 for both the "analog" (V_{out}=2.5V) and "digital" (V_{out}=1.8V) converters in stage 1 and for an output power of 6W. The optimum inductor size changing with the frequency, for each point in the chart a different inductor from the Coilcraft RF 132 series was taken and its resistance was corrected for skin effect as appropriate for each frequency.

We then performed calculations for different loads and determined the size of the power switches leading to the highest efficiency in our distribution scheme. This will drive the development of converter prototypes. From our calculations, in the 0.18µm technology considered, the optimum size for the power switches gives an on-resistance of 30mΩ. The inductor to be used for the converter is chosen as a function of the load current and its value, together with the estimated efficiency for the converter, is reported in Figure 6 for both the analog and digital conversion stage 1 (inductors from the Coilcraft RF 132 series). An efficiency of around 90% can be reached for the conversion stage 1 of the analog power distribution, whilst a peak of about 86% is possible for its counterpart in the digital power distribution, in both cases for output currents in the range 3-5 A.

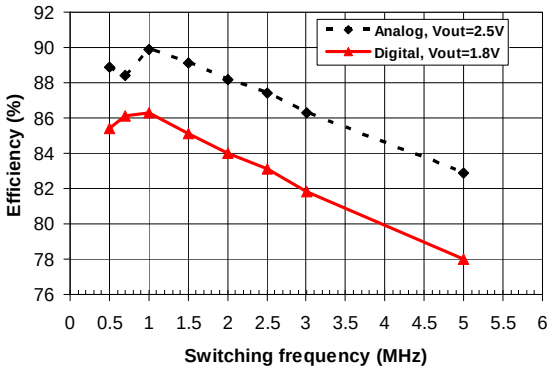

Figure 5: Estimated converter efficiency as a function of the frequency of operation for both the "analog" and "digital" power distribution (conversion stage 1). Results for R_{on}= 30mΩ.

B. Conversion stage 2

In the proposed distribution scheme, converter stage 2 is integrated in the front-end readout or controller ASICs, and has therefore to provide a more modest level of current (20-100mA). The possibility of using a magnetic converter for this stage would be attractive only if the inductor could be embedded on-chip, which is not possible because of the large ESR of on-chip inductors (about 1Ω for a 15nH inductor in state-of-the-art 130nm RF technologies). A switched capacitor converter, used as a divide-by-2 stage, seems to be the most adequate solution in this case even in the absence of regulation from the converter (regulation is provided by a stage 1 converter a few cm away).

The schematic of the switched capacitor converter considered in our work is shown in Figure 7 [12]. The

"flying" capacitor C_1 is alternatively connected in parallel to either C_2 for recharge or C_3 to provide power to the load. Such switching sequence is driven by a control circuit that drives the gate of transistors Q_1 to Q_4. A quick simulation has been run for this topology in a 130nm technology, using I/O transistors as switches, and gave an efficiency of 93% for a switching frequency of 20MHz. It seems therefore likely that, after careful choice of the most appropriate operating parameters (frequency in particular), an efficiency larger than this value can be obtained.

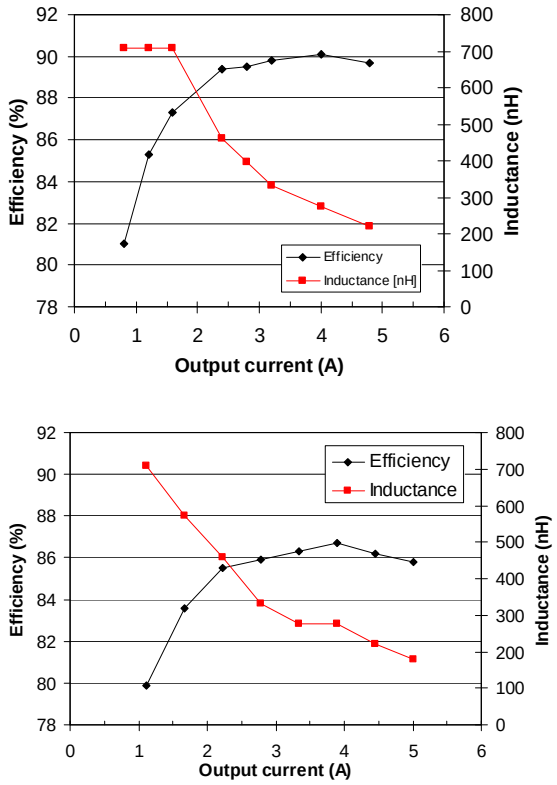

Figure 6: Estimated efficiency and required inductance for the ASIC used as conversion stage 1 for the "analog" (V_{out}=2.5V, top) and "digital" (V_{out}=1.8V, bottom) power distribution for different output loads

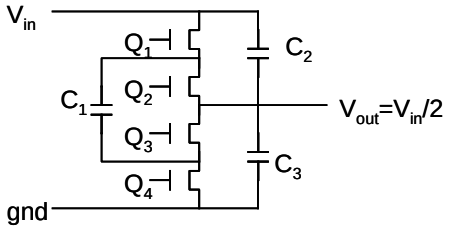

Figure 7: Schematic of the switched capacitor converter considered in this work.

IV. Conclusion

A power distribution scheme based on the use of on-hybrid and/or on-stave switching converters can satisfy the requirements for the SLHC generation of experiments. A comprehensive comparative study of different converter topologies led us to the choice of a 2-stages scheme. A first stage with a ratio of 4 is implemented as a 2-phase interleaved buck converter with integrated voltage divider or as a simple buck converter and requires the use of a technology rated for high-voltage (15-20V) applications. A second stage with a ratio of 2 is implemented as switched capacitor converter on-chip. Our calculations show that, combining the efficiencies of first and second conversion stages, an overall efficiency larger than 80% is achievable.

The proposed distribution scheme allows for distributing multiple voltages on-stave from a unique 10V input line from off-detector power supplies. Different voltages for analog and digital functions can easily be supported, achieving superior system efficiency. It also provides large modularity for grouping on-hybrid ASICs in power groups and facilitating system start-up and turn off of defective circuits.

V. References

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