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Custom DC-DC converters for distributing power in SLHC trackers

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The tenfold increase in the number of channels in SLHC trackers, and the wish to actually decrease the material budget to improve the physics performance of the detectors, set uncomfortable limits for the on-detector power budget. A power distribution system based on DC-DC converters has the potential to contribute significantly to the drastic reduction in wasted power necessary to meet these limits. A possible distribution scheme, based on two stages of conversion performed by custom-developed components, is discussed together with the main technical challenges for the development of these components.

Summary

In the design of upgraded trackers for SLHC, the HEP community will strive to reduce material budget with respect to the LHC trackers just completed. A quick look at the relative contribution to the total material inside these trackers clearly shows that cables and cooling systems are amongst the 3 main contributors –the third being the mechanical supporting structure which is also somehow related to the other two.

Since both cables and cooling depend on the amount of power burnt in the tracker, we evidently need to manage such power: how to minimize the power necessary to perform the electronic functions required inside the trackers and how to bring this power where it is needed. To address the first issue, designers of front-end, control and communication electronics will need to optimize their designs to perform the essential functions at minimum power. This will most likely result in FE ASICs manufactured in advanced CMOS/BiCMOS technologies, where different voltage levels are used for different functionalities (e.g. analog and digital), and where large circuit blocks are turned off whenever possible. To address the second issue, the power distribution system shall provide regulated power to the on-detector electronics with minimum losses on the way. This implies the capability of locally supplying different voltage levels, with loads variable in time, from a small number of low-current cables from the off-detector power supplies.

This contribution presents a power distribution system based on two stages of DC-DC converters and having the potential to meet the above requirements.

A first stage with a conversion ratio of 4 reduces the input voltage to an intermediate bus voltage of about 3V. This component shall therefore be compatible with an input voltage of 12V, which forbids the use of the same advanced low-voltage submicron technologies used for the front-end ASICs. Special high-voltage technologies from automotive applications look adequate, but require qualification and special design techniques for reliable radiation hardness. One example of such qualification study will be presented. On the other hand, the topology of this first stage of conversion is strongly influenced by the necessity to use air-core inductors as magnetic elements, and of minimizing the output ripple and the noise. A possible topology addressing all these constraints is discussed.

The second stage, acting as a Point-Of-Load converter, takes power from the 3V intermediate bus and converts it to the appropriate voltage required by the electronics. This POL sits very close to the on-detector ASICs, possibly even on-chip, and given the 3V input voltage requirement it can be manufactured in the same advanced technology. This in turn makes it possible to achieve a switching frequency in the tens of MHz range –which limits the noise injected in the system at frequencies where the FE ASICs are most sensitive. A high switching frequency allows for inductor values in the nH range, available for on-chip integration in advanced CMOS processes for RF applications. A possible topology for the POL converter will also be discussed.

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