Characterization of the Noise Properties of DC to DC Converters for the sLHC

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Abstract

The upgrade of the Large Hadron Collider (LHC) experiments sets new challenges for the powering of the detectors. One of the powering schemes under study is based on buck converters mounted on the front-end modules. The switching noise emitted by these converters is susceptible to affect the performance of the powered systems. A model to identify and to control the noise sources of the converter was developed. A reference test setup with associated measurement methods is used to characterize the noise properties of the converter. Complementary tools and simulations were also used to evaluate the noise couplings at system level.

I. Introduction

The experiments at the Super Large Hadron Collider (sLHC) will be more demanding in terms of power and cabling than at the LHC, in particular for the trackers. The cabling constrains of the detectors, together with the thermal management and the overall power efficiency, force the development of new radiation hard and magnetic field tolerant powering schemes. One of the proposed schemes is based on air core buck converters [1] to be distributed on the front-end (FE) modules of the trackers [2].

The switching converter and its air core inductor will be placed in the close vicinity of the FE detectors and electronics. The FE system will be exposed to new sources of noise from the power converters (Fig.1), in the form of conducted and radiated electromagnetic noise.

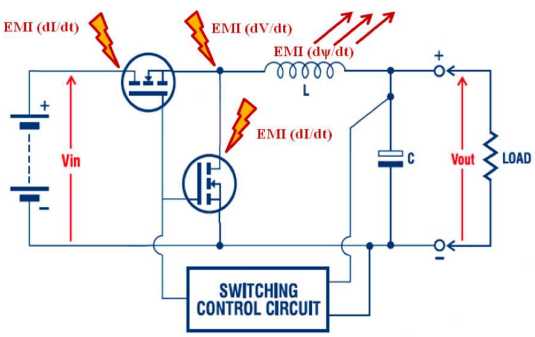

Figure 1: Noise emission model of a buck converter.

Like in industrial, medical or military applications, the reduction and control of electromagnetic interferences (EMI) is also a topic of primary importance for today's high energy physics experiments. These interferences can produce malfunctions on the devices, because of this it has been necessary to establish limits for the maximum amount of radio frequency (RF) noise that an equipment can emit and the minimum noise that it must be able to tolerate. The electromagnetic compatibility (EMC) tries to achieve that goal, establishing limits for the harmony and well operation of the equipments when they are put together in a system. International EMC standards as CISPR were born, forcing the manufacturers to fulfill those limits for being able to sell their products in Europe and in the USA.

The theory of electromagnetic compatibility is well described in the literature [3][4], providing valuable guidelines for the engineers to develop systems in compliance with the standards at early stages of the design process. The understanding of the EMC aspects of a system requires a deep analysis, usually carried out on the basis of models that enable simulations. Several models have been published aiming to predict the common mode (CM) and differential mode (DM) noise for different kinds of switching converters. These models rely on simplifications, the most relevant one being the substitution of the switching devices with the waveforms seen across their nodes [5]. Further simplifications assume an ideal characteristic of critical passive components [6] or neglect the presence of parasitic capacitances between the nodes of the printed circuit boards and the ground plane [7].

This paper proposes a model to predict the CM current at the input and output ports of a PWM buck converter, considering the dV/dt that results from the switching action of the MOSFETs as the primary source of common mode current. The proposed model is based on the susbtitution described earlier of the power transistors with the switching voltage developed between the drain and source nodes. However, aiming for an improved accuracy of the model, the parasitic properties of the passive components and the stray capacitances between the board nodes and the ground plane are taken into account. This model was analyzed through parametric simulations, in order to find the fundamental factors that contribute to the generation of the CM noise. The determination of the noise sources and the associated coupling paths allow applying suitable grounding, shielding and filtering methods to achieve the required detector performance. Experimental results will be compared with the simulations, in order to validate the model.

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II. Measurement method for common mode current

To ensure an accurate and reproducible measurement of the conducted noise of a specific equipment under test (EUT), a standard and well define test setup is required. Fig. 2 illustrates the scheme used for measuring the common mode current of a power converter, where the following items are found:

- A copper ground plane to define a low impedance return path for the common mode currents. The converter is placed 40 mm above the ground plane, fixing in that way the stray capacitances with respect to earth of every node of the converter's PCB.
- A standardized line impedance stabilization network (LISN) on both input and output ports. The LISN provides ideally a 50 Ω common mode impedance to the ground plane between 150 kHz and 30 MHz, allowing for reproducibility and comparison of the results obtained at different test places. The LISN also provides the isolation of the conducted noise coming from the power mains and a port for measuring the RF voltage emitted by the EUT.
- Input and output shielded cables, with the shield ends bonded to the ground plane to prevent capacitive and inductive couplings.

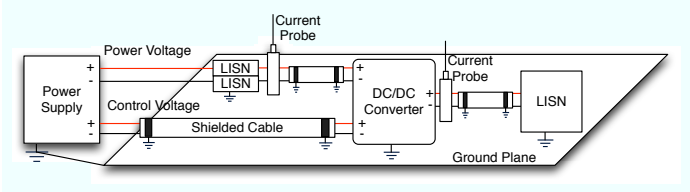

Figure 2: Scheme of the measurement setup for DC/DC converters.

The common mode current is measured with a calibrated current probe and a high resolution EMI receiver. Fig. 3 shows a picture of the test bench used for the measurements.

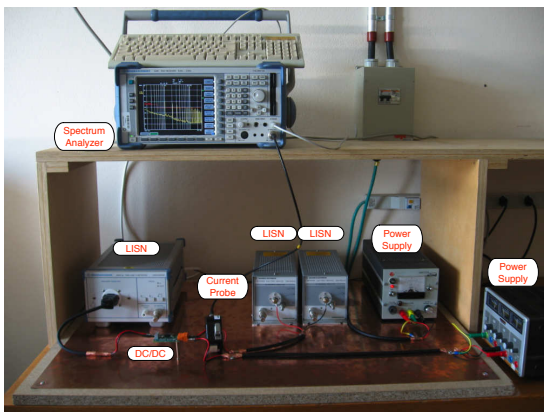

Figure 3: Test setup.

III. Conducted common mode noise modeling

The arrangement of the power converter to be tested, fixed on the test bench and properly connected to the LISN, can be modeled for simulation purposes. This model tries to give an insight in the prediction of the CM current before the converter has been built, helping in the early design stage.

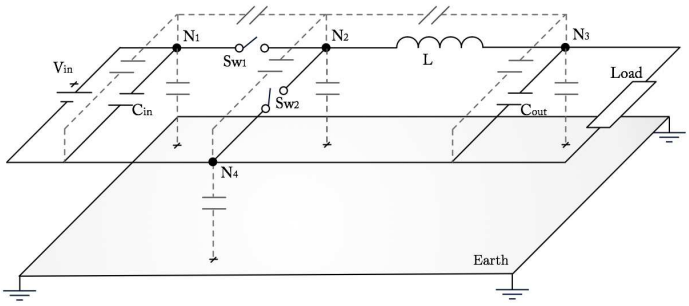

Figure 4: Principal nodes and stray capacitances (dotted lines) for a Buck converter.

A prototype buck converter was modeled on this basis. The principal nodes of the buck converter and the stray capacitances between them were identified and are showed in Fig. 4. A 3D model of the converter's printed circuit board was analyzed with Ansoft Q3D (Figure 5) in order to obtain the values of the stray capacitances between all the critical nodes and the ground plane. The obtained result is displayed as a matrix of order N×N (see the Table 1), N being the number of nodes.

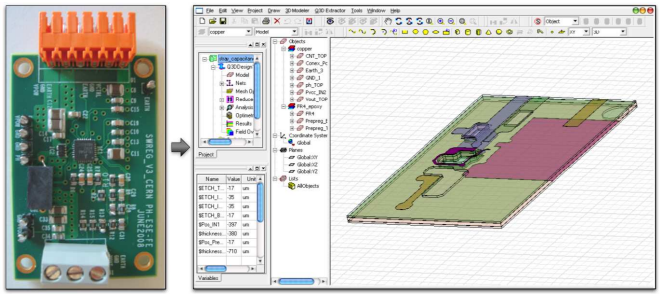

Figure 5: Q3D simulation of stray capacitances to earth of the buck converter.

Table 1: Stray capacitance matrix in pF.

pF	Earth	N1	N2	N3	N4
Earth	- - -	0.069	0.0062	0.0074	3.8097
N1	0.069	- - -	0.018	0.0012	11.926
N2	0.0062	0.018	- - -	0	3.3286
N3	0.0074	0.0012	0	- - -	5
N4	3.8097	11.926	3.3286	5	- - -

The power converters can have a switching frequency up to few MHz, and the resulting spectrum of harmonic frequencies that contribute to the conducted noise can span up to many tens of MHz. In this range of frequencies, the passive components

can't be considered as ideal anymore. The impedances of the real passive components in Fig. 4 (C_{in}, C_{out} and L) were measured using a HP 4194A impedance analyzer, and a three component model was obtained for each of them. The ideal passive components were replaced with the high frequency models (Fig. 6). Their values are shown in the Table 2.

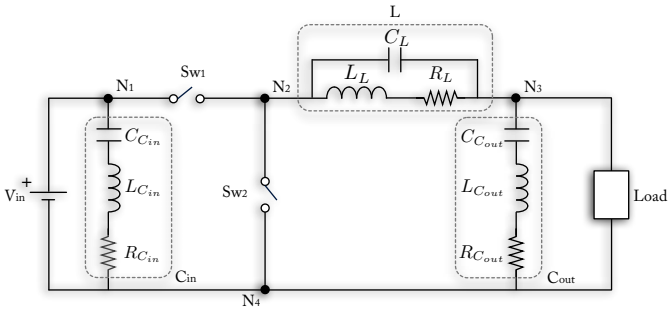

Figure 6: High frequency model of the real components.

Table 2: High frequency model's values

	R	L	C
C_{in}	8.8mΩ	0.72nH	$30\mu F$
C_{out}	8mΩ	1.45nH	$14{,}1\mu F$
L	90m Ω	531.8nH	$22.5pF$

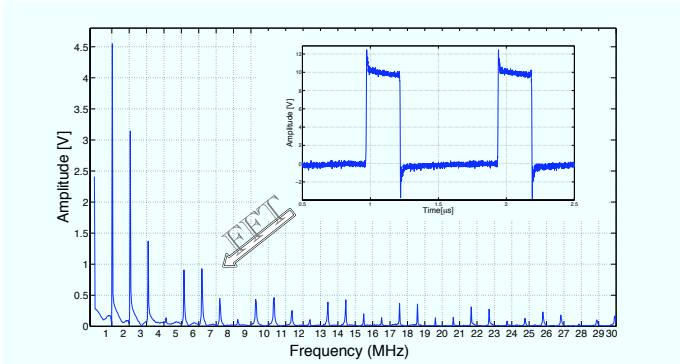

Figure 7: FFT of the temporal Drain-Source voltage in the lower switch.

In order to model the effect of the switches on the CM noise and to make the circuit linear, they are replaced by normalized AC voltage sources of 1V, phased out by 180 degrees. The substitution enables the fast AC simulation of the linear circuit using PSpice. These simulation runs predict the input and output common mode current for a normalized switch voltage of 1V for all the frequency range, expressed in ampere per volt. To compute the net common mode current emitted by the modeled converter, the frequency spectrum of the switch voltages is determined by means of the FFT of the waveform (Fig. 7). The obtained frequency voltage peaks are multiplied with the normalized CM current curves obtained from the simulation.

The method is exercised on the buck converter model described previously, taking into account the stray capacitances (Fig. 4), high frequency models (Fig. 6) and voltage sources instead of the switches (Fig. 7), as is shown in Fig. 8. The converter switches at 1 MHz, with a duty cycle of 25%. The drain to source voltage across the switches was measured with differential probes and its spectrum (obtained by FFT) is used to weight the normalized simulation data to explore the validity of the proposed model.

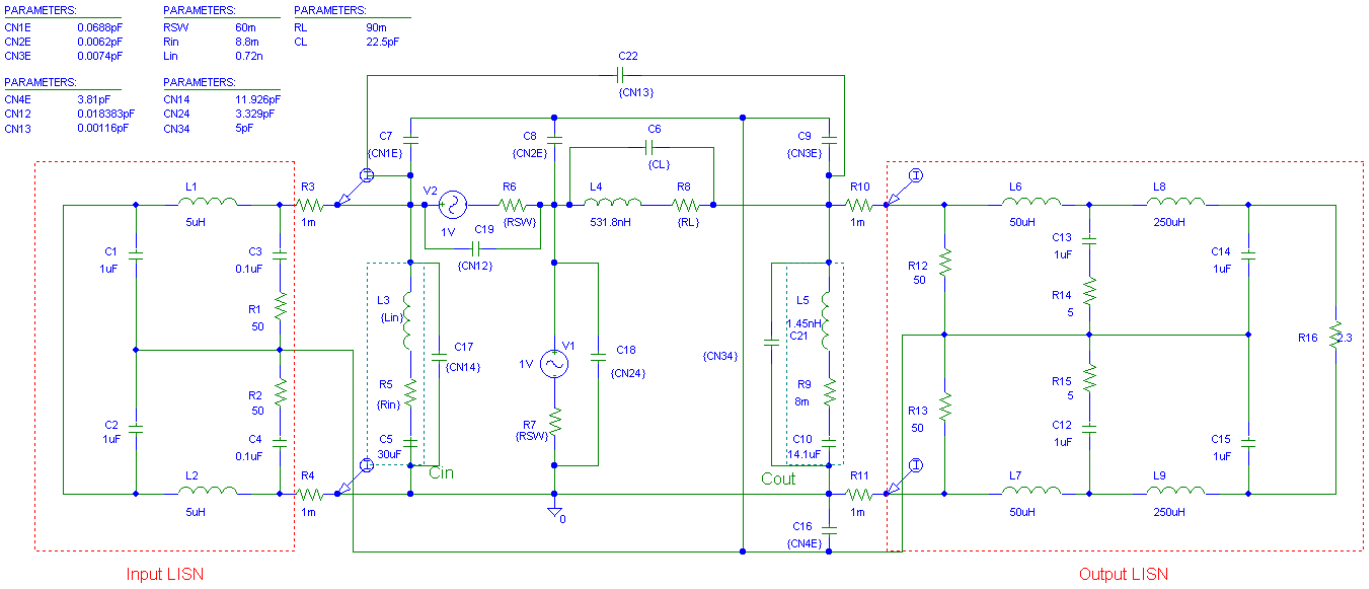

Figure 8: Conducted Common Mode noise simulation model.

IV. Model analysis

The model allows exploring, with parametric simulations, the impact of each element on the input and output common mode current. It predicts that the conducted noise emissions are strongly dependent of the electrical properties of the input and output capacitances, in particular of the lead inductance (Fig. 9) and the series resistance (Fig. 10). Nevertheless, the value of the capacitance itself doesn't play a major role, except at low frequencies (Fig. 11).

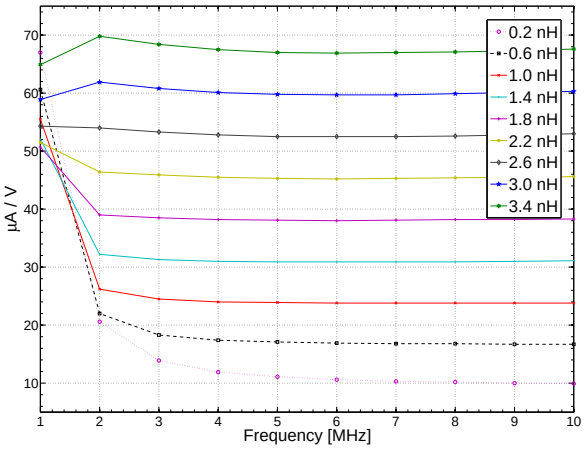

Figure 9: Normalized input common mode current versus $L_{C_{out}}$.

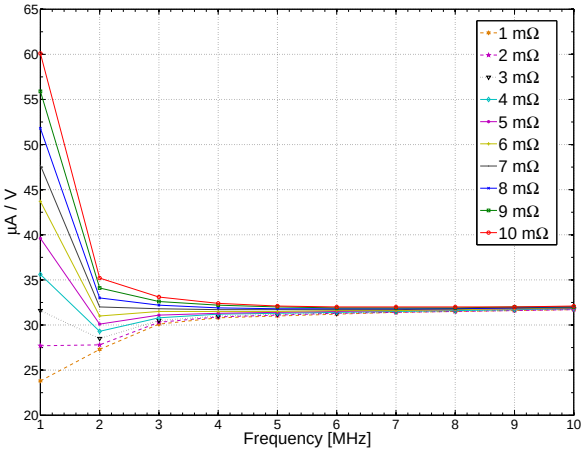

Figure 10: Normalized input common mode current versus $R_{C_{out}}$.

The proposed setup (Fig. 2) makes the measurement result insensitive to the stray capacitances to the ground plane, being the noise exclusively contributed by the design of the converter. This was corroborated empirically placing the converter at different heights and measuring the respective CM noise, finding no differences between the measurements. Actually, the LISNs provide a relatively low impedance path for the CM current, such that the current flowing through the stray capacitances is negligible. The design of the converter, and in particular the choice of the passive components, can be explored experimentally on the basis of the model simulations, making abstraction of any stray capacitance between the converter and the ground plane. It must be noted that this is not longer true if a short circuit is made between the return path and the ground plane.

In order to estimate the effect of the stray capacitances, the output LISN must be replaced by the model of the targeted load (taking into account the capacitance between the load and earth). In this configuration, the CM noise model becomes sensitive to the high frequency model of the load that is used, enabling the optimization of the grounding of the front-end to minimize the amount of noise current injected by the converter into it.

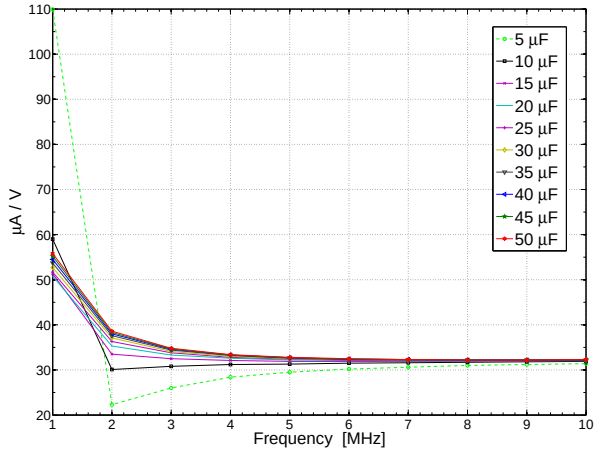

Figure 11: Normalized input common mode current versus $C_{C_{in}}$.

V. Model validation

To validate the results obtained with the model, a comparison between the simulation and the measurement was done for the converter prototype. Fig.12 shows the comparison for the measured and simulated first ten harmonic peaks. The simulations are in good agreement with the measurements, the bigger difference being found for the 4th and 8th harmonic, attributed to inductive near field couplings that are not taken into account by the proposed model.

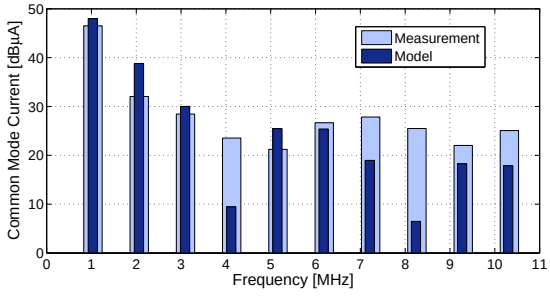

Figure 12: Predicted and measured CM currents with the nominal array of capacitors.

The model analysis revealed a dominant contribution of the decoupling capacitors properties to the conducted noise current. To validate this, the same buck converter prototype was simulated and measured using different decoupling capacitors. The capacitors were measured and modeled with an impedance an-

alyzer, and then included in the PSpice model (Table 3). In the same way, the CM noise for the new converters was measured. First, 100μF ceramic capacitors were put at the input and output of the converter (Table 3). The comparison between the simulation and the measurement is illustrated in Fig. 13. In comparison with the original configuration (Fig. 12), it can be seen that the model predicts a 7.5dB increase of the CM current for the converter equipped with the new 100uF ceramic capacitors that is corroborated by the measurements.

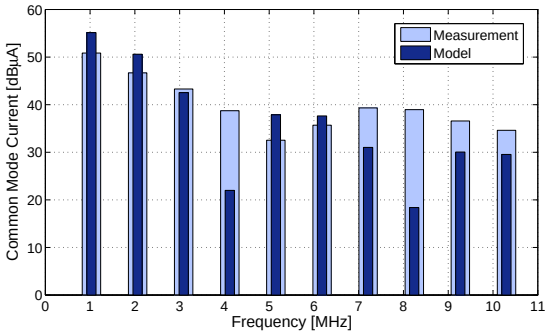

Figure 13: Predicted and measured CM currents with one ceramic capacitor of 100 μ F on the input and on the output.

If electrolytic capacitors are used instead (Table 3), the model predicts again a further increase of 12.9 dB of the noise current respect to the ceramic capacitors, again verified with the measurements. This proves empirically that the decoupling capacitors have a significant impact in the conducted CM noise emitted by the converter (Fig. 14).

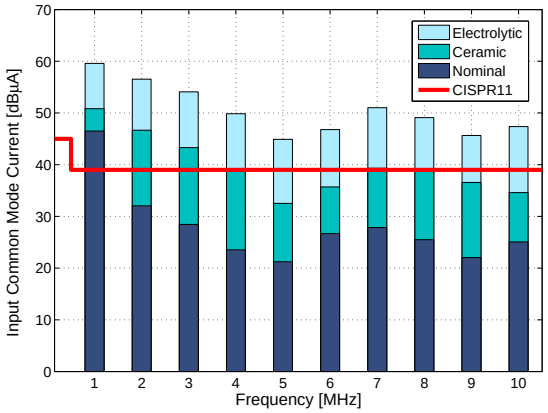

Figure 14: Measured CM current for nominal (Table 2) and new arrays of capacitors (Table 3).

Table 3: Different capacitor arrays parasitics

	R	L	C
Ceramic	0.8mΩ	3.5nH	76.9μF
Electrolytic	95,4mΩ	6.96nH	111.2μF

VI. Conclusions

The powering challenge for the sLHC requires the understanding of the noise couplings mechanisms between power converters and the front-end electronics. For this, a model of the common mode current for a buck DC/DC converter has been proposed, considering the two switches as the dominant contributor of the emitted noise. An innovative method to make the circuit linear has been proposed, enabling simple parametric simulations that allowed the identification of the decoupling capacitors as critical components for the design process.

The simulation results were cross checked on prototypes with different arrangements of decoupling capacitors, confirming the announced sensitivity to the capacitors parasitic. The model appears to be in agreement with the measurements up to 10 MHz. Discrepancies are observed at some harmonic frequencies, attributed to inductive near field couplings that are not taken into account by the proposed model that considers the capacitive coupling as the major contributor in the noise.

The test setup on which the model is defined, using LISNs on the input and output power ports, is intended for standard measurements. It allows measuring the output common mode noise, to make the model insensitive to its position with respect to the ground structure and to maximize the noise emissions for their analysis.

For front-end specific studies, the output LISN must be replaced by the front-end load model that should include the real parasitic parameters with respect to the grounded structure.

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