Characterization of the Noise Properties of DC to DC Converters for the sLHC

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Abstract

The upgrade of the LHC experiments sets new challenges for the powering of the detectors. One of the powering schemes under study is based on buck converters mounted on the front-end modules. The switching noise emitted by these converters is susceptible to affect the performance of the powered systems. A model to identify and to control the noise sources of the converter was developed. A reference test setup with associated measurement methods is used to characterize the noise properties of the converter. Complementary tools and simulations were also used to evaluate the noise couplings at system level.

Switched power conversion topology for the sLHC

The experiments at the sLHC will be more demanding in terms of power and cabling than at the LHC, in particular for the trackers. The cabling constrains of the detectors, together with the thermal management and the overall power efficiency force the development of new radiation hard and magnetic field tolerant powering. One of the proposed powering schemes is based on air core buck converters to be distributed on the front end modules of the trackers (Fig. 1).

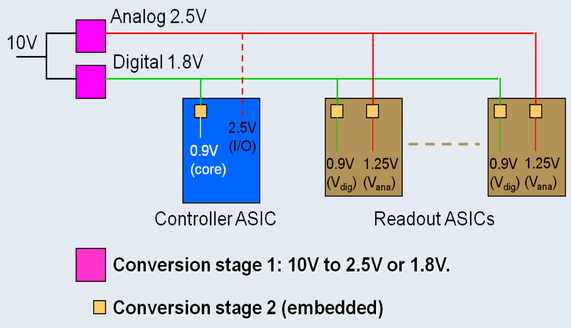

Figure 1: proposed power distribution topology for the sLHC.

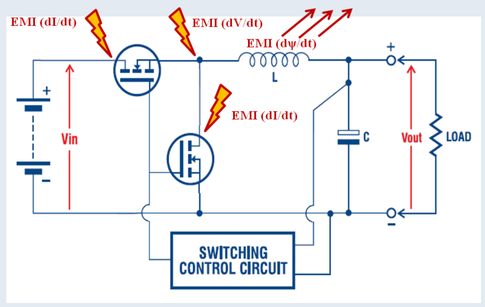

Figure 2: noise emission model of a buck converter.

The switching converter and its air core inductor will sit in the close vicinity of the front-end detectors and electronics. The front-end system will be exposed to new sources of noise from the power converters, in the form of conducted and radiated noise. To achieve the required detector performance, these noise sources must be understood so that a suitable grounding, shielding and filtering methods can be applied.

In the proposed buck converter, the dominant noise sources are (Fig.2):

- dV/dt at the phase node between the two switches, that develops common mode currents on the input and output cables through on-board and stray capacitances.
- dI/dt at the drain tracks that connect to the switches, that develop common mode currents on the input and output cables through near field inductive coupling.
- dφ/dt radiated by the inductor that will develop common mode and differential mode disturbances in the front-end module.

Measurement method

The accurate and reproducible measurement of the conducted noise requires the use of a well defined test setup (Fig.3):

- A plain ground plane to define a low impedance return path for the common mode currents.
- Standardized line impedance stabilization network (LISN) on both input and output ports to set a known impedance between each wire and the ground plane. The LISN provides a 50 Ω common mode impedance to the ground plane between 150 kHz and 30 MHz.
- The input and output cables are shielded, with the shield ends bonded to the ground plane.

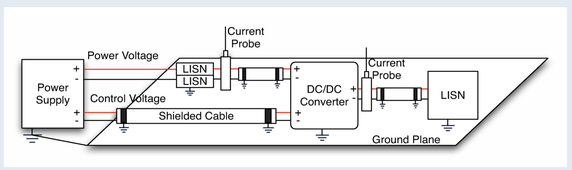

Figure 3: characterization setup for DC/DC converters.

The common mode current is measured with a calibrated current probe and a high resolution EMI receiver or spectrum analyzer. The converter under test is placed at a distance of 40mm above the ground plane (Fig.4).

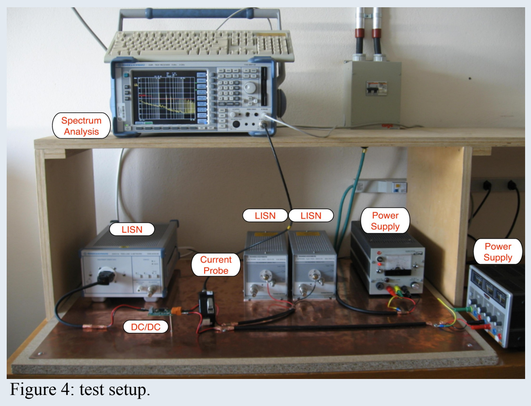

Figure 4: test setup.

Conducted noise modeling

The contribution of the switches drain to source voltage to the conducted noise is modeled in PSpice on the basis of the buck converter connected between the LISNs, above a ground plane (Fig.5):

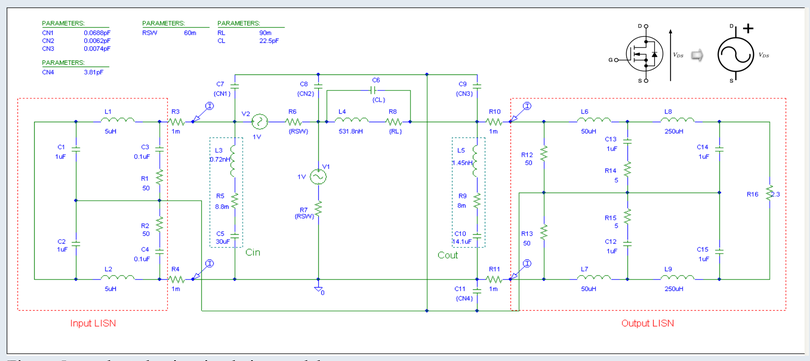

Figure 5: conducted noise simulation model.

The PSpice model includes the printed circuit board capacitances estimated with Ansoft Q3D (Fig. 6), and the measured model of each decoupling capacitor (Fig. 7). The switches are replaced in the model by normalized voltage sources of 1V, phased out by 180 degrees, in order to make the circuit linear. This allows predicting the input and output common mode current for a normalized switch voltage of 1V at each harmonic frequency.

To obtain the net common mode current, each normalized frequency peak obtained from the PSpice simulation is then weighted with the corresponding FFT peak of the measured drain to source voltage (Fig. 8).

Board capacitances modeling

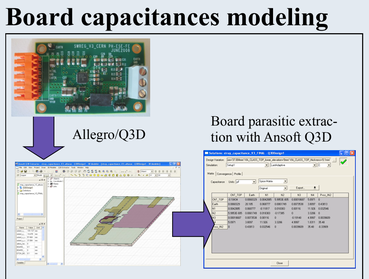

Fig.6: The board copper geometry is analyzed with Ansoft Q3D tool to extract the values of the critical stray capacitances between tracks and copper planes.

Decoupling capacitances modeling

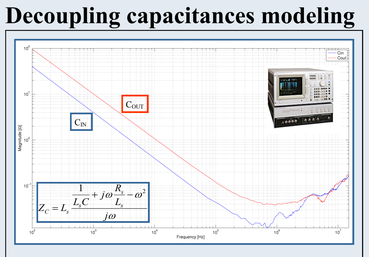

Fig.7: The exact capacitances, series resistance and inductance of every decoupling capacitors is measured with an impedance analyzer.

Switch voltages modeling

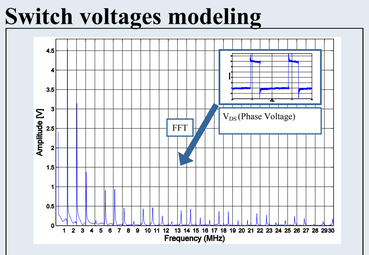

Fig.8: The phase voltage is accurately measured on the prototype The voltage magnitude of each harmonic frequency is computed through a fast Fourier transform.

Model analysis

Parametric simulation runs allow for the identification of critical parameters, such as the lead inductance (Fig. 9) and the series resistance (Fig. 11) of the decoupling capacitors. The model predicts that the conducted noise emissions are strongly dependent of the electrical properties of the input and output capacitances. However, the value of the capacitance itself doesn't appear as playing a major role, except at low frequencies (Fig. 10).

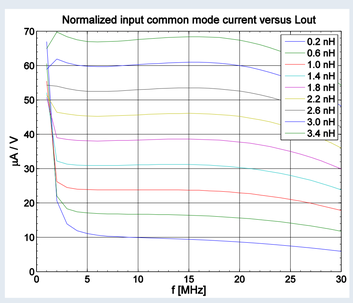

Fig.9: the input CM current is sensitive to the lead inductance of the output decoupling capacitor.

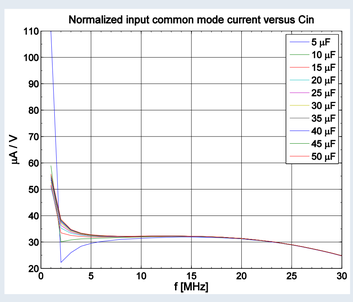

Fig.10: the input CM current is sensitive to the capacitance value for frequencies below 5 MHz.

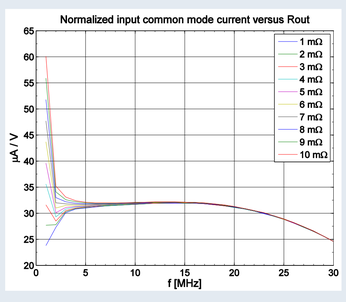

Fig.11: the input CM current is sensitive to the series resistance of the output decoupling capacitor for frequencies below 5 MHz.

The proposed setup makes the measurement result insensitive to the stray capacitances to the ground plane, the noise being exclusively contributed by the board layout and by the components used. In order to estimate the effect of these capacitances, the output LISN must be replaced by a single resistive load. The predictions of the model in this configuration are also in agreement with the measurements made on several prototypes.

Model validation

The model analysis reveals a dominant contribution of the decoupling capacitors properties to the conducted noise current. To validate this, the noise was modeled and then measured on a prototype fitted with different capacitors that were previously characterized. The nominal array of capacitors allows to achieve noise emissions 10 dB below the standard CISPR11 limit, while the use of inadequate electrolytic capacitors lead to noise emissions that are 15 dB above this reference limit (Fig. 14).

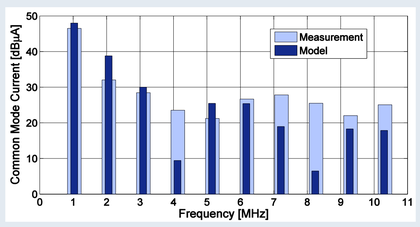

Figure 12: predicted and measured CM currents with the nominal array of capacitors.

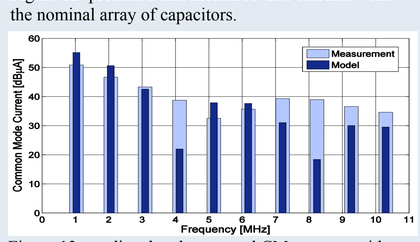

Figure 13: predicted and measured CM currents with one ceramic capacitor of 100 µF on the input and on the output.

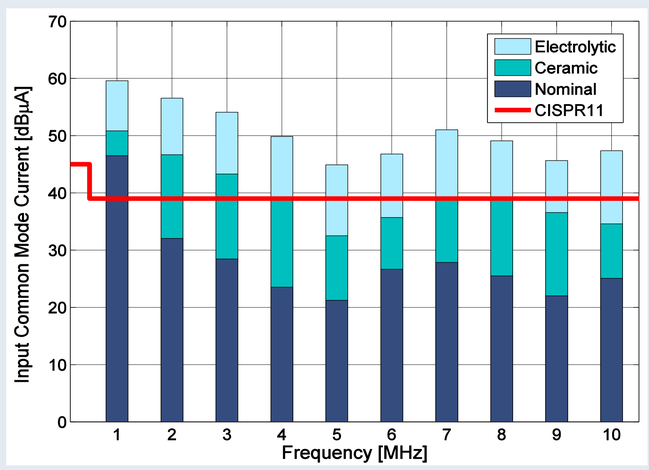

Figure 14: for different arrays of decoupling capacitors, the common mode current peaks at values of 46 dBµA (42 µF ceramic array, 8.8 mΩ, 0.7 nH), 51 dBµA (100 µF ceramic, 0.8 mΩ, 3.5 nH) and 60 dBµA (5x22 µF electrolytic, 95 mΩ, 7.0 nH).

The conducted noise spectrum measured on the prototypes appears to be in good agreement with the amplitudes predicted by the model, for frequencies up to 10 MHz.

Conclusions

The powering challenge for the sLHC requires the understanding of the noise couplings mechanisms between power converters and the front-end electronics. For this, a model of the common mode current for a buck DC/DC converter has been proposed, considering the two switches as the dominant contributor of the emitted noise. An innovative method to make the circuit linear has been proposed, enabling simple parametric simulations that allowed the identification of the decoupling capacitors as critical components for the design process.

The simulation results were cross checked on prototypes with different arrangements of decoupling capacitors, confirming the announced sensitivity to the capacitors parasitic. The model appears to be in agreement with the measurements up to 10 MHz. Discrepancies are observed at some harmonic frequencies, attributed to inductive near field couplings that are not taken into account by the proposed model, that considers the capacitive coupling as the major contributor in the noise.

The test setup on which the model is defined, using LISNs on the input and output power ports, is intended for standard measurements. It allows to make the model insensitive to its position with respect to the ground structure and to maximize the noise emissions for their analysis.

For front-end specific studies, the output LISN must be replaced by the front-end load model that should include the real parasitic parameters with respect to the grounded structure.