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Development of a fast readout system for DEPFET sensors

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The DEPFET sensor is a favorable technology for use in particle physics experiments. The current system is developed for application in the vertex detector of the planned International Linear Collider (ILC). Besides high spatial resolution, low noise and a low material budget a very high readout speed is required. A new prototype readout system has been built; utilizing a new generation of DEPFET sensors (PXD5) with up to 256x1024 channels, new steering ASICs (called Switcher3), new readout ASICs (called DCD2) and a new FPGA-based high speed PCB. An overview of this system will be given and first measurements will be shown.

Summary

The DEPFET sensors are based on a fully depleted high resistivity silicon substrate, where a field effect transistor is directly integrated into every pixel. An additional implantation below the FET creates a potential minimum for electrons right underneath the transistor channel. Signal electrons created by an impinging particle will be collected in this so-called internal gate, resulting in a modulation of the transistor current. This concept allows the first amplification stage to be realized with a very small input capacitance, thus featuring intrinsically low noise measurements. Pixel sizes of 24x24um² guarantee a binary position resolution of ˜7um, while a resolution «4um can be achieved using analog readout.

In addition to high spatial resolution, low power consumption and low material budget, the physics goals of a future vertex detector for the ILC require a high readout speed to cope with the expected hit densities. For this purpose a new prototype readout system is being developed.

The DEPFET system consists of the sensor matrix itself, a control ASIC (called Switcher3), a readout ASIC (called DCD2) and a FPGA-based control and data acquisition system.

The Switcher3 chip is a fast analog multiplexer with an integrated intelligent sequencer. It is used to select and enable individual pixel rows for readout operation, and to perform a clearing operation of the accumulated charge. The outputs must be able to switch voltages of up to 10V and achieve rise/fall times of <10ns for a load of 20pF. Fast settling times are not only crucial for high speed readout, but also for complete clearing of the accumulated charge ensuring a low noise operation.

The second ASIC (DCD2, “drain current digitizer”, successor of CURO) is used to process the drain signal currents of the DEPFET. The drain voltage has to be kept constant for high speed readout; therefore a regulated cascode has been chosen to provide a low input resistance to the DCD2 chip. The design has been optimized for input capacitances of up to 40pF, which corresponds to the drain lines of long DEPFET matrices (1024 Switcher channels and 256 readout channels). The DCD2 chip features an algorithmic current-based ADC with eight bit resolution in every input channel; the signal currents are immediately digitized. One LVDS channel per six input channels is used to transfer the data to an FPGA at rates up to 600Mbit/s. This prototype ASIC allows the connection of up to 72 input channels.

A new readout PCB has been designed, featuring a Virtex-4 FPGA and a USB2 connection for data transfer to a PC. It can provide all necessary steering signals for the Switcher3 and DCD2 chips, while also providing the connectivity for future beam test efforts. A burst data rate of 14.4Gbit/s per 144 DCD2 input channels is supported. An additional focus is the implementation and testing of algorithms for zero suppression and data manipulation.

Additionally, a new Hybrid PCB has been designed, hosting one DCD2 and two Switcher3 chips. A 128x128 DEPFET matrix can be connected; optionally a 256x1024 DEPFET matrix can be used to evaluate the readout performance with higher input capacitance.

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