3D IC Pixel Electronics – *the next challenge*

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Outline

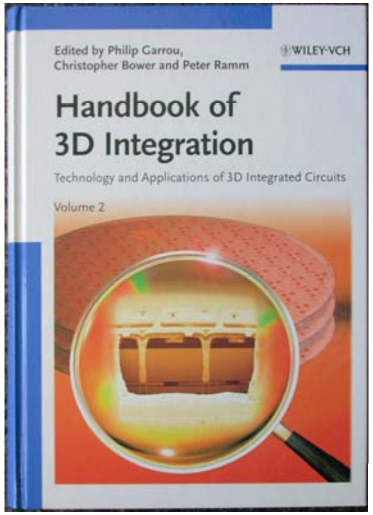
- The Reasons for 3D Integration
- Principles of 3D
- 3D Activities in HEP
- Lessons and a Path Forward

The Challenge

- There is no question that 3D integrated circuit design will play an important role in the continuing development of high performance integrated circuits. Will HEP be prepared to take advantage of these new technological developments? - *that is the challenge that lies before us*

Definition of 3D Integration and Driving Factors for 3D

- The just released Handbook of 3D Integration defines 3D integration as "the vertical integration of thinned and bonded silicon integrated circuits with vertical interconnects between the IC layers."[1]
- 3D is now positioned to make significant improvements to major drivers for that are critical for the semiconductor industry
  - Better electrical performance
  - Lower power consumption
  - Form factor improvement
  - Lower cost
  - More functionality
  - Mixed technologies



Edited by Philip Garrou,
Christopher Bower and Peter Ramm

WILEY-VCH

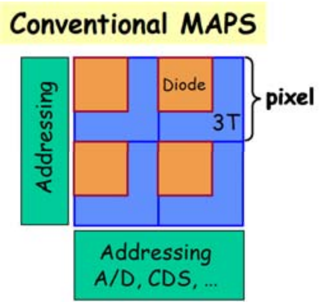
Handbook of
3D Integration

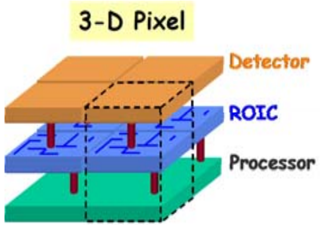
Technology and Applications of 3D Integrated Circuits

Volume 2

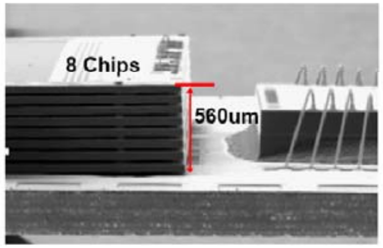
Major Markets being Pursued by Industry for 3D integration[1]

- Pixel arrays for imaging
  - Pixel arrays with sensors and readout are well suited to 3D integration since signal processing can be placed close to the sensor. Current 2D approaches cannot handle the data rate needed for high speed imaging.
- Memory
  - All major memory manufactures are working on 3D memory stacks. Significant cost reductions can be expected for large memory devices. The cost of 3D can be significantly less than going to a deeper technology node.[2]


Conventional MAPS
Addressing
Diode
3T
pixel
Addressing
A/D, CDS, ...


3-D Pixel
Detector
ROIC
Processor

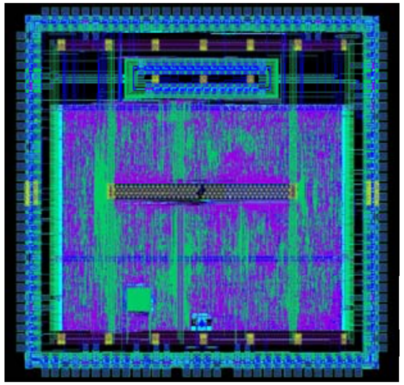
< NAND 8 Stacked Memory Card >

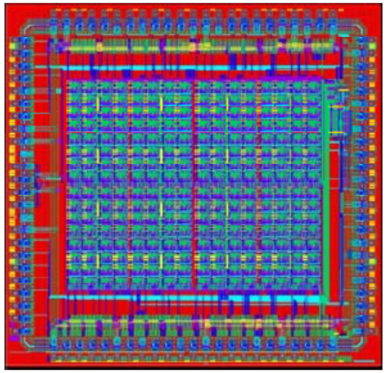

8 Chips
560um

(Samsung)

Major Markets being Pursued for 3D

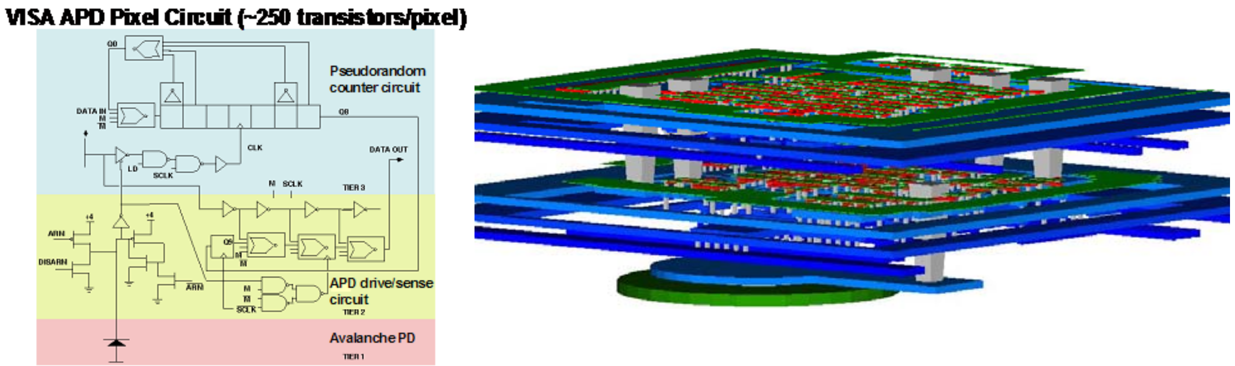
- Microprocessors
  - A major bottleneck is access time between CPU and the memory. Memory caches are used as an interface but the area required is significant. Initial applications for 3D will use Logic to Memory, and Logic to Logic stacking. Intel is claiming terabyte transfer rates between stacked memory and multicore processors is possible.
- FPGAs
  - Wire delays are an inherent problem is 2D FPGAs. 3D integration can improve performance by removing the programmable interconnect from the logic block layer and moving it to another tier.


CPU and 220 MHz memory Stack (Tezzaron)

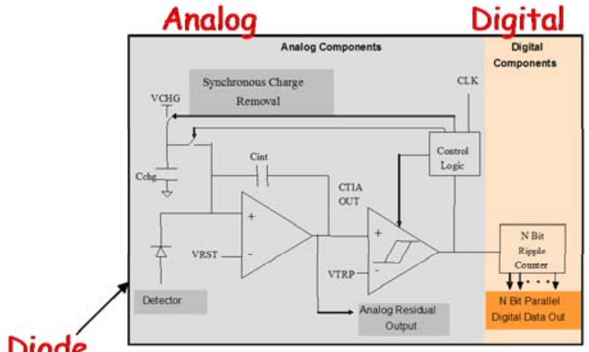

FPGA – 12 vertical interconnects per logic block (Tezzaron)

Areas of Interest to HEP

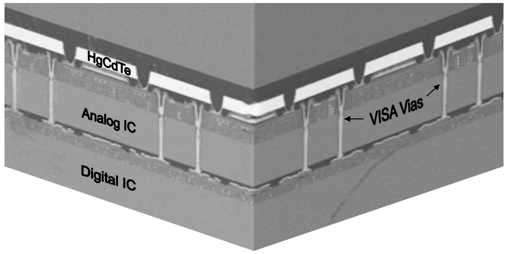
- 3D Pixel arrays with high functionality and smaller form factor for particle tracking


VISA APD Pixel Circuit (~250 transistors/pixel)
Pseudorandom counter circuit
DATA IN
CLK
DATA OUT
LD
SCLK
TIER 3
ARM
DISARM
APD drive/sense circuit
TIER 2
Avalanche PD
TIER 1

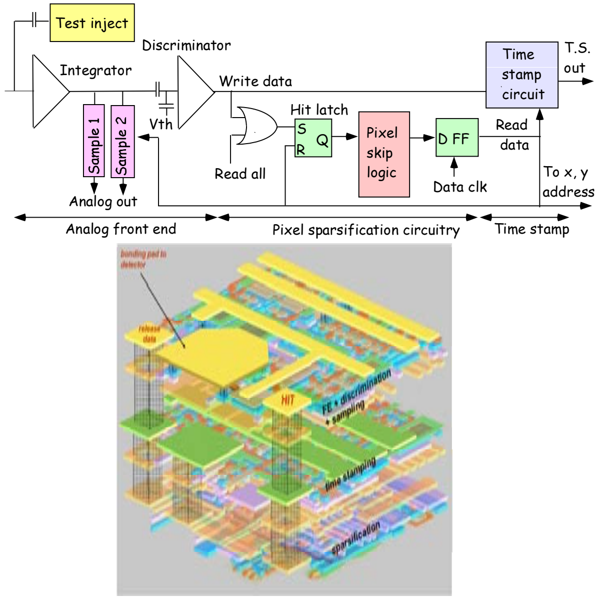
MIT LL 3D Laser Radar imager[3]


Analog
Digital
Analog Components
Digital Components
Synchronous Charge Removal
VCHG
CLK
Control Logic
Cint
Cchg
CTIA OUT
VRST
VTRP
N Bit Ripple Counter
Detector
Analog Residual Output
N Bit Parallel Digital Data Out
Diode

3 Tier circuit diagram


HgCdTe
Analog IC
VISA Vias
Digital IC

256 x 256 Infrared Pixel Array[4]

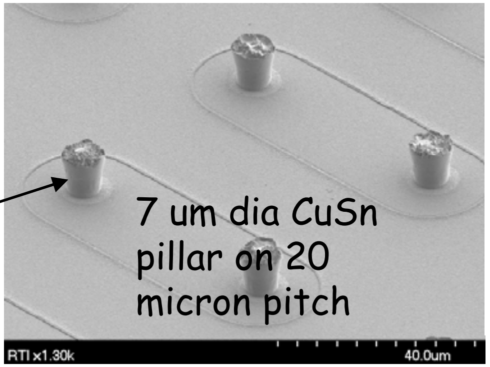

Test inject
Discriminator
Integrator
Write data
Time stamp circuit
T.S. out
Hit latch
S
Q
R
Pixel skip logic
D FF
Read data
Sample 1
Sample 2
Vth
Read all
Data clk
To x, y address
Analog out
Analog front end
Pixel sparsification circuitry
Time stamp
bonding pad to detector
HIT
FE + discrimination + sampling
time stamping
sparsification

Fermilab ILC Pixel Chip – VIP1[5]

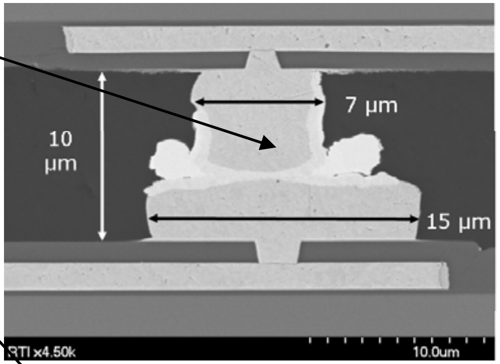
3.3 Mpixel CMOS camera.
To be described at Pixel 2008 (Tezzaron)

Areas of Interest to HEP

- 3D bonding technology to replace bump bonds in hybrid pixel assemblies.
- Bonding options being explored by Fermilab
  - CuSn eutectic with RTI[6]
  - Direct bond interconnect (DBI) using "magic metal" with Ziptronix. 3um pitch possible
  - CuCu fusion with Tezzaron
- Excellent strength and yield obtained with 7 um CuSn pillar on a 20 micron pitch. However 10 um of CuSn covering 75% of bond area would represents Xo=0.075. Too high for some HEP applications.
- CuCu fusion and DBI offer the lowest mass bond required by many HEP experiments.

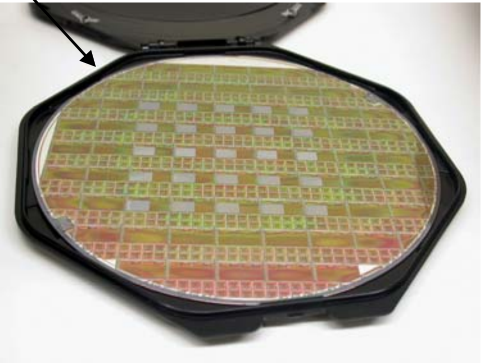


7 um dia CuSn pillar on 20 micron pitch



CuSn bond cross section

25 Pixel sensors bonded to BTEV ROIC wafer



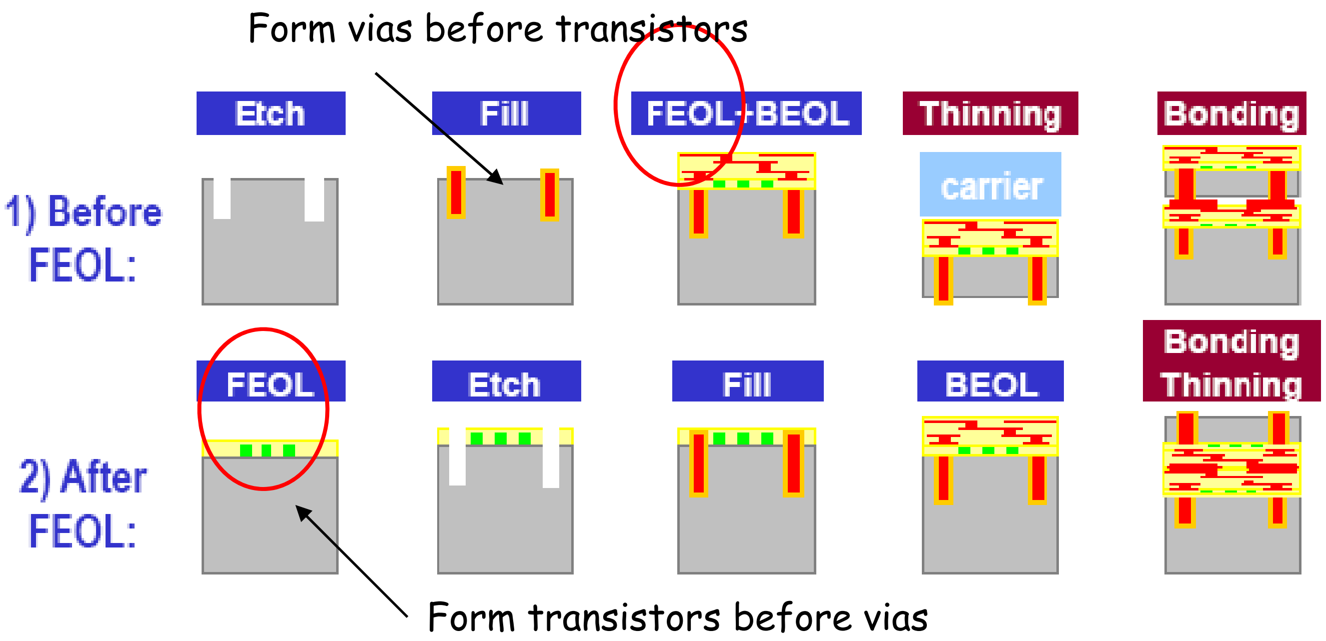
Sensors thinned to 100 um after chip to wafer bonding

Understanding the Basic Principles of 3D Integration

- Vias
  - Via First – done at foundry, lowest cost
  - Via last – after wafers are made, often done by third party vendors.
  - General movement in industry toward via first approach
- Bonding options
  - Mechanical bond only, electrical connections later
    - Oxide to oxide bonding
    - Adhesive such as BCB
  - Mechanical and electrical connection formed together
    - CuSn Eutectic
    - CuCu Fusion
    - Direct Bond Interconnect – combination of oxide bonding and metal fusion
- Thinning
- Alignment

Via First Approach

- Through silicon Via formation is done either before or after CMOS devices (Front End of Line) processing [7]



Form vias before transistors

1) Before FEOL:

Etch → Fill → FEOL+BEOL → Thinning (carrier) → Bonding

2) After FEOL:

FEOL → Etch → Fill → BEOL → Bonding Thinning

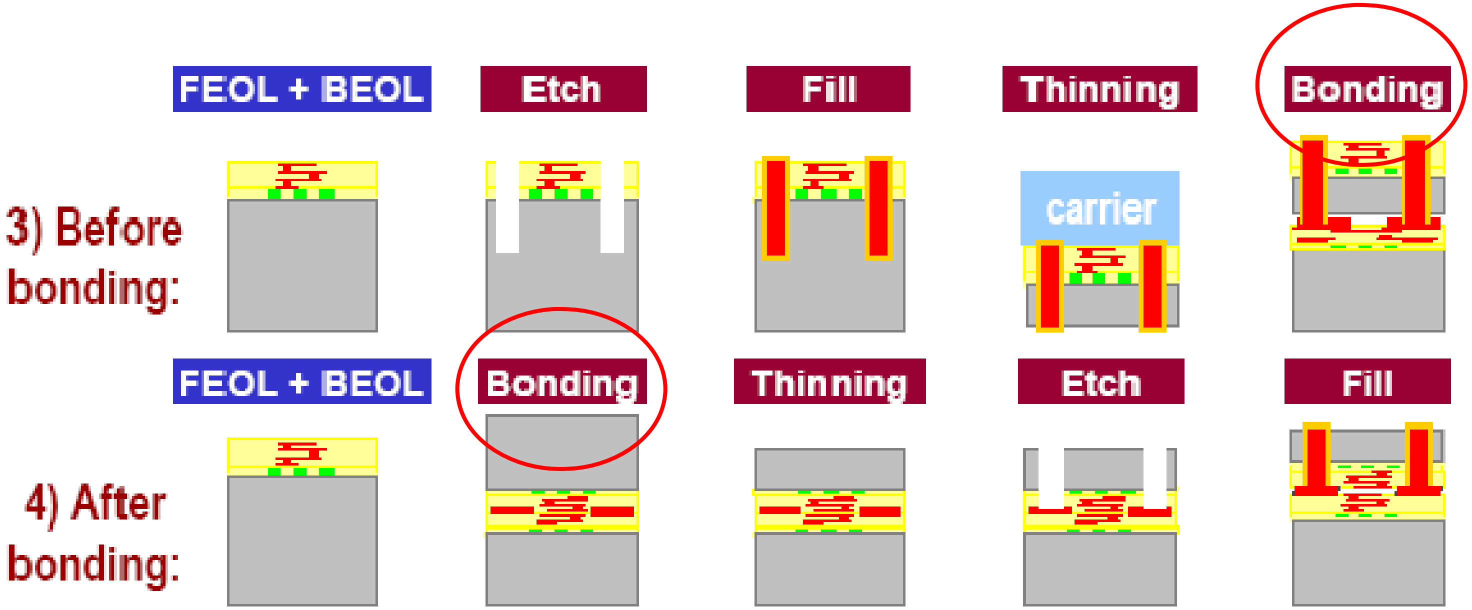
Form transistors before vias

IBM, NEC,
Elpida, OKI,
Tohoku, DALSA….

Tezzaron, Ziptronix
Chartered, TSMC,
RPI, IMEC……..

Via Last Approach

- Via last approach occurs after wafer fabrication and either before or after wafer bonding [7]


FEOL + BEOL
Etch
Fill
Thinning
Bonding
3) Before bonding:
carrier
FEOL + BEOL
Bonding
Thinning
Etch
Fill
4) After bonding:

Zycube, IZM, Infineon, ASET…

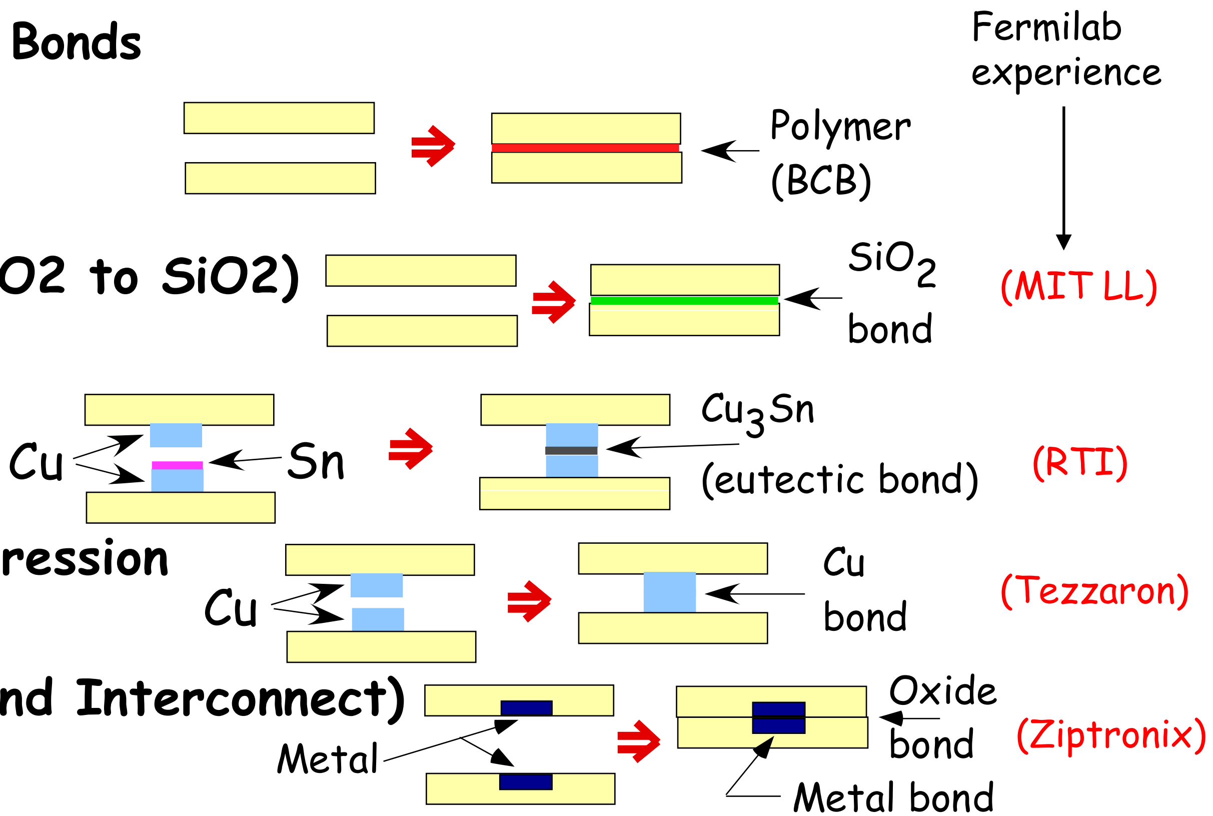
Samsung, IBM, MIT LL, RTI, RPI….

Notes: Vias take space away from all metal layers. The assembly process is streamlined if you don’t use a carrier wafer.

Bonding Choices

Electrical and Mechanical Bonds

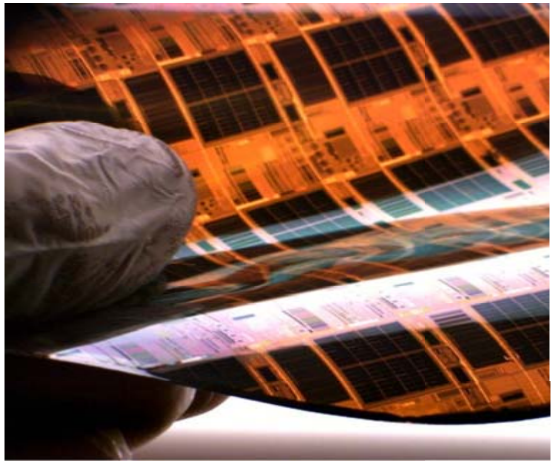
- a) Adhesive bond
- b) Oxide bond (SiO2 to SiO2)
- c) CuSn Eutectic
- d) Cu thermocompression
- e) DBI (Direct Bond Interconnect)


Fermilab experience
Polymer (BCB)
SiO_2 bond
(MIT LL)
Cu
Sn
Cu_3Sn (eutectic bond)
(RTI)
Cu
Cu bond
(Tezzaron)
Metal
Oxide bond
Metal bond
(Ziptronix)

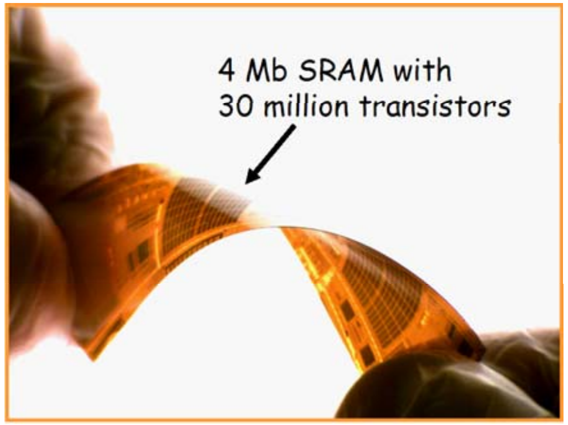
For (a) and (b), electrical connections between layers are formed after bonding. For (c), (d), and (e), the electrical and mechanical bonds are formed at the same time.

Thinning and Alignment

- Thinning –
  - Thinning is done by a combination of grinding, CMP and etching.
  - Through wafer vias typically have an 8 to 1 aspect ratio for etched vias. Thus, in order to keep the area associated with the vias as small as possible, the wafers should be as thin as possible.
- Alignment
  - Alignment of better than 1 um (3 sigma) is now possible on wafer to wafer bonding.



6 inch wafer thinned to 6 um and mounted to 3 mil kapton



4 Mb SRAM with 30 million transistors

Photos from MIT LL

Growing Activity for HEP

- First 3D integrated circuit for HEP submitted by Fermilab to MIT Lincoln Labs October, 2006.
- 3D Integration Technology Perspectives – First Workshop on LHC – ILC Prospects, Ecole Polytechnique, Palaiseau, France. November 29-30, 2007, sponsored by CNRS/IN2P3.[8]
- Vertical Integration Technologies for HEP and Imaging Sensors Meeting held at Ringberg Castle, Tegernsee, Germany, April 6-9, 2008, sponsored by the Max Planck Insitiute. [9]
- DEVDET FP7 proposal did not receive funding but 3D portion of proposal effort received positive comments from reviewers.

Growing Activity for HEP

- Italian programs
  - Italian Ministry of Research program on 2D MAPS and Vertically Integrated Sensors (Pisa, Pavia, Bergamo, Bologna)
    - Focus on device and technology investigations rather than experiments
    - 2 year program starting in September 2008
    - P.I. - M. Giorgi (Pisa)
  - Proposal for INFN research program “Pixel systems for thin charged particle trackers based on vertical integration technologies” - VIPIX (INFN Pisa, Pavia, bologna, Trieste, Trento, Perugia, Roma3, Torino)
    - 3 year program starting in September 2008
    - For ILC and Super B
    - P.I. – Valerio Re (Pavia)
    - 800K Euros

Growing Activity for HEP

- French Activities
  - Meeting at Palaiseau, France 2007 resulted in collaboration for development of vertically integrated circuits.
    - 5 HEP related labs in France expected to participate
      - CPPM
      - IPHC
      - IRFU
      - LAL
      - Paris
    - Funding from IN2P3, 200K Euros initially
    - Coordinated by Jean-Claude Clemens
  - Expected applications
    - ILC smart CMOS pixels and ministrips
    - SLHC with hybrid pixels
    - Spin off to imaging applications

Growing Activity for HEP

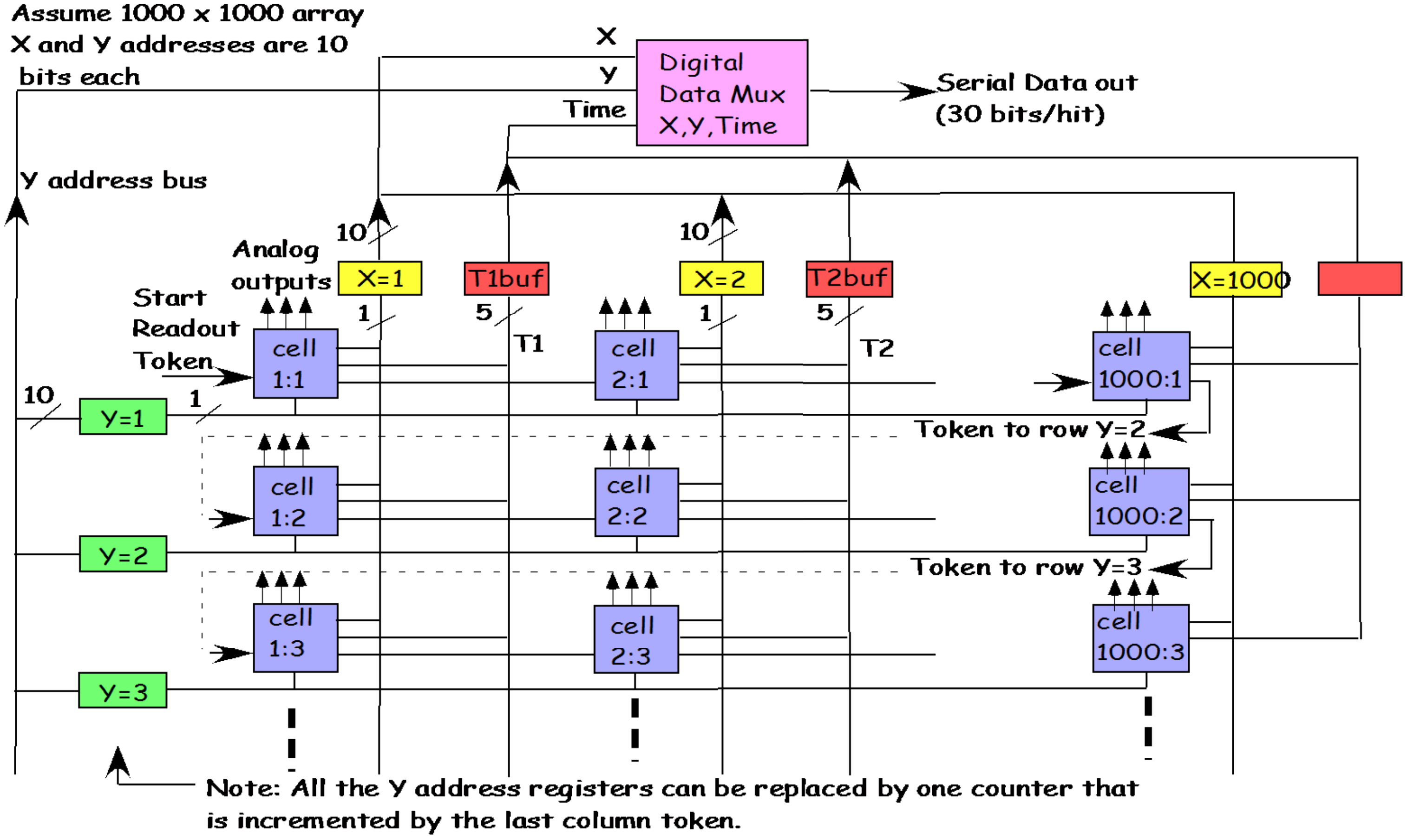
- Second 3D integrated circuit for HEP submitted by Fermilab to MIT Lincoln Labs, September 2008.
- 3D collaboration coordinated by Fermilab for vertically integrated circuits through Tezzaron, Naperville, Illinois.
  - Multi-project wafer run using commercial vendors
  - Two stacked circuits with deep N-well capability.
  - Up to 10 fully integrated 3D wafers in 0.13 um process
  - Submission targeted for early 2009
  - Tezzaron MPW run to be discussed in greater detail later in this talk.
- Monolithic And Vertically Integrated Silicon Pixel Detectors proposal by Chris Damerell for an international collaboration.

VIP1 Demonstrator Chip for ILC Vertex Detector

- 3D Pixel ROIC fabricated in the MIT LL 0.18 um SOI process with 3 tiers (first 3D chip for HEP).
  - Chip designed in 10 weeks using 4 designers
  - Forced to work with poor SOI models and had to develop design kit at same time. (extremely ambitious project)
- Details of VIP1 chip design and operation presented at 12th LHC electronics workshop[11]
  - Readout between ILC bunch trains
  - High speed data sparsification included
  - Analog output available for improved resolution
  - Digital and analog time stamping options explored
    - Designed for 5-10 bit resolution (30-1 usec resolution)
  - Test input for every pixel
  - 4096 pixel array with 20 um pixels, scaleable to 1 Mpix

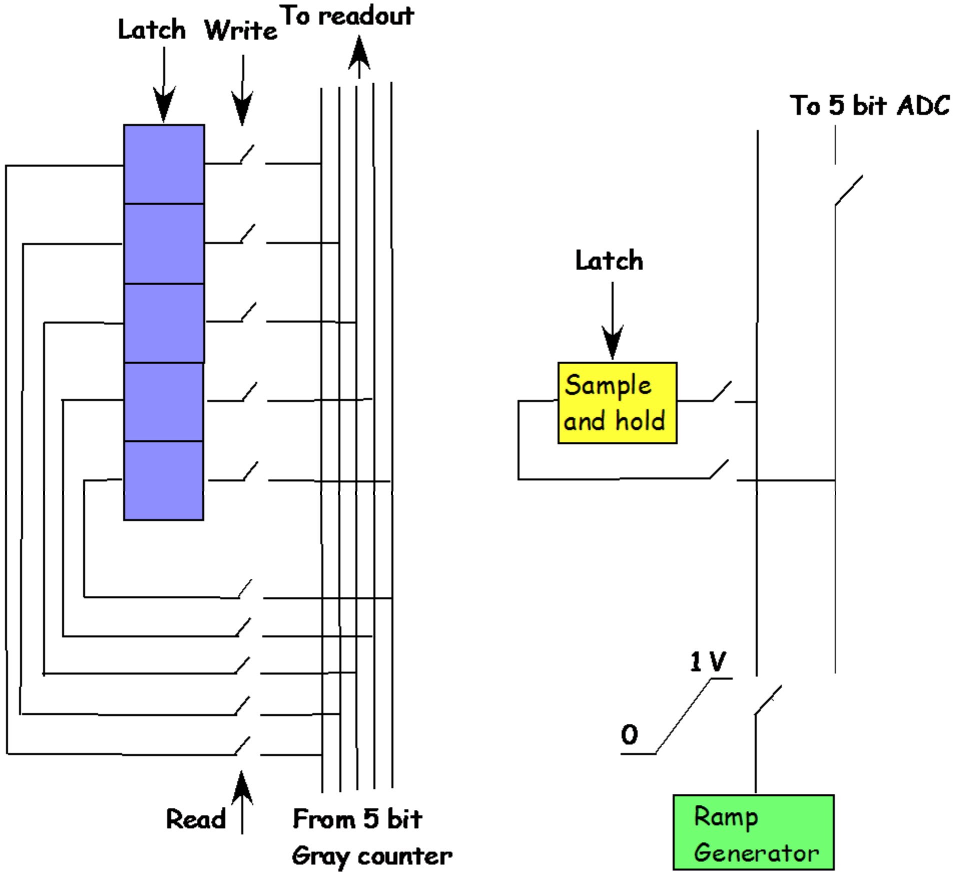
VIP1 Block Diagram

- Pixel being read points to the x address and y address stored on the perimeter.
- At same time, time stamp information and analog pulse height is read out.
- During pixel readout, token scans ahead for the next hit pixel


Assume 1000 x 1000 array
X and Y addresses are 10 bits each
X
Y
Time
Digital Data Mux X,Y,Time
Serial Data out (30 bits/hit)
Y address bus
10
10
Analog outputs
Start Readout Token
X=1
T1buf
X=2
T2buf
X=1000
1
5
1
5
T1
T2
cell 1:1
cell 2:1
cell 1000:1
10
Y=1
1
Token to row Y=2
cell 1:2
cell 2:2
cell 1000:2
Y=2
Token to row Y=3
cell 1:3
cell 2:3
cell 1000:3
Y=3
Note: All the Y address registers can be replaced by one counter that is incremented by the last column token.

VIP1 Time Stamping

- Various schemes have suggested 20 time stamps/msec for ILC vertex detector.
- VIP1 is built to evaluate both digital and analog time stamping, each with 5 bit resolution (32 time stamps/msec).
- Combined analog and digital time stamping could provide 10 bit resolution (1024 time stamps/msec)


Latch
Write
To readout
Read
From 5 bit
Gray counter
To 5 bit ADC
Latch
Sample and hold
1 V
0
Ramp Generator

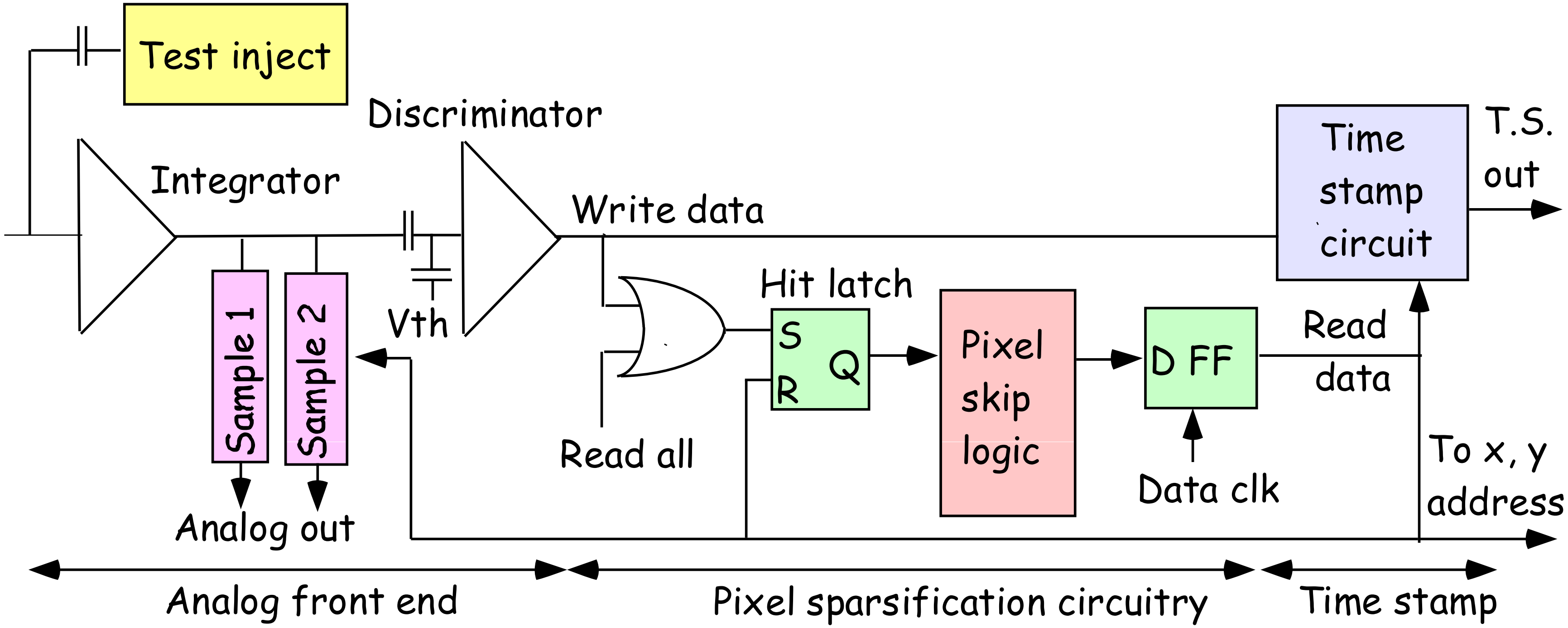
Counter operates at a slow speed, 32 KHz, (30 usec/step)

All digital - 10 transistors/bit

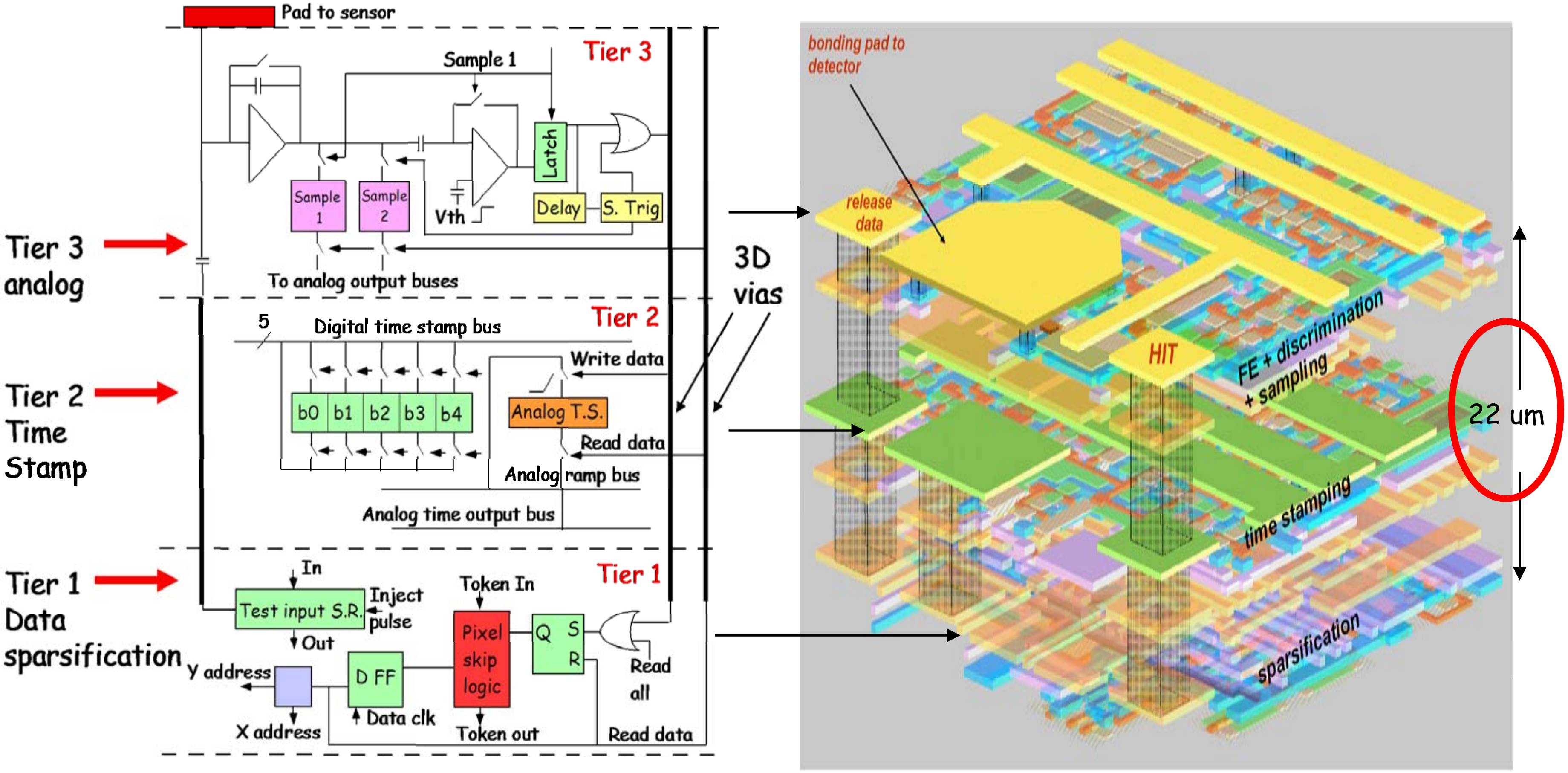
Ramp operates at low speed for low power.

Analog approach - fewer transistors

Simplified VIP1 Pixel cell Block Diagram


Test inject
Discriminator
Integrator
Write data
Time stamp circuit
T.S. out
Sample 1
Sample 2
Vth
Hit latch
S
R
Q
Pixel skip logic
D FF
Read data
Data clk
Read all
To x, y address
Analog out
Analog front end
Pixel sparsification circuitry
Time stamp

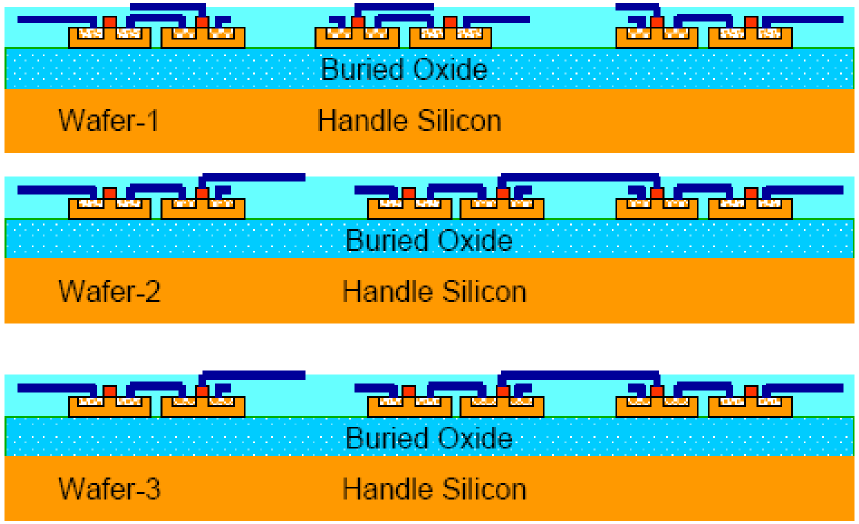
Three Tier Arrangement for VIP1 Pixel


Pad to sensor
Tier 3
Sample 1
Latch
Sample 1
Sample 2
Vth
Delay
S. Trig
To analog output buses
Tier 3 analog
Tier 2
5
Digital time stamp bus
Write data
b0
b1
b2
b3
b4
Analog T.S.
Read data
Analog ramp bus
Analog time output bus
Tier 2 Time Stamp
Tier 1
In
Test input S.R.
Inject pulse
Out
Token In
Pixel skip logic
Q
S
R
Read all
Y address
D FF
Data clk
X address
Token out
Read data
Tier 1 Data sparsification
3D vias
bonding pad to detector
release data
HIT
FE + discrimination + sampling
time stamping
sparsification
22 um

MIT LL 3DM2 Vertical Integration Process Flow

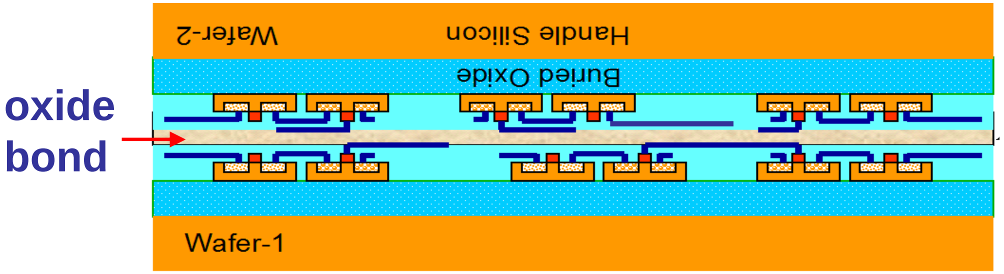
"Via last" process – vias are formed after FEOL and BEOL processing is completed

Step 1: Fabricate individual tiers

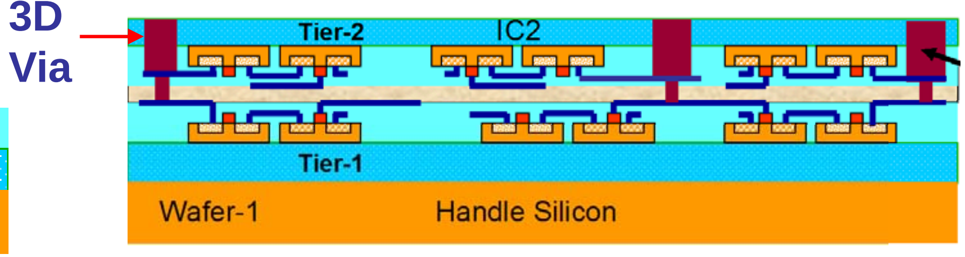

Buried Oxide
Wafer-1
Handle Silicon
Buried Oxide
Wafer-2
Handle Silicon
Buried Oxide
Wafer-3
Handle Silicon

In principle wafer 1 could also be bulk

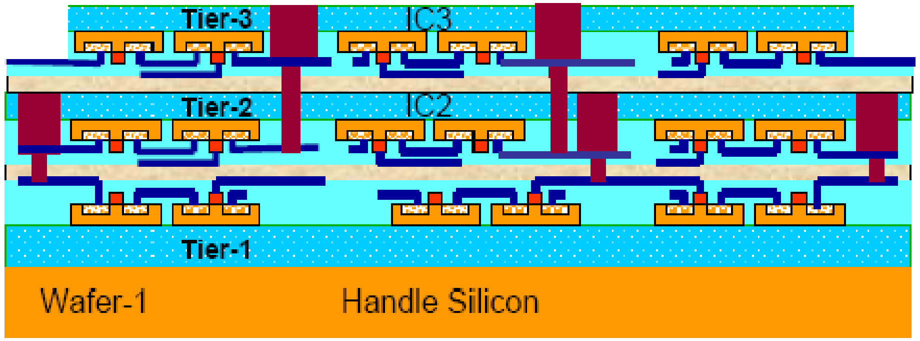
Step2: Invert, align, and bond wafer 2 to wafer 1


Wafer-2
Handle Silicon
Buried Oxide
oxide bond
Wafer-1

Step 3: Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten


3D Via
Tier-2
IC2
Tier-1
Wafer-1
Handle Silicon

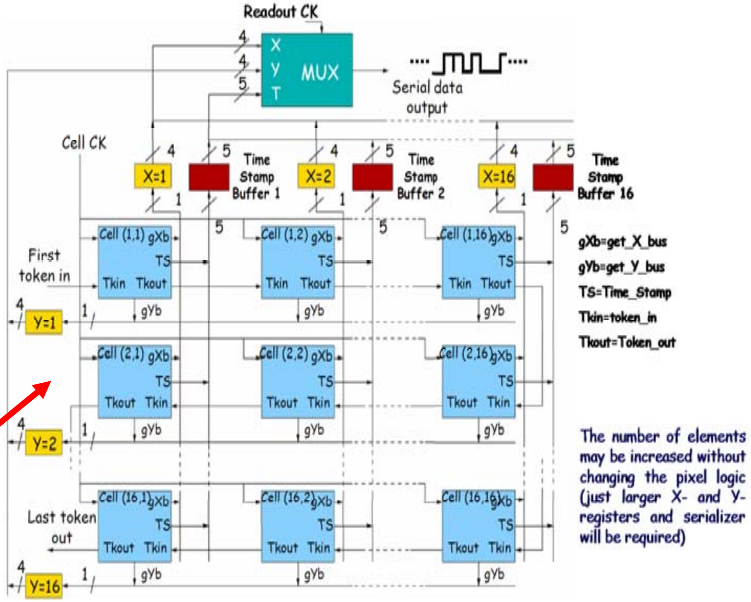
Step 4: Invert, align and bond wafer 3 to wafer 2/1, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3, etch bond pads


Tier-3
IC3
Tier-2
IC2
Tier-1
Wafer-1
Handle Silicon

TWE

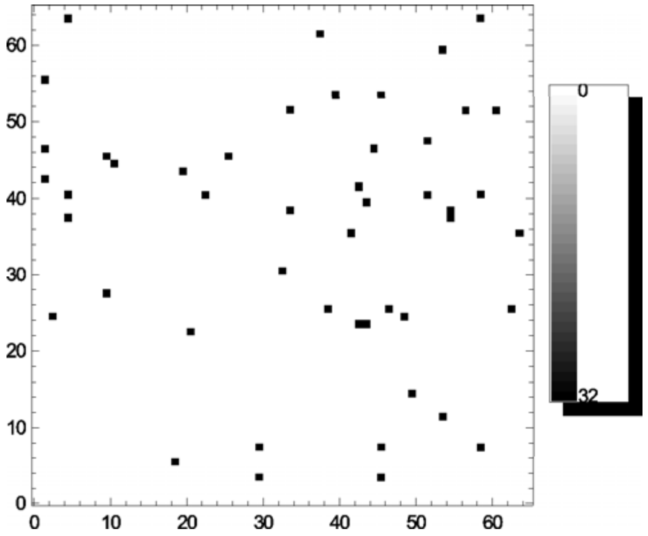
VIP1 Test Results[12]

- Basic functionality of chip has been demonstrated
  - Propagation of readout token
  - Threshold scan
  - Input test charge scan
  - Digital and analog time stamping
  - Full sparsified data readout
  - Fixed pattern and temporal noise measurements
- No problems could be found associated with the 3D vias between tiers.
- Chip performance compromised by poor transistor models and low yield.
- Same readout architecture (without analog time stamping and analog output information) has been demonstrated to work by Valerio Re in a ST Microelectronics 0.13 um, 2D MAPS design. [13]

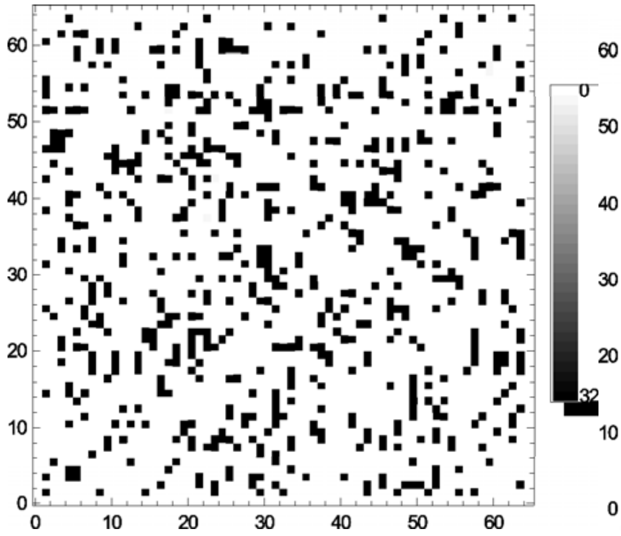

Readout CK
X
Y
T
MUX
4
4
5
Serial data output
Cell CK
X=1
X=2
X=16
Time Stamp Buffer 1
Time Stamp Buffer 2
Time Stamp Buffer 16
First token in
Last token out
Cell (1,1)
Cell (1,2)
Cell (1,16)
Cell (2,1)
Cell (2,2)
Cell (2,16)
Cell (16,1)
Cell (16,2)
Cell (16,16)
gXb
TS
Tkin
Tkout
gYb
Y=1
Y=2
Y=16
1
gXb=get_X_bus
gYb=get_Y_bus
TS=Time_Stamp
Tkin=token_in
Tkout=Token_out
The number of elements may be increased without changing the pixel logic (just larger X- and Y- registers and serializer will be required)

Hit Pixels in Full Array as a Function of Threshold

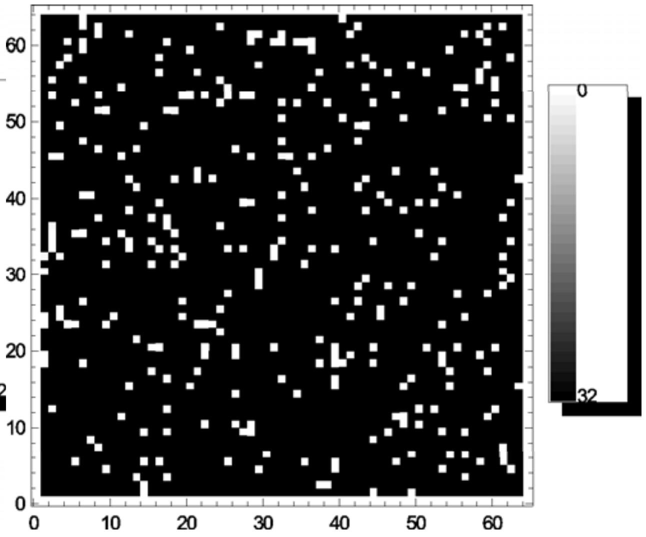
Data readout out using data sparsification scheme.



Maximum threshold



Intermediate Threshold



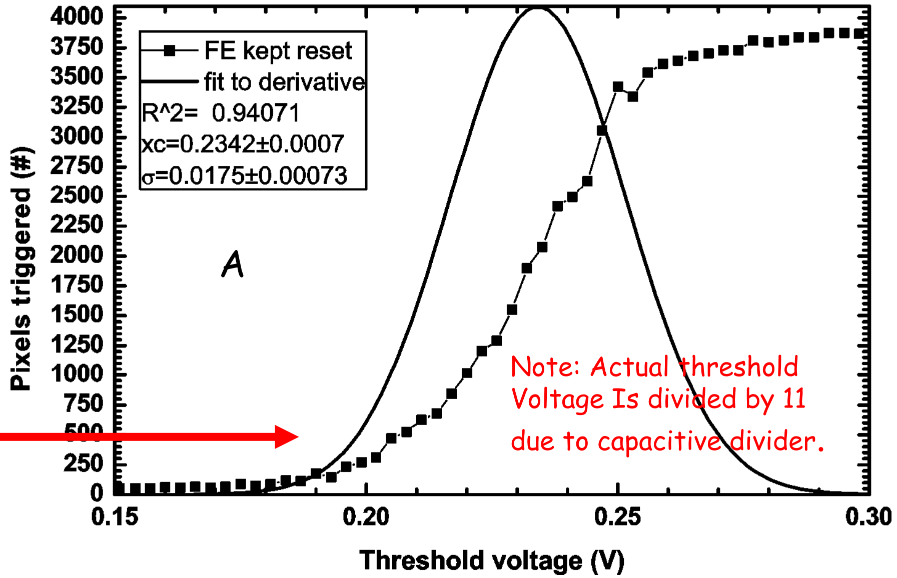
Minimum Threshold

Decreasing Threshold

Pixel to Pixel Threshold Dispersion Scan

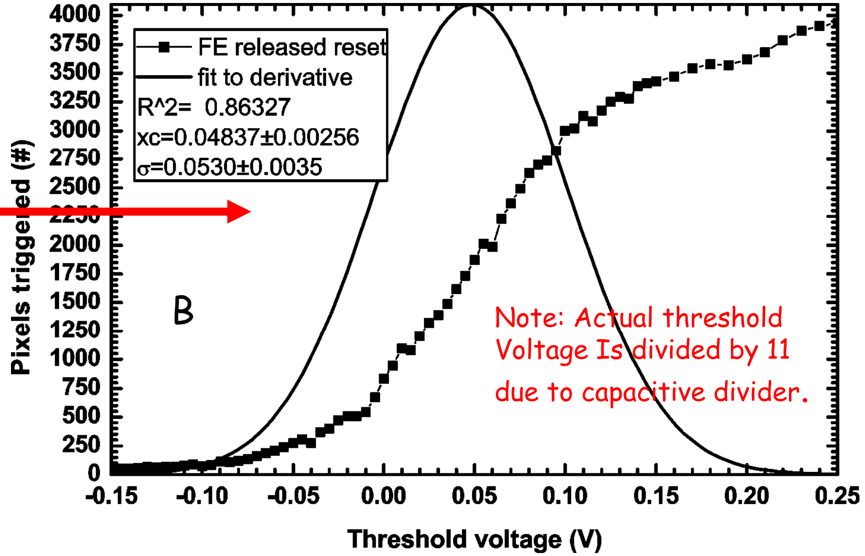
Threshold set at increasing levels and all pixels over threshold read out using data sparsification scheme.

A) With integrator held reset, threshold dispersion has a sigma of 1.6 mv or about 25e-.



Note: Actual threshold Voltage Is divided by 11 due to capacitive divider.

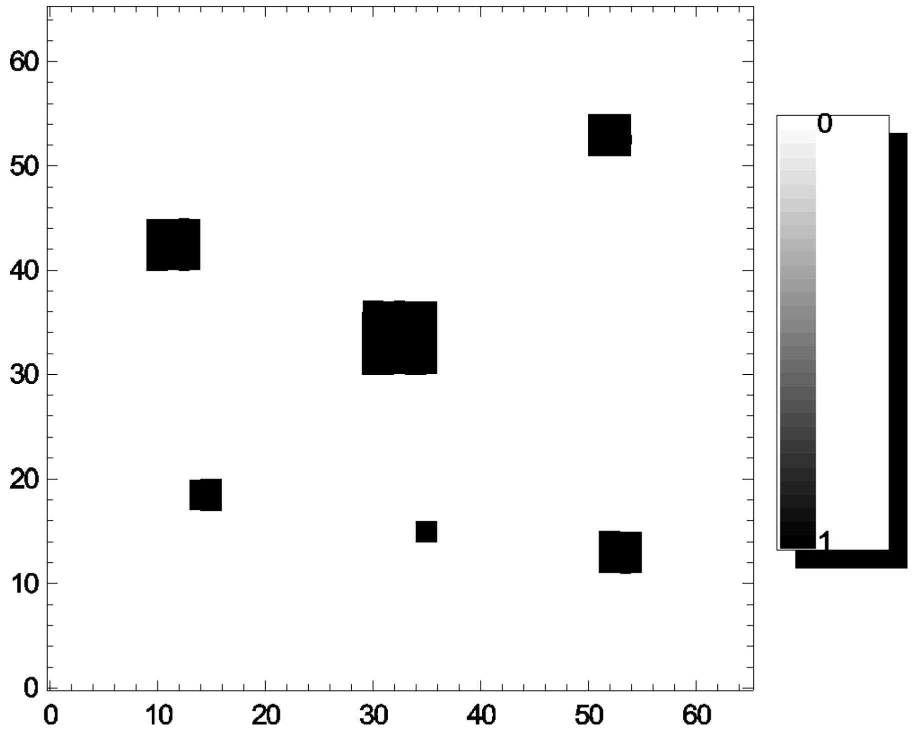
B) With integrator reset and released, discriminator reset (autozeroed), threshold dispersion has a sigma of 4.9 mv or about 75 e-.



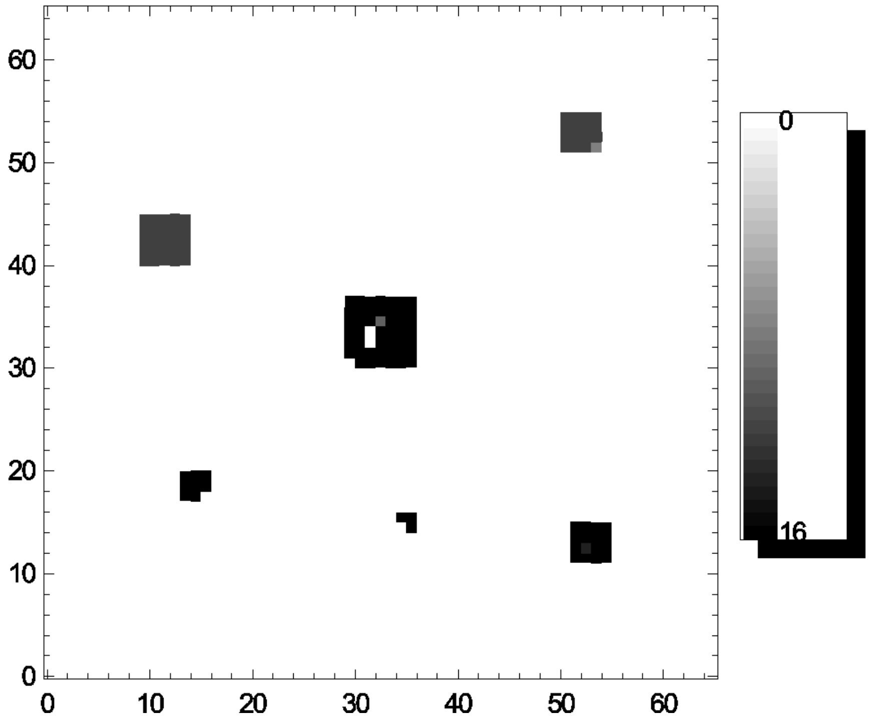
Note: Actual threshold Voltage Is divided by 11 due to capacitive divider.

The threshold shift between A and B and the increase in dispersion is thought to be due to internal coupling problems.

Injection of Test Charge into 119 Integrator Inputs of 64 x 64 Array



Preselected pattern of pixels for the injection of signal to the front-end amplifiers; pattern shifted into the matrix, than positive voltage step applied accross the injection capacitance; threshold levels for the discriminator adjusted according to the amplitude of the injected signal

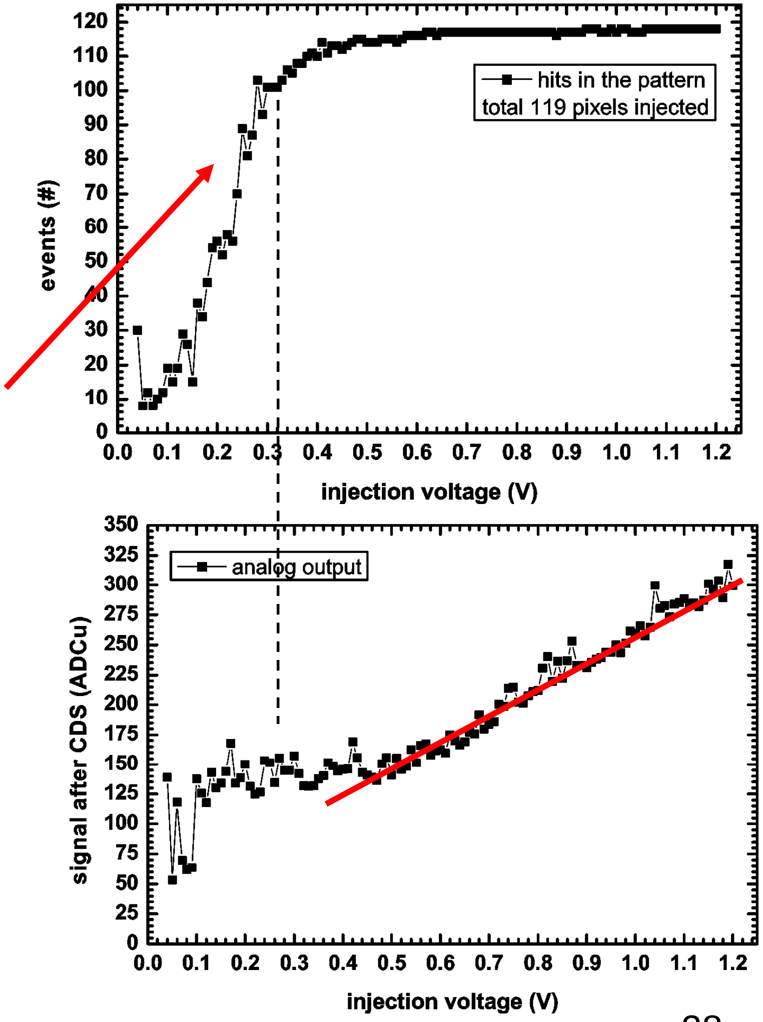


Pattern of pixels from the preselected injection pattern that after injection of tests charge reported as hit (grey level represents number of repetition – 8 times injection)

Analog Signal Response from Pixels in Test Pattern

Examine analog response for 119 pixels in preselected pattern using sparsified readout.

As level of test charge through test capacitor (located between tier 2 and 3) is increased, more pixels exceed the threshold up to the maximum of 119 pixels



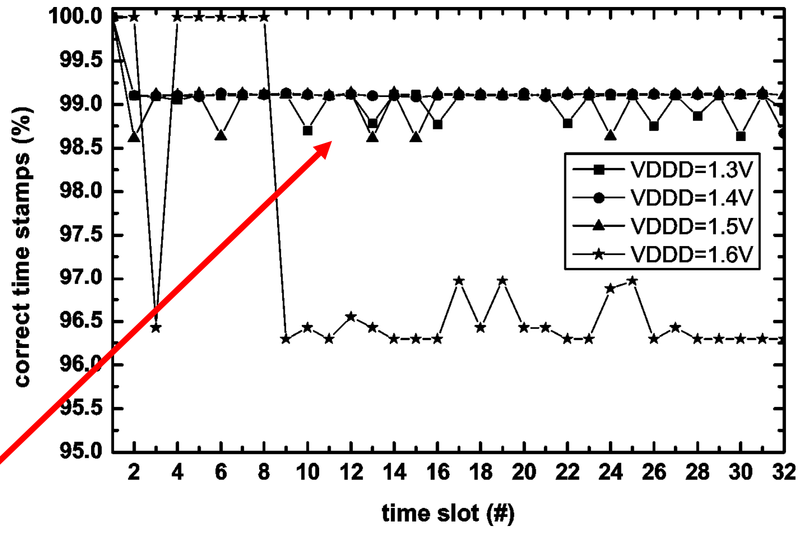
Lower plot shows mean analog signal level of pixels exceeding the threshold voltage. The red line is an indication of the linearity of the analog output signal (100 ADC units = 35 mv). Note charge injection capacitor = 0.2 fF

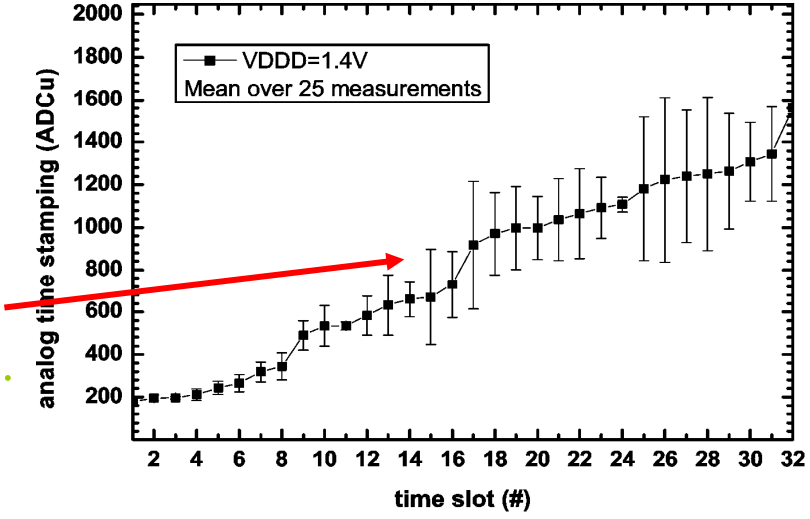
Time Stamping Performance

Time stamping studied for 119 pixels in preselected pattern using sparsified readout. Digital time stamping uses inverted Gray code. External ADC used for analog time stamp

Charge is injected at a specific time, and time is compared to the digital time stamp. The readout shows a dependence on VDDD. Data shows that 118 of 119 pixels have correct time stamp for VDDD = 1.4V.

Analog time stamping suffers from high leakage current in sample and hold circuit. Problem to be corrected in next submission.





New Submission to MIT LL

- Work is proceeding on an improved version of VIP1 to be submitted to MIT LL at the end of September 2008. The new chip is called VIP2a
  - Different power and grounding layout
  - Redundant vias and larger traces in critical paths
  - Added diagnostics
  - More bits in digital time stamp (7 bits)
  - Redesign of current mirrors
  - Removal of dynamic logic due to leakage problems
  - Other
- VIP2 has a larger pixel size. However, the goal is for improved yield and better performance.

Lessons Learned

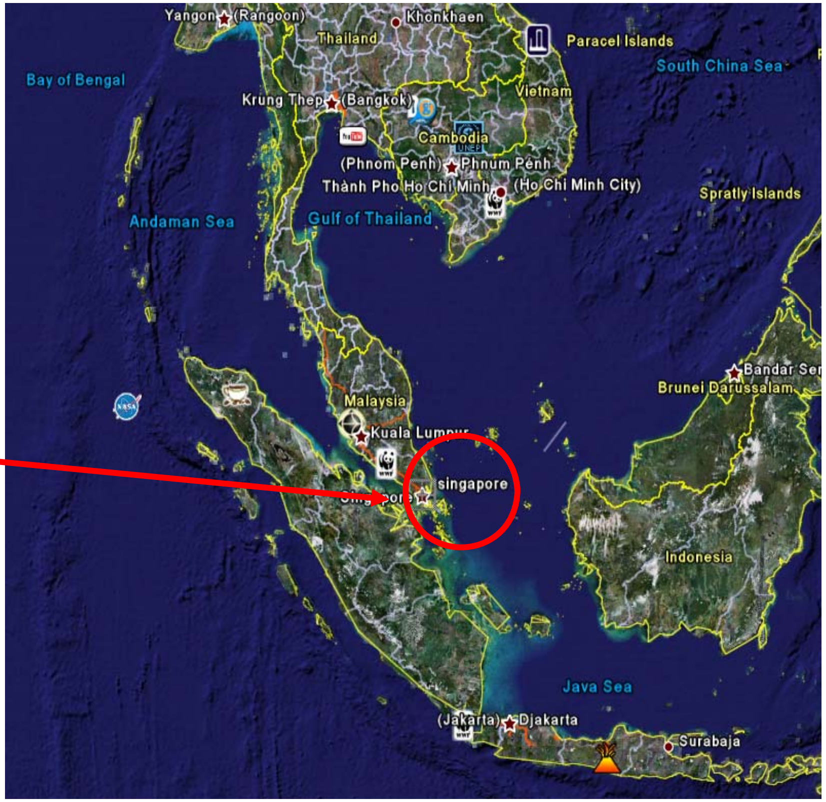
- If possible work with an organization that can provide all steps of 3D fabrication (wafer fab, via formation, thinning, bonding)
  - Eliminates multi vendors, and reduces contamination, and breakage problems
  - Generally provides for established via and bonding layout rules
- If possible, work with commercial vendors
  - Unfortunately, there are not very many yet
  - Take advantage of industrial developments
  - Sources such as MIT LL have their limitations
    - Foundry process is not well characterized
    - Delivery takes one year
  - Chose a vendor that has access to an established reliable foundry process.
  - If you can find a vendor, you can get lower cost and faster overall turn around.
- For better analog performance circuits chose CMOS instead of SOI
  - Precision circuits such as current mirrors are hard to design in SOI due to possible trapped charge effects and local heating
  - CMOS will most likely be more radiation hard for those applications that require it.

Lessons Learned

- Understand that small scale fabrication is an issue since most 3D assembly require full wafer processing at some point.
  - Full wafer processing of sensors wafers should not be a problem for HEP
  - Access to wafers of ROICs can be expensive especially in deep submicron processes
  - If parts are limited, die to wafer assembly is possible
- Use of a via first process can eliminate wasted space for vias
- Cost of development can be a limiting factor depending on the avenue taken
  - Cost of MIT LL 3D MPW run is well in excess of $1M
  - Using a commercial vendor, 8 inch wafer to wafer assemblies in a 0.13 um process can be fabricated for under $300K
    - This cost can be easily shared among HEP organizations.
- Availability of MPW runs for HEP is important for development of 3D for HEP
  - One vendor Tezzaron has agreed to accept MPW runs from Fermilab
  - Tezzaron will fabricate wafers in a well established, high yield process

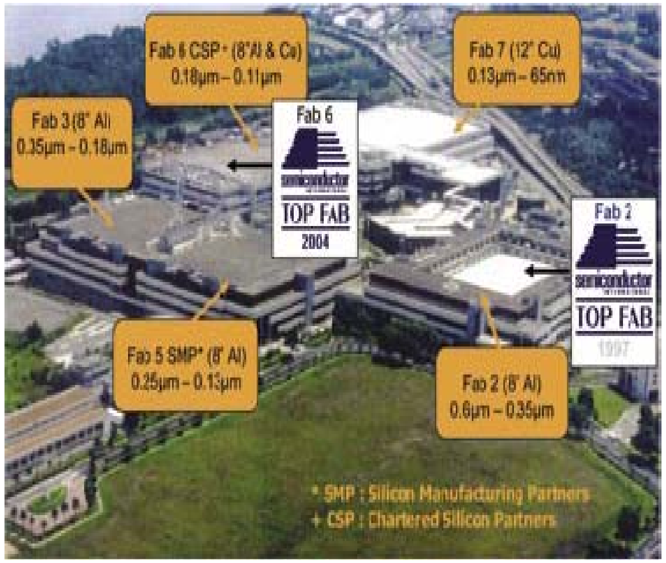
Why Tezzaron?

- Tezzaron is one of the leaders in developing 3D technology
- Tezzaron has built 3D devices for imaging, memory stacking, FPGAs, and microprocessors.
- Gearing up for 10,000w/mo in 18 months
  - Chips will include 2, 3 and 5 layer stacks of memories from 512 Mb to 4 Gb.
  - Customers are in the top 20 memory manufactures.
- Wafers are fabricated by Chartered in Singapore.
- 3D assembly is completed by Tezzaron also in Singapore
- Tezzaron expects announce their process being used by 1 to 3 more foundries by the end of the year
- Advantages
  - Existing rules for vias and bonding
  - Low cost
  - Relatively fast turn around
  - One stop shopping for wafer fabrication, via formation, thinning, bonding.


Yangon (Rangoon)
Khonkhaen
Thailand
Paracel Islands
South China Sea
Bay of Bengal
Krung Thep (Bangkok)
Vietnam
Cambodia
(Phnom Penh) Phnum Penh
Thanh Pho Ho Chi Minh (Ho Chi Minh City)
Spratly Islands
Andaman Sea
Gulf of Thailand
Bandar Ser
Brunei Darussalam
Malaysia
Kuala Lumpur
singapore
Indonesia
Java Sea
(Jakarta) Djakarta
Surabaja

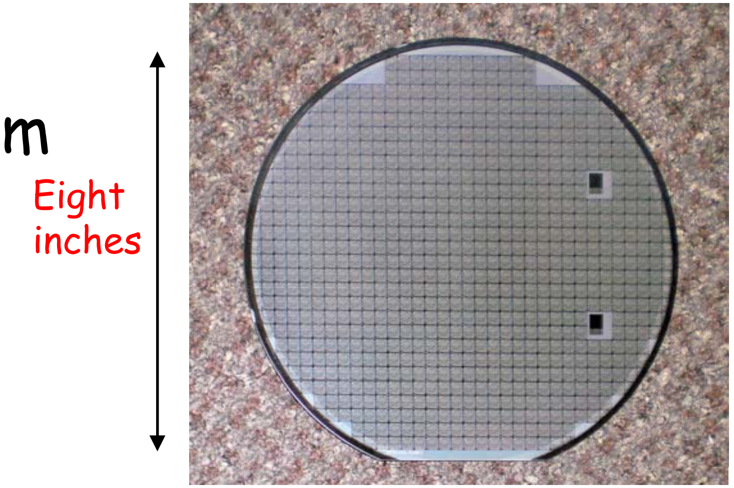
Why Chartered Semiconductor?

- Chartered is one of the world's top dedicated semiconductor foundries, located in Singapore, offering an extensive line of CMOS and SOI processes from 0.5 um down to 45 nm.
- Offers Common Chartered-IBM platform for processes at 90 nm and below.
- Chartered 0.13 um mixed signal CMOS process was chosen by Tezzaron for 3D integration
  - Chartered has made nearly 1,000,000 eight inch wafers in the 0.13um process
  - Data shows consistent high yield
- Extension of TSV process to 300mm wafers and 45nm technology
- Commercial tool support for Chartered Semiconductor is extensive
  - DRC – Calibre, Hercules, Diva, Assura
  - LVS - Calibre, Hercules, Diva, Assura
  - Simulation – HSPICE. Spectre, ELDO, ADS
  - Libraries – Synopys, ARM, Virage Logic


Fab 6 CSP+ (8" Al & Cu)
0.18µm – 0.11µm
Fab 7 (12" Cu)
0.13µm – 65nm
Fab 3 (8" Al)
0.35µm – 0.18µm
Fab 6
semiconductor
TOP FAB
2004
Fab 2
semiconductor
TOP FAB
1997
Fab 5 SMP* (8" Al)
0.25µm – 0.13µm
Fab 2 (8" Al)
0.6µm – 0.35µm
* SMP : Silicon Manufacturing Partners
+ CSP : Chartered Silicon Partners

Chartered Campus

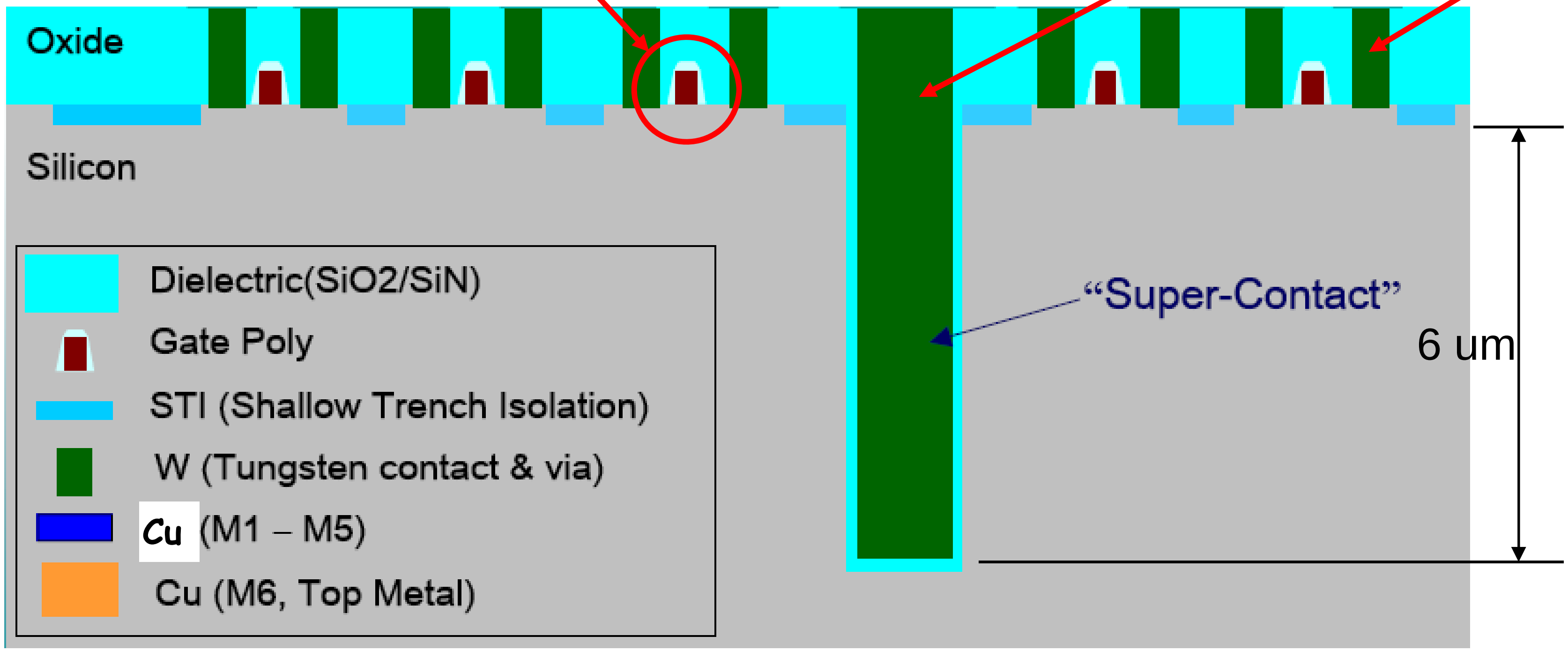
Chartered 0.13 um Process


Eight inches

- 8 inch wafers
- Large reticule – 24 mm x 32 mm
- Features
  - Deep N-well
  - MiM capacitors – 1 fF/um^2
  - Single poly
  - 8 levels of metal available
  - Zero Vt (Native NMOS) available
  - A variety of transistor options with multiple threshold voltages can be used simultaneously
    - Nominal
    - Low voltage
    - High performance
    - Low power

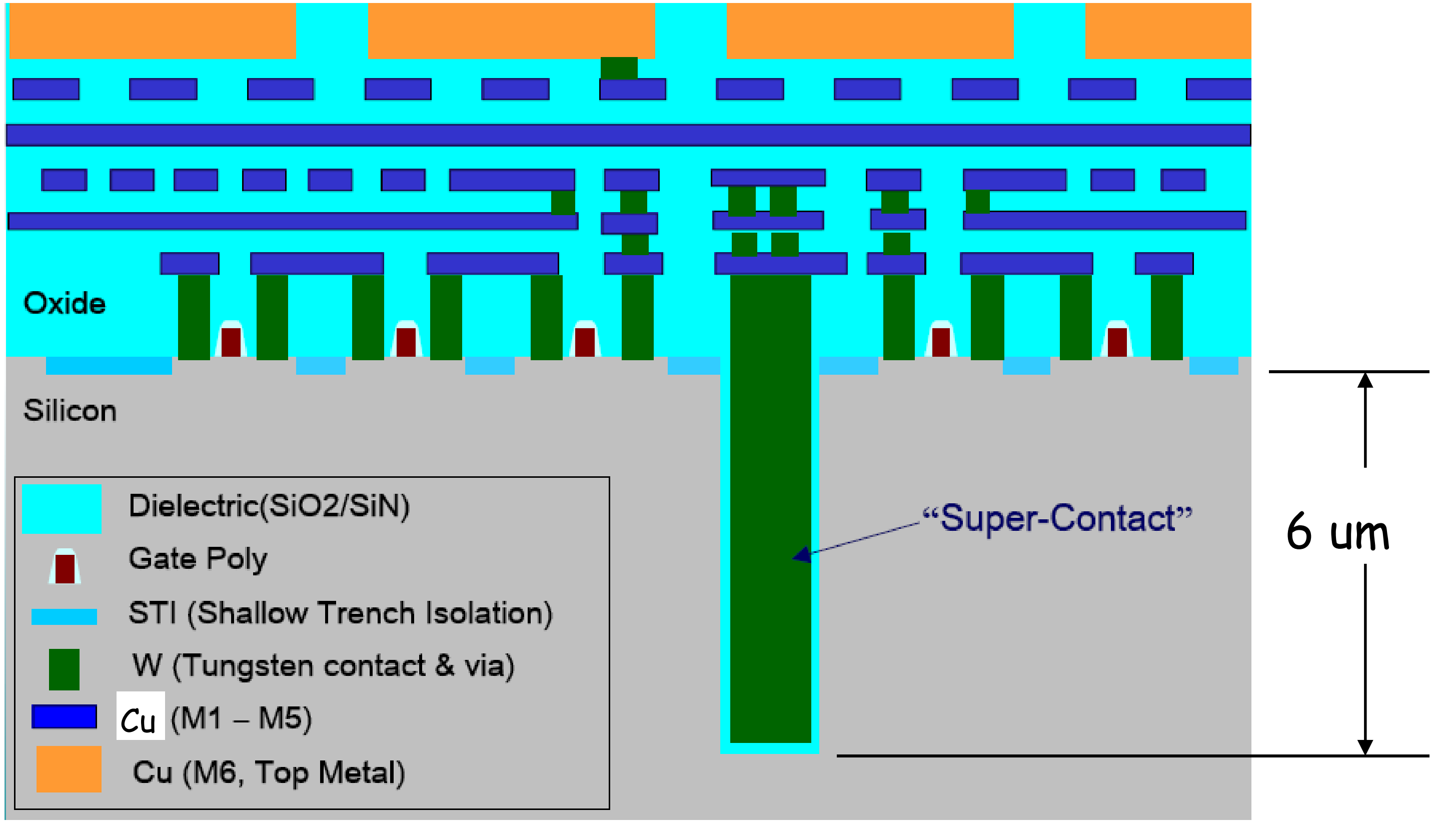
Tezzaron 3D Process[14]

- Through silicon vias are fabricated as a part of the foundry process. "Via first" approach.
- Complete FEOL (transistor fabrication) on all wafers to be stacked
- Form and passivate super via on all wafers to be stacked
- Fill super via at same time connections are made to transistors


Oxide
Silicon
Dielectric(SiO2/SiN)
Gate Poly
STI (Shallow Trench Isolation)
W (Tungsten contact & via)
Cu (M1 – M5)
Cu (M6, Top Metal)
"Super-Contact"
6 um

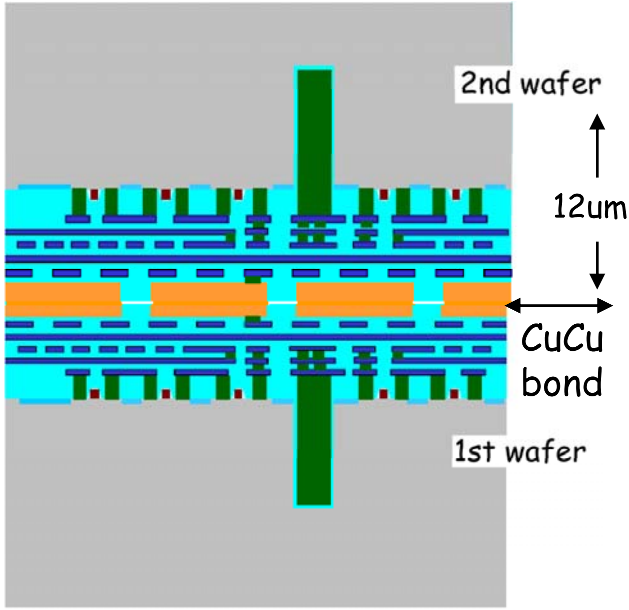
Tezzaron 3D Process

- Complete back end of line (BEOL) processing by adding Cu metal layers and top Cu metal (0.8 um)


Oxide
Silicon
Dielectric(SiO2/SiN)
Gate Poly
STI (Shallow Trench Isolation)
W (Tungsten contact & via)
Cu (M1 – M5)
Cu (M6, Top Metal)
"Super-Contact"
6 um

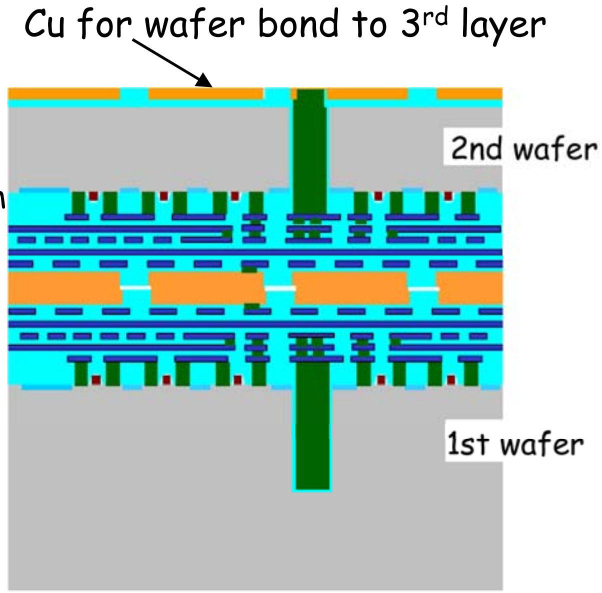
Tezzaron 3D Process

Example: bonding identical wafers


2nd wafer
12um
CuCu bond
1st wafer

Flip 2nd wafer on top of first wafer.

Bond second wafer to first wafer using Cu-Cu thermo-compression bond.

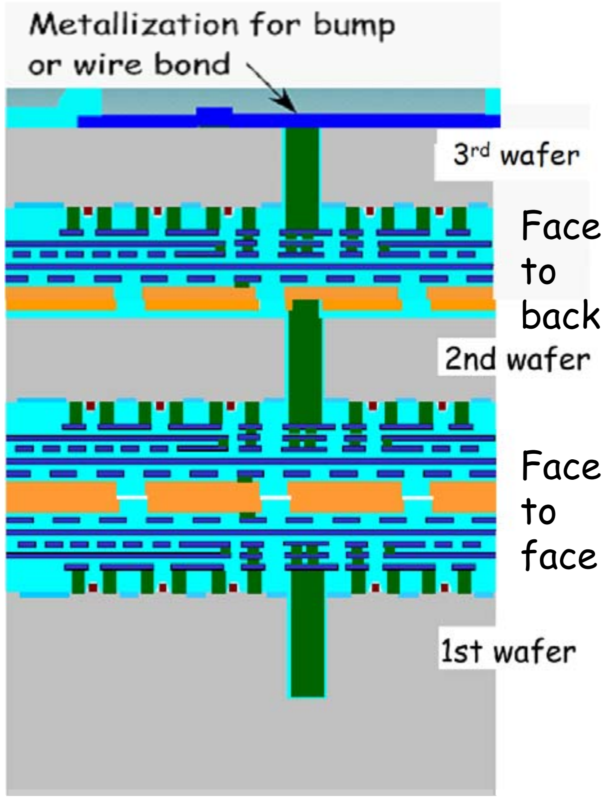

Cu for wafer bond to 3rd layer
2nd wafer
1st wafer

Thin second wafer to about 12um to expose super via.

Add metallization to back of 2nd wafer for bump bond or wire bond.

OR

Add Cu to back of 2nd wafer to bond 2nd wafer to 3rd wafer


Metallization for bump or wire bond
3rd wafer
Face to back
2nd wafer
Face to face
1st wafer

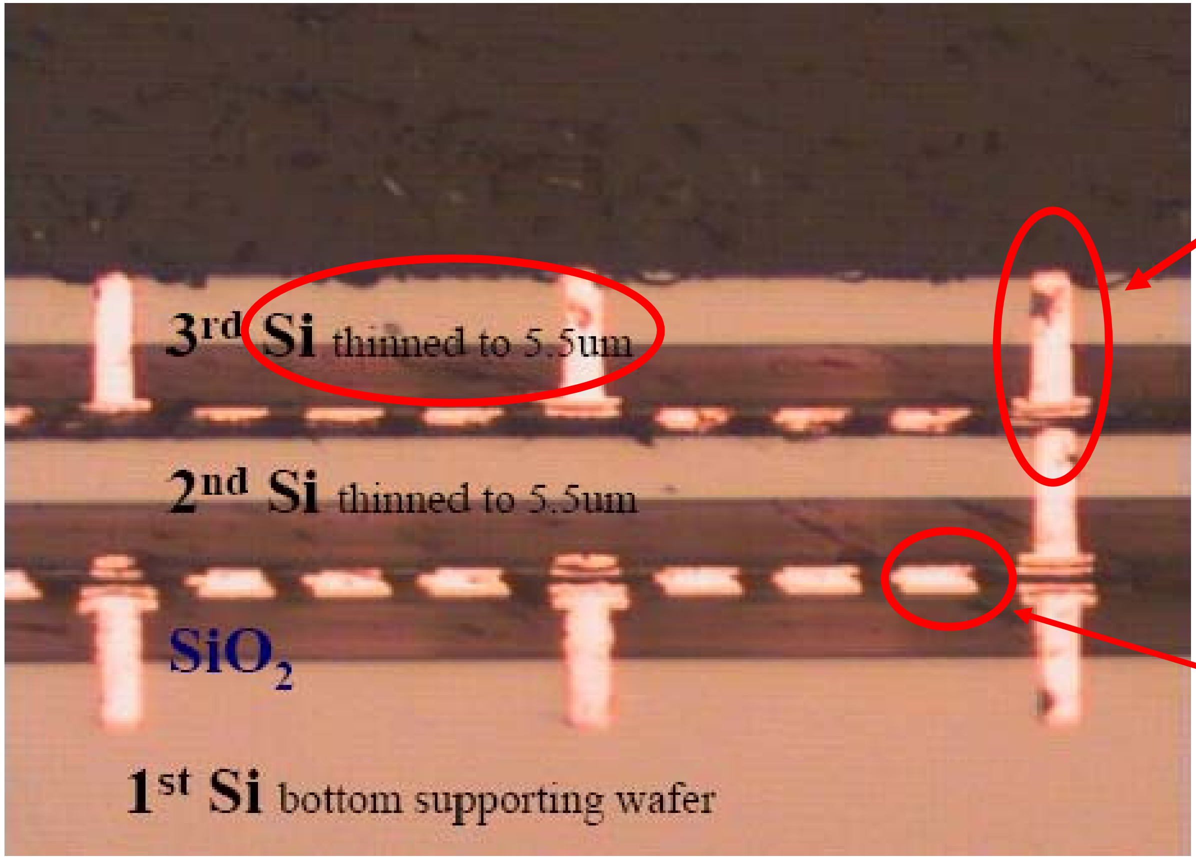
Flip 3rd wafer

Bond 3nd wafer to 2rd wafer.

Thin 3rd wafer to expose super via.

Add final passivation and metal for pads

Cross section of Tezzaron 3 Layer Stack[14]

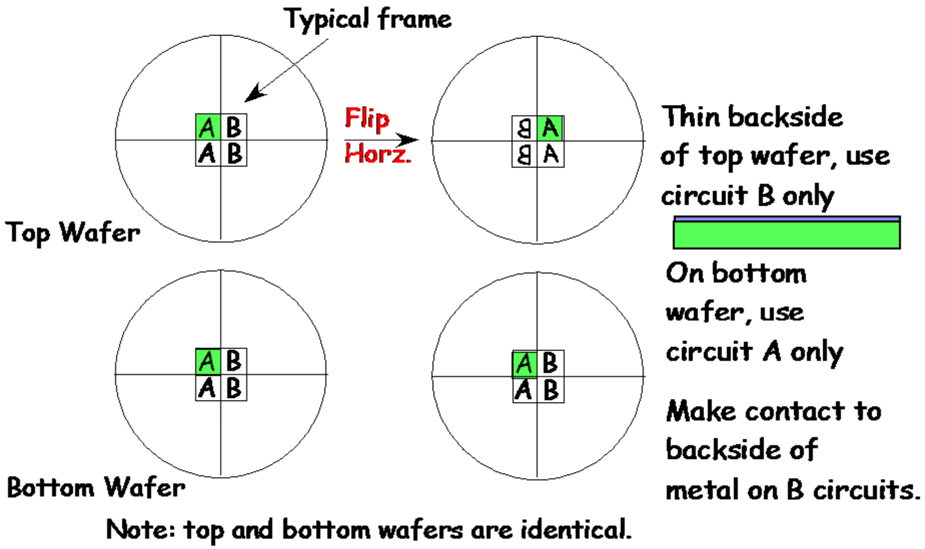

3rd Si thinned to 5.5um
2nd Si thinned to 5.5um
SiO2
1st Si bottom supporting wafer

Through silicon via

CuCu bond

Fermilab 3D Multi-Project Run

- Fermilab is planning a dedicated 3D multi project run using Tezzaron for HEP.
- There will be 2 layers of electronics fabricated in the Chartered 0.13 um process, using only one set of masks. (Useful reticule size 15.5 x 26 mm)
- The wafers will be bonded face to face.


Typical frame
Flip
Horz.
A B
A B
Top Wafer
Bottom Wafer

Thin backside of top wafer, use circuit B only

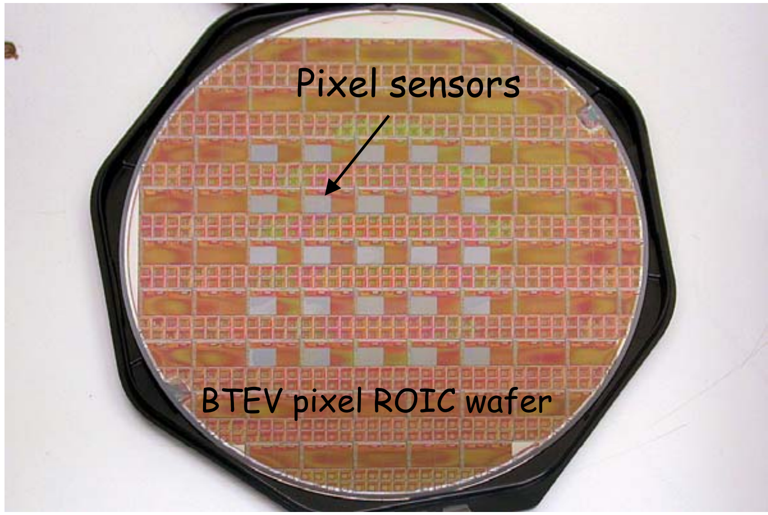
On bottom wafer, use circuit A only

Make contact to backside of metal on B circuits.

Note: top and bottom wafers are identical.

Face to Face Bonding

For devices without integrated sensors, bond pads will be fabricated for bump bonding to sensors to be done later at Ziptronix as shown below.


Pixel sensors
BTEV pixel ROIC wafer

Contributors to the MPW Run

- Received LOI from CNRS/In2P3 to join first Fermilab MPW run
  - Several French laboratories have received funding to perform 3D electronics development
- Received LOI from Universita di Bergamo to join first Fermilab MPW run
  - INFN has received funding for study of MAPS, including 3D circuit design
- Fermilab – coordinator for MPW run
  - Submission expected at the beginning of 2009 with delivery of 3D parts about 12 weeks later.
  - Cost – fabricate 25 eight inch wafers in 130 nm process and provide completed wafer to wafer 3D assemblies for under $300K.

Labs with Tezzaron NDAs for MPW Run

- Fermilab, Batavia
- University at Bergamo
- University at Pavia
- University at Perugia
- INFN Bologna
- INFN at Pisa
- INFN at Rome
- CPPM, Marseilles
- IPHC, Strasbourg
- IRFU Saclay
- LAL, Orsay
- LPNHE, Paris
- CMP, Grenoble

Total = 13

ILC Projects in Tezzaron MPW

- Convert MIT LL VIP2a design to the Tezzaron/Chartered process (VIP2b) - Fermilab
  - CMOS design should be easier.
  - Going from 3 layers in 0.18 um technology to 2 layers in 0.13 um technology could reduce pixel size below 20 um.
  - Using the "via first" process at Chartered eliminates the wasted area needed for vias in the "via last" MIT LL process.
  - Fabrication in the Chartered fully characterized process and models, along with standard cell libraries should lend itself to high yield.
  - Because VIP2b is in a CMOS deep sub micron process, the design should be inherently more radiation hard.
    - Radiation tolerance of Chartered 0.13 um process is currently being studied by another group.
- Convert 2D MAPS device design for ILC to 3D design where PMOS devices are placed on the tier without sensing diodes – Italy
- CMOS pixels with one tier used as a sensitive volume and the second containing electronics. - France

SLHC Projects in Tezzaron MPW Run

- Convert the current 0.25 um ATLAS pixel electronics to a 3D structure with separate analog and digital tiers in the Chartered 0.13 um process. – France [15]
- Develop a 3D chip with 2 tiers of electronics to explore the advantages of 3D for the Super CMS pixel detector. - Fermilab
  - Going from 1 layer of circuitry in a 0.25um process to 2 layers in a 0.13 um process can increase circuit density by a factor of 7.
  - Circuit density can by traded for smaller pixel size.
  - Features to consider for parallel processing
    - In pixel digitization
    - Large digital storage
    - Triggering capability
    - Sparsification
    - Reduction of peripheral circuitry

Conclusion

- New technologies have always presented challenges to HEP.
- Success with new technologies in HEP has often led to dramatic advances.
- Industry is making rapid progress in developing 3D integrated circuits.
- HEP is beginning to respond with new initiatives to explore this technology.
- Fermilab has 2 years of experience working in 3D. Others are welcome to join our program
- Working together we can meet the challenge.

“Ten years from now we won’t be asking ‘Why 3-D?’, we’ll be asking ‘Why 2-D?’”

– Jochen Reisinger, Infineon Technologies, IMEC annual review meeting, Oct. 15-16, 2007

Where will we be?

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