# Achieving Best Performance with VME-based Data Acquisition Systems and 2eSST

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The double edge Source Synchronous Transfer (2eSST) is the fastest block transfer cycle offered by the VME64x standard. The maximum achievable data-rate foreseen by the protocol is 320 Mbyte/s.
In this paper we present a reference design based on a FPGA for the reader willing to implement 2eSST in his VME64x application. By using this template, we have designed a custom Bit Error Rate Tester, in order to probe the block transfer reliability within and beyond the data rate limit presently set by the standard. Our results show that 800 Mbyte/s data transfers can be achieved in a 21 slots crate with a BER smaller than 10ˆ-12.

## Summary

Since its appearance in the 80's, the VMEbus played a leading role in the embedded computing, real-time control and data acquisition systems for High Energy Physics experiments. Nowadays, the original standard has undergone major improvements and new features have been added to its physical and logical layers.
The double edge Source Synchronous Transfer (2eSST) is the fastest block transfer cycle offered by the VME64x standard. It consists of exchanging bursts of 64-bit words between the master and the slave without any hand-shake. The data sender validates words with rising and falling edges on a strobe line, thus achieving a Double Data Rate (DDR) transfer. In this protocol, the transfer rate is only limited by the timing skews of the data lines with respect to the strobe. Presently, the standard sets the transfer rate to 320 Mbyte/s.
In our paper we present a reference design to implement 2eSST in a FPGA-based VME board and we propose a general implementation and layout scheme. The nature of 2eSST suggests the deployment of FPGAs providing DDR input/output blocks, but our scheme applies even to older, non-DDR capable FPGAs. Our design implements a Bit Error Rate Tester (BERT) and we used it to perform Bit Error Rate (BER) tests on 2eSST transfers within and beyond the maximum data rate specification. We measured BER, data timing jitter and eye diagrams with different bus load configurations and data patterns. Our measurements show that, on a 21 slots VME crate, it is possible to achieve reliable 2eSST transfers with rates up to 800 Mbyte/s, keeping the BER under 10ˆ-12.
The BERT has been conceived such that the user can use it as a starting point for the design of its own application. In this view, we also discuss the critical issues the user has to deal with in the design of a 2eSST interface both at FPGA and board levels.

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