FPGAs in 2008 and beyond
the future platform for transforming, transporting and computing
TWEPP Topical Workshop on Electronics for Particle Physics
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Presented by Volker Lindenstruth
Including slides from Ivo Bolsens
Agenda

• The FPGA Trends

• The Triple Play Opportunity

• The Platform Approach

• V5 News

• Conclusions
Twenty Years of Evolution

- 1988: XC3090
- 2008: XC5VLX330T

- 1000 times the number of LUTs
- 2000 times the number of configuration bits = complexity
- 20 times the speed
- 500 times cheaper per function, not counting inflation

*Moore’s Law has been good to all of us!*
FPGA Status

Clocking Flexibility
- DCM (precision synthesis)
- + PLL (Low jitter)

Faster Time To Market
- Cross Platform Compatibility in “T” devices

Greater System integration
- PowerPC 440 with crossbar and APU
- Integrated x1, x4, x8 End-point blocks

More Logic Packing
- 6-LUT architecture

Optimized Serial IO
- Low power 100Mbps to 3.2Gbps GTP
- 150Mbps to 6.5Gbps GTX

Integrated Reliability
- System Monitor

New PCI Express
- Integrated x1, x4, x8 End-point blocks

Integrated PLL (Low jitter)
FPGA Capacity Trends

ITRS 2013:
2.6M LCs
(3.1B transistors)

Largest Xilinx FPGA

Historical Data
FPGA Performance Trends

Historical FPGA data:
- 2007: 325 MHz typical; 500 MHz max
- 2013: 500 MHz typical, 750 MHz max

System Speed (MHz)
FPGA Power Trends

$V_{ccint}$

Total Power of Largest Device

ITRS 2013: 25W

Core Power Supply (V) [Lines]

Power (W)


ITRS LP $V_{dd}$
Price Per Logic Cell

![Graph showing the decrease in price per logic cell over time from 1990 to 2015. The y-axis represents $/LC, with values ranging from 0.0001 to 1.0, and the x-axis represents years from 1990 to 2015. The graph displays a downward trend, indicating a decrease in price per logic cell over the years.]
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The Triple Play Opportunity

- Global Internet traffic will reach 44bn gigabytes per month in 2012, compared to less than 7bn in 2007
- Video goes from 22% of consumer traffic in 2007 to 90% in 2012
- Mobile data traffic will roughly double each year from 2008-2012

Source: Cisco Visual Networking Index – Forecast and Methodology 2007-2012

Backdrop: focus on reducing power consumption to reduce operating expense
Consumer Internet Traffic Analysis 2007-2012

All Video: 49% of IP traffic

Fastest growth: Video to TV

Video Comm will be driver beyond 2012

P2P is large portion of IP traffic: 33%

Source: Cisco
Triple Play: Key Technologies

1. Digital Signal Processing
   - Transforming data
2. Packet Processing
   - Transporting data
3. Tera Computing
   - Analyzing data
Wired Networking Trends

- The line rate is what drives the processing and input/output challenge on each line card.
- The challenge is growing in step with Internet traffic growth.

Sources: IP Traffic, Cisco; Line Rate, Standards/Nortel
Trend Towards Packetized Network-on-Board

QPI (processor-memory)

- Protocol layer
- Transport layer
- Routing layer
- Link layer
- Physical layer

Examples

PCI-Express (local interconnect)

- Transaction layer
- Data link layer
- Physical layer

MIPI (mobile peripherals)

- Transport layer
- Network layer
- Data link layer
- PHY adapter sub-layer
- Physical layer

Packets sent over physical serial link

Layer 1 header | Layer 2 header

Layer n header | Data payload
**Wireless Networking Trends**

Longer-term trends:
- Multi-mode radio and cognitive radio (increasing adaptability)
- Mobility as central feature of Internet (increasing demands)

Computation and programmability grow, power budgets shrink

Source: Nokia/NXP
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Bridging the Gap

- **Systems and Applications**
- **Platform Design Methods and Software**
- **Circuits and Architectures**

The opportunities
The full power of silicon
Misery of details

The full power
Miser of details
Platform-based Methodology

- **Use of high level language:**
  - Describe top-level relationships between system components
  - Program processor-based components
  - Program some logic-based components
  - APIs hide all HW components
  - APIs hide external interface detail
  - Debugging in Soft terms

- **Hides underlying platform detail:**
  - ISE and EDK tools
  - OS device drivers
  - Board settings
Design Methodology Roadmap

EDA world GUI (e.g. ISE)

Hardware

Software

IDE world GUI (e.g. Eclipse)

User interface

Look and feel

Domain-specific methodologies

Component-based software engineering

Programming language and development environment

HDL

IP block integration

Software + APIs

Platform-based design and debug

Back end technology

Flattening synthesis and PAR

Hours

Compilation time

Minutes

Structured synthesis and PAR

Packet Processing Processing

DSP Data
High Performance Compute Platform
Added:
- I/O processing
- Co-processing
- Peer Processing

Animated boxes and the Virtex-5 Logo

TTAFKAA, 3/26/2007
Heterogeneous Multi-Processor

- 1066Mhz I/O Characterization
- FSB protocol on FPGA
- 8.5 GByte/s Memory BW
The Software Solution

C/C++/FORTRAN Source

Serial application on standard processor

Dynamic library call

C Inner Loop

Compile directly from C to FPGA-ISA

Parallel algorithm On FPGA

High-performance interconnect
Abstraction API

- **Message Passing Interface (MPI)**
  - HPC Industry Standard API
- **Communication in heterogeneous systems**
  - Processor-to-Processor
  - Processor-to-Hardware Engine
  - Hardware Engine-to-Hardware Engine
- **Identical API in C & HDL**
  - Node Discovery (ID)
  - Node Programming (.exe and .bit)
  - Data Send & Receive
  - Synchronization
- **Abstract and isolate hardware changes**
  - Promotes portability
  - Allows code reuse
  - Improves system scalability

**Heterogeneous Clusters:**
- Intel, AMD x86 Binaries
- FPGA Bitstreams
- Infiniband & 10GE Backplane
Combining Xilinx FPGA Technologies with Software and Hardware to help the “Domain Expert”

Measure It and Fix It
The Engineering Innovation Process

- Design
- Prototype
- Deploy

Consistent User/Domain-level Software Tools and COTS Hardware

Standard Component Hardware and Backend Software

LEGO Mindstorms NXT
“the smartest, coolest toy of the year”
100’s thousands of students

CERN Large Hadron Collider
“the most powerful instrument on earth”

Engineering Team
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Virtex-5 Common Features

- 6-LUT + Express Fabric
- 36Kb Dual-Port Block RAM / FIFO with ECC
- SelectIO with IDELAY/ODELAY and SerDes
- 10/100/1000 Mbps Ethernet MAC
- PCI-Express Endpoint Blocks
- GTP 3.75 Gbps Transceivers
- GTX 6.5 Gbps Transceivers
- PowerPC440 Processors
- 550 MHz Clock Management
- Integrated System Monitor A/D Converter
- Advanced Configuration Options
- 25x18 DSP Slices
- New Capability
- Higher Bandwidth
- Higher Precision
- Saves Logic
- Precision + low jitter
Virtex-5 FXT
Additional Capabilities

• One or two PPC440 hard Microprocessor cores faster and more efficient than PPC405, super-scalar, larger caches, deeper instruction pipeline, integrated crossbar switch saves thousands of slices

• GTX High-performance Transceivers optimized for performance and low power and pc-board signal integrity for an “open eye”.

5 family members, 3 in volume production by Sept.08
More Than Just a PPC440...

- Four built-in DMA channels provide high speed access to memory or I/O
- Separate memory and I/O buses greatly improve system performance
- External masters can access memory or I/O through the crossbar
**PPC440+128-bit FPU via APU**

- Soft co-processor module, free-of-charge accessible by the 440 processor instruction pipeline
- Single- and double-precision IEEE-754 compliant
- Speed-up 6 to 30 times, 200 MFLOPS sustained
GTX Multi-Gigabit Transceiver

- 8 to 24 transceivers per device (40 and 48 in ‘TXT subfamily)
- Supporting data rates from 150 Mbps to 6.5 Gbps
- Power dissipation less than 250 mW per channel
- Programmable Tx pre-emphasis and Rx equalization
6.5 Gb/s Transmit Eye Opening

http://www.xilinx.com/support/documentation/virtex-5.html#19312
New Additions to the Family

- XC5VTX150T and ‘TX240T
- Like ‘FX130T and ‘FX200T minus the PPC microprocessor.
  but with twice the number of GTX transceivers
  40 and 48 GTXs respectively
- Availability: ES 4Q08, Production 1Q09

When you need lots of fast transceivers
Conclusions

• FPGA the programmable platform for
  – Transforming, transporting and computing digital data

• A trend towards specialized HW and SW to support programmable system solutions

• A strategy of working with Academics to enable exploration of new system applications & research

• Multi-gigabit transceivers are very popular

• Moore’s Law will give us much more logic and lower cost
  – Speed, power consumption, packaging pose a difficult challenge

• Users want and need to improve design productivity
  – The pace is becoming faster and more competitive.
Thank You