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FPGAs in 2008 and Beyond

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Since 90 nm, Moore's Law offers diminishing performance increase,
requires architectural changes:
Bigger LUTs, dedicated hard cores, microprocessors and transceivers.
Virtex-5 had excellent start in 2007
In 2008: Virtex-5 FXT.
PPC440 with attached 5 x 2 Crossbar for performance and flexibility.
GTX Transceivers achieve 6.5 Gbps data throughput.

After 2008 through 2013:
45 nm followed by 32 nm technology.
More transistors and lower cost per function.
(average 10% per year, or factor 10 every 7 years))
Capacity limited by die size
Performance limited by power and heat budget.
Various effects and trade-offs are discussed.

Summary

Below 90 nm, Moore's Law no longer gives higher speed for free. Most performance improvement must come from architecture: 6-input LUTs, better memory, hard cores for Ethernet, PCIe, Gigabit transceivers, embedded microprocessors.
Virtex-5 had an excellent start in 2007, and still has no serious competition in its field. New in 2008 is Virtex-5FXT with PPC440 microprocessor(s) plus up to 48 faster transceivers.

PPC440 is not only faster than its PPC405 predecessor was in Virtex-4, it is also more flexible and far more efficient thanks to an embedded 5x2 Crossbar which supports two simultaneous transfers over 128-bit wide channels.
The PPC440 also has an Auxiliary Processor Unit Port for attaching a co-processor, e.g. a floating point unit. Xilinx offers a soft core that supports IEEE single- and double-precision floating point operation, and is between 6 and 28 times faster than running software on the PPC440, or 3 times faster than an equivalent co-processor solution running on the Virtex-4.

Virtex-5 FXT and 'TXT devices offer up to 48 Transceivers with improved features and higher data rate.
Wide frequency range, 150 Mbps to 6.5 Gbps, at only 200 mW per channel.
Each transmitter offers programmable pre-emphasis, while each receiver has analog equalization and digital multi-tap Decision Feedback Equalization (DFE). The receiver can handle up to 150 consecutive 1s or 0s without losing lock, but also supports 8B/10B, 64B/66B and Interlaken protocol.

2009 to 2013

45 nm technology, followed by 32 nm
Moore's Law is still alive, offering more transistors and lower cost per function (average 10% per year, or a factor 10 every 7 years)
But raw transistor speed will become more difficult to improve, and supply voltage scaling reaches its limits.
Chip capacity will grow, since it is determined by the ratio of die size to feature size.
System performance will mainly be limited by the power and heat budget.

Issues:
Need for alternative technologies optimized for either performance of power, not both. Limited power budgets: 2 W max for cell-phones, due to heat, even if there will be better batteries.
As feature size shrinks, manufacturing spread becomes a bigger issue, affecting yield. Increase in logic density might outstrip pin-count (presently at around 1200). High demands on long-term reliability can preclude experimentation with new device materials and exotic processing.

Higher design productivity.
Users'design time may become a limitation. Design re-use becomes more important. Place-and-route times

must remain acceptable, need for incremental compile and block-based design. Learn to utilize multi-core computers.

The Future:
As systems get more complex, and their product lifetime decreases, FPGAs become an ever more attractive solution.

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