

# CMS microstrip tracker readout at the SLHC

Thursday 18 September 2008 12:15 (25 minutes)

The increased luminosity at the SLHC and associated increases in occupancy and radiation levels present severe challenges for the CMS tracker, which will require complete replacement. Inner pixellated regions will expand to higher radii and the outer tracker region will most likely be instrumented with short strip silicon sensors. It is also necessary for the tracker to provide information to the level 1 trigger.

Power consumption is one of the main challenges for the tracker readout system, because of the higher granularity. We will present the current status of readout chip development for a short strip outer tracker, with projections for performance and power consumption.

## Summary

The biggest challenge for tracker readout systems at the SLHC is power; consumption and provision. Higher luminosity and therefore granularity means more front end chips. Advanced CMOS technologies will help, but power savings/chip will depend on functionality.

The current CMS strip tracker readout system is analogue, with no sparsification on-detector, utilising 0.25  $\mu\text{m}$  CMOS technology throughout. The readout architecture at SLHC is not yet defined, but will certainly be different. Data transmission links at SLHC will be digital, taking advantage of commercial developments, so front end digitization is required if we decide to retain pulse height information. ADC power estimates indicate that this is possible, but only after a multiplexing stage. Zero-suppression may also be needed to reduce the transmitted data volume and maximise the ratio of FE chips to links, to minimize link power contribution.

0.13  $\mu\text{m}$  CMOS technology will be used to develop readout circuits for SLHC. MPW (multi-project wafer) access to the technology is available, and has already been characterised for HEP applications. We need to begin mass production of readout chips several years before installation, so timescales dictate that prototype development must begin now.

Power provision is also a major challenge. Since 0.13  $\mu\text{m}$  chips operate at half the supply voltage of 0.25  $\mu\text{m}$ , the supply current increases even if the total SLHC tracker power remains the same as LHC, increasing power dissipated, and voltages dropped, in cables. Serial powering or on-detector DC-DC conversion will help, both of which have implications for FE chip design.

Front end specifications must be developed. A number of relevant sensor technology issues are yet to be decided, and are the subject of wider CMS tracker R&D. Aspects which are directly relevant to the readout chip development are:

- sensor signal polarity: n-side readout of p-substrate or vice-versa.
- sensor-FE chip coupling: DC coupling simplifies sensor design and reduces cost, but requires the front- end chip to sink or source leakage currents.
- sensor strip lengths and pitches: capacitance and leakage current, and hence noise, depend on length and pitch, requiring optimization of the amplifiers.

We report on the current status of developments for CMS short strip tracker readout at SLHC, giving predictions for performance and power consumption for electronic architectures matched to different sensor and readout choices.

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**Session Classification:** TOPICAL 1 - LHC Upgrades