Contribution ID: **76** Type: **Poster**

Data Acquisition System for the KL Experiment at J-Parc

Thursday 18 September 2008 16:15 (20 minutes)

We present the proposed Data Acquisition (DAQ) System for the KL Experiment at J-Parc, Japan. It comprises three distinctive flavors of 6U VME boards: a 14-bit, 125 MHz ADC module for reading out an approximately 3000-channel Cesium-Iodide (CsI) detector; a 12-bit, 500 MHz ADC module for reading out a 100-channel Beam Hole Phase Veto (BHPV) detector; and a digital Trigger module able to provide a detector-wise synchronous energy sum. The Csi Calorimeter readout board amplifies analog pulses from 16 photomultipliers and passes them through a 10-pole shaper before digitizing. Data are then processed locally with field programmable gate arrays (FPGAs) to determine real-time energy values for the system Trigger Supervisor. The ADC module is provided with a pipeline, up to 4us long, which stores the acquisitions, awaiting the system trigger pulse. After a trigger, data are packed and buffered for readout via the VME32/64 backplane. The full design and preliminary test results will be described

Summary

This paper presents the Data Acquisition (DAQ) System for the Step-1 phase of the E14 experiment, a high energy physics kaon experiment at the Japan Particle Accelerator Research Complex (J-PARC). The goal of the experiment is to measure the rate of the rare decay KL->pi0 nu nubar. This flavor changing neutral current decay is predicted by the Standard Model to happen only once every 3.3x10*11 KL decays. If not observed or observed at a rate very different from the predictions, it will shed light on the mechanism responsible for CP in the quark sector.

The front-end electronics comprises over seventeen 6U VME Crates, and includes three distinctive blocks:
- The Cesium Iodide (CsI), using custom 14-Bit, 125MHz ADC Modules, with 16 channels per module. This block has up to 3,000 Channels.
- The Veto Detectors, using the same custom 14-Bit, 125MHz ADC Modules, fitted with a different firmware. This block has up to 512 channels.
- The Beam Hole Phase Veto, using custom 12-Bit, 500MHz ADC Modules, with 4 channels per module. This block has up to 100 channels.

In the CsI Calorimeter, every analog pulse generated by the photomultiplier tube (PMT) is amplified and passed through a 10-pole filter/shaper with a cutoff frequency of about 10 MHz, which converts the fast PMT pulse into a Gaussian form, while keeping the total energy information constant. The filter/shaper was calculated for optimal Full Width Half-Height (FWHH) of the resulting shape with respect to fitting and timing. After shaping, each pulse is applied to a sample-and-hold ADC chip.

Digitized data are processed locally with field programmable gate arrays (FPGAs), Altera EP2S60F1020C5 chips from the STRATIX II family that perform the board total energy calculation and determine real-time board energy related values. These values are passed through the crate's backplane to custom Transition Boards for successive summing in the crate. The result is a crate-level energy value, which is sent over to the Trigger Supervisor Module, for final decision, and eventual trigger pulse generation.

Each ADC module is provided with a pipeline, up to 4us (500 samples) long, which stores the acquisitions while awaiting the system trigger pulse. After a trigger, data are packed and buffered for readout. In this experiment, events happen in 0.75 second long "spills", followed by 2.65 second long periods of no activity. All events acquired in the 0.75 second spill can be stored in the on board 32 MBytes SRAMs. This allows readout only during the no activity period, to improve the overall signal-to-noise performance. The readout can be performed via the VME32/64 backplane, or via an optional front panel optical link.

Sampling for all calorimeter channels is simultaneous on one low jitter system clock.

In conclusions, this DAQ System is designed to accommodate the particular requirements for the JParc KL Experiment, such as signal conditioning with 10-pole filters that convert narrow PMT signals into Gaussian shaped pulses with optimal FWHH; low input noise; powerful real-time processing with on board FPGAs, and relatively small overall size.

Author: Mr BOGDAN, Mircea (The University of Chicago)

Co-authors: Mr GENAT, Jean-Francois (The University of Chicago); Dr TECCHIO, Monica (University of Michigan); Prof. CAMPBELL, Myron (University of Michigan); Prof. WAU, Yau (The University of Chicago)

Presenter: Mr BOGDAN, Mircea (The University of Chicago)

Session Classification: POSTERS SESSION