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DAQ and Control Systems for the CMS Global Calorimeter Trigger Matrix Processor

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A new trigger component based on the uTCA standard is being developed for the CMS Global Calorimeter Trigger (GCT). The new system is designed to handle the exchange of data between GCT and the Global Muon Trigger and is called the GCT Muon System. The GCT muon system consists of a uTCA crate with a custom uTCA backplane instrumented with several Matrix processor cards, which use a Xilinx Virtex-5 FPGA and an M21141 72x72 cross-point switch. We discuss the development and use of the various communication systems available for the Matrix processor. Given the nature of the Virtex-5 FPGAs used as the basis of the design, there are several communication protocols available. In this paper we focus on the use of PCI express and Gigabit Ethernet UDP/IP using the built-in Virtex-5 interfaces, and TCP/IP and IPMB via an NXP microcontroller interface on the Matrix board itself. The use of these interfaces for slow control of the board and fast Data AcQuisition (DAQ) are discussed in terms of available bandwidth and resource usage. Furthermore we discuss the implications of the use of such industry-standard interfaces as a replacement for more traditional simplex busses such as VME. To that end we outline the development of a new Hardware Abstraction Layer (HAL) with built-in overlapped I/O and one possible serial bus architecture providing a metastability-tolerant interface and auto-discovery for ease of use.

Summary

The Matrix Processor is a generic processing module designed for use in the GCT Muon system as well as a prototype for the next-generation CMS trigger system which is anticipated for future upgrades of the off-detector electronics. The board combines advanced telecoms switching and the latest Xilinx Virtex 5 FPGAs in a dense 3U uTCA form-factor. Being a specification based on serial links, uTCA provides definitions of how to design electronics that can interoperate using several standard protocols, including Gigabit Ethernet (GbE) and PCI express (PCIe), as well as a card management interface derived from the Inter-IC (I2C) specification (called IPMB). The Xilinx Virtex-5 FPGAs natively support GbE and PCIe, containing both tri-mode Ethernet MACs and PCIe endpoints. These can be driven either into the uTCA backplane or to the optical fibres on the front of the Matrix board. The board also provides a 10/100 Ethernet control interface via an NXP microcontroller. This provides a plethora of interfaces to choose from for both command/control and DAQ functionality.

In this paper we discuss the usage of these interfaces in the context of a larger configurable trigger system. The implications of using these industry-standard interfaces and the replacement of more traditional simplex bus interfaces such as VME is also considered. To that end we discuss the development of a new Hardware Abstraction Layer (HAL) based on overlapped I/O that allows the concurrent completion of register reads/writes from a single application in a thread-safe manner, necessary for optimal performance when using such interfaces. Coupled to this we discuss a possible bus implementation that simplifies the construction of the internal configuration space in the FPGA firmware.

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