R & D on High Precision TDC for CMS MG-RPC

Université Claude Bernard Lyon 1

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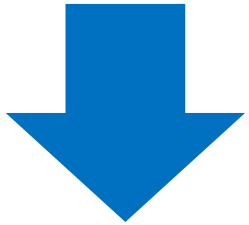
Requirements for CMS MG-RPC

- **Single Gap RPC timing resolution : < 1 ns**

- **Multi Gap RPC timing resolution ("LSB") : < 20 ps**
- **Counting rate : 10^4 Hz (100 µs)**



Goal

- **TDC timing resolution : 10 ps**
- **Precision : < 3 ps RMS**
- **Dead Time : << 100 µs**

TDC for medical imaging based on DLL

- ✓ **CMOS 0.35µm AMS process**
- ✓ **Clock : 160 MHz**
- ✓ **32 cells delay**
- ✓ **LSB : 200 ps**
- ✓ **RMS resolution : 60 ps**
- ✓ **RMS jitter 15 ps**
- ✓ **Power supply : 5.6 mW**

TDC concept in FPGA

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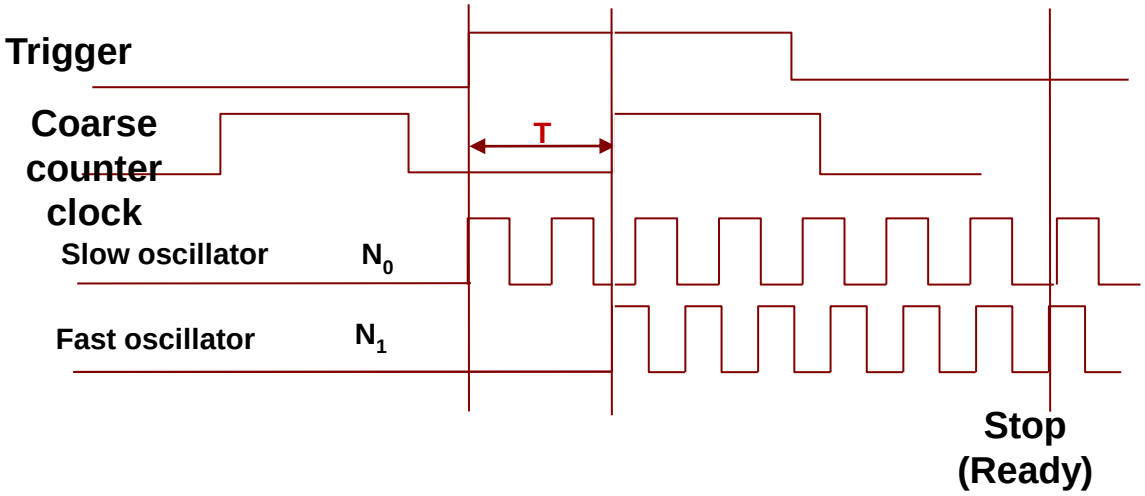
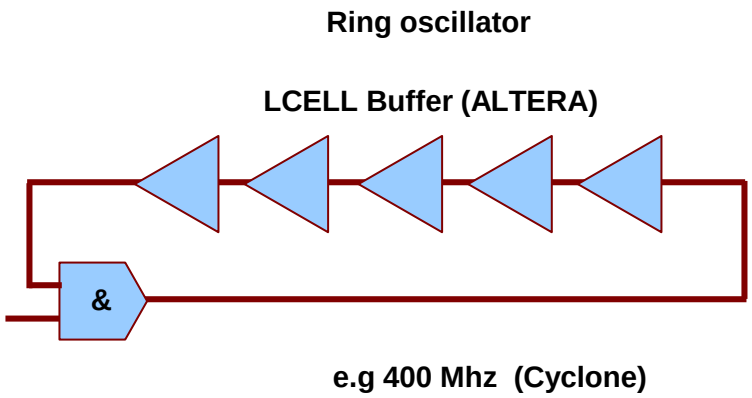
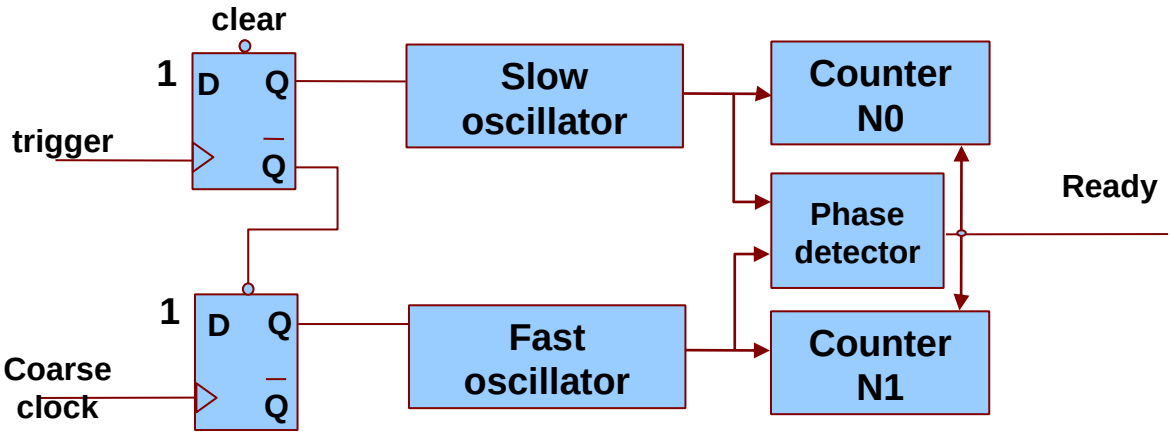
- Possible solution : Ring oscillators TDC
  - low area
  - low power

- Autocalibration
  - T_{slow}
  - Δt







$$T = N_0 T_{slow} - N_1 T_{fast}$$

Some values

$$T - T' = (N_0 - N'_0)T_{slow} - (N_1 - N'_1)T_{fast}$$

$$\Delta t = T_{slow} - T_{fast}$$

$$T = (N_0 - N_1).T_{slow} + N1.\Delta t$$

Timing Resolution = Δt

Dead Time = $T_m = T_{coarse\ counter} + (T^2_{slow} / \Delta t)$

Counter Range N1 = $T_{slow} / \Delta t$

Counter Range N0 = $(T_{slow} / \Delta t) + (T_{coarse\ counter} / T_{slow})$

$F_{coarse\ counter}$ (Mhz)	F_{slow} (MHz)	Δt (ps)	Tm (ns)	DR N0	DR N1
40	400	10	625	260	250

Input | Design parameters

Preliminary results TDC in FPGA

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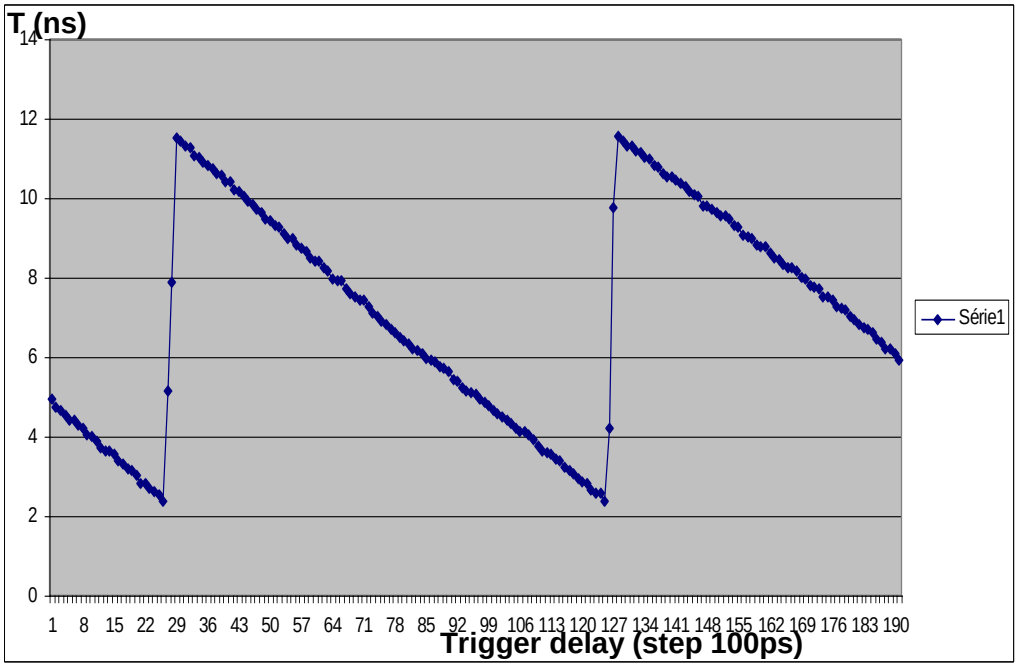
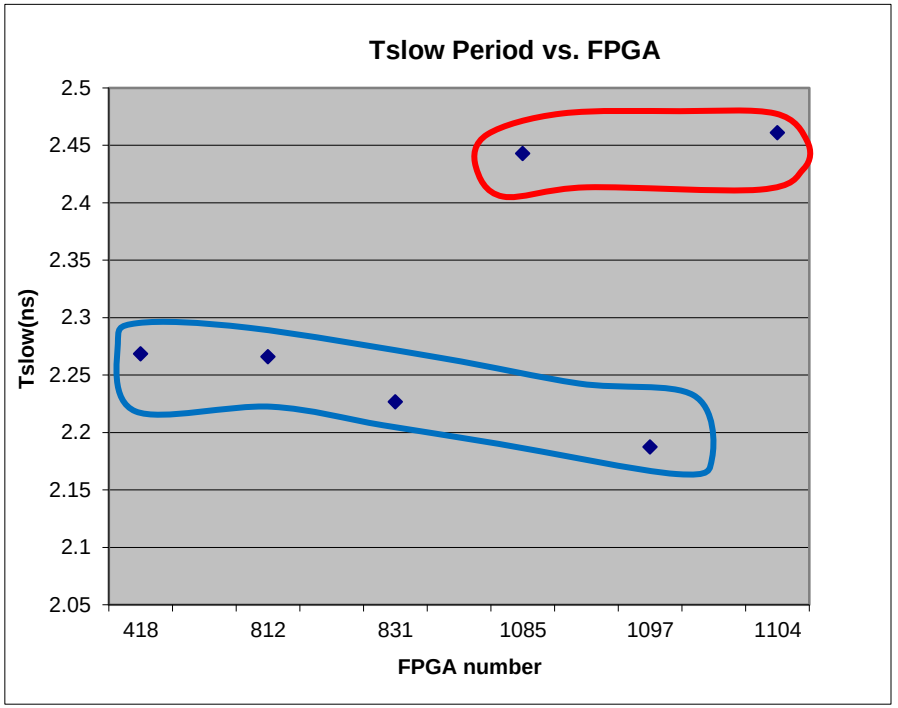
- **Remote implementation on telescope : First tests are very positive**
- **Coarse counter clock period = 10 ns**
- **Trigger step 100 ps**

TDC response (mean of 10 measurements)



T_{slow} response comparison on 6 FPGAs



Good linearity and no missing code

R & D in 2013 on this Achitecture

- Implement this architecture in full a custom ASIC
- Based on ring oscillator :
  - Δt =Ts-Tf = 10 ps ?
  - Δt drift ?
  - Matched ring oscillators
  - Ts & Tf jitter
  - Process ?
  - Process Dispersion ?
  - Temperature effect ?
- Key issue is analog (ring oscillator)

Pro :

- Ring oscillator works on trigger event
- Power supply reduction
- Easy to calibrate with 2 specifics runs
- Mostly digital TDC (except ring oscillator)

Con:

- Dead Time
- Ring oscillator design

- Start by a design study on ring oscillator : process stability and Δt
- Run schedule by Q3 or Q4 2013
- Funds from IN2P3