ROC CHIPS

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http://omega.in2p3.fr/

Orsay MicroElectronics Group Associated

OMEGA/Orsay « ROC chips »

- The OMEGA group (10 designers) has been designing "ROC" ASICs for 10 years, in AMS (AustriamMicroSystem) SiGe 0.35 µm technology to read out signals from various families of detectors and photodetectors
- Readout for MaPMT and SiPM and Si Pin diodes for ILC calorimeters and other applications
- Very high level of integration : System on Chip (SoC)

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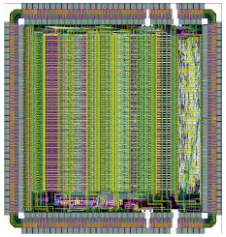
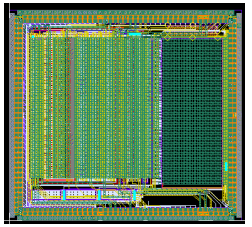
Chip	detector	ch	DR (C)
MAROC	PMT	64	2f-50p
SPIROC	SiPM	36	10f-200p
SKIROC	Si	64	0.3f-10p
HARDROC	RPC	64	2f-10p
PARISROC	PM	16	5f-50p
SPACIROC	PMT	64	5f-15p
MICROROC	µMegas	64	0.2f-0.5p

PETIROC SiPm 16 50fC- 300pC

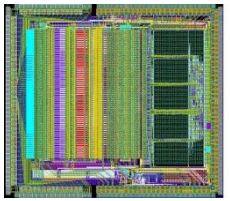
MAROC3



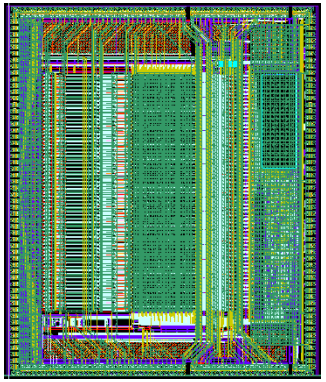
HARDROC2



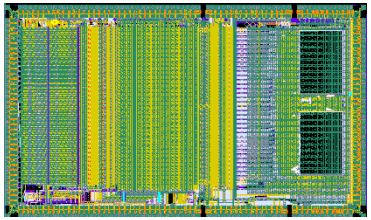
MICROROC1



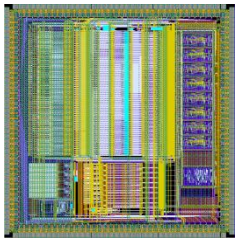
SKIROC2



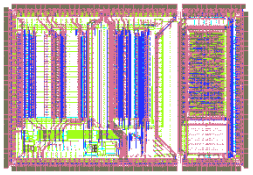
SPIROC2



SPACIROC



PARISROC2



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HARDROC2b

- 10000 chips to readout the RPC of SDHCAL technological proto (ILC)

- **64 inputs,** Current preamp with **8 bits** gain correct:
  - G=0 to 255 (analog G=0 to 2)

- **3 shapers**, variable Rf,Cf and gains:
  - Fsb1, G= ½,**1/4**,1/8,1/16
  - Fsb2, G= 1/8,**1/16**,1/32,1/64

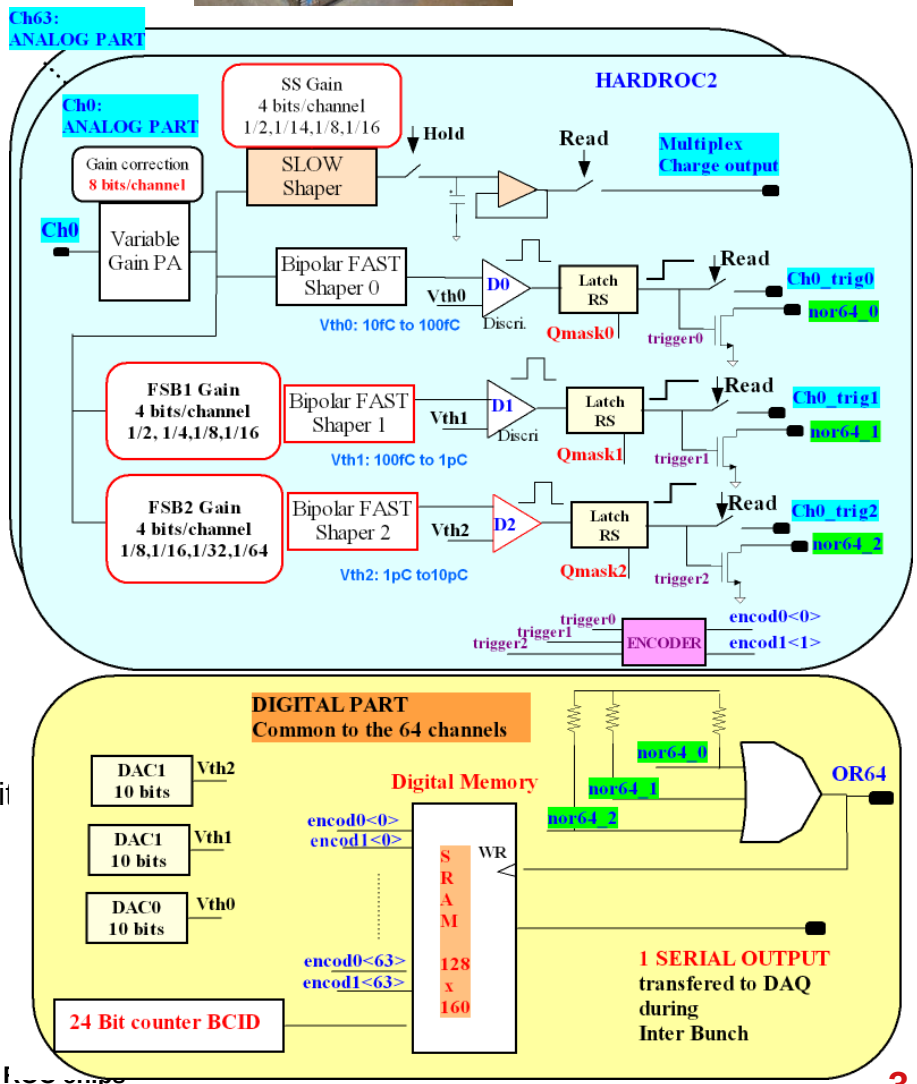
- **3 discriminators**
  - 3 10 bit-DACs to set the thresholds (100fC, 1pC, 10pC)
  - Encoded in 2 bits

- **Auto-trigger down to 10fC up to10pC**

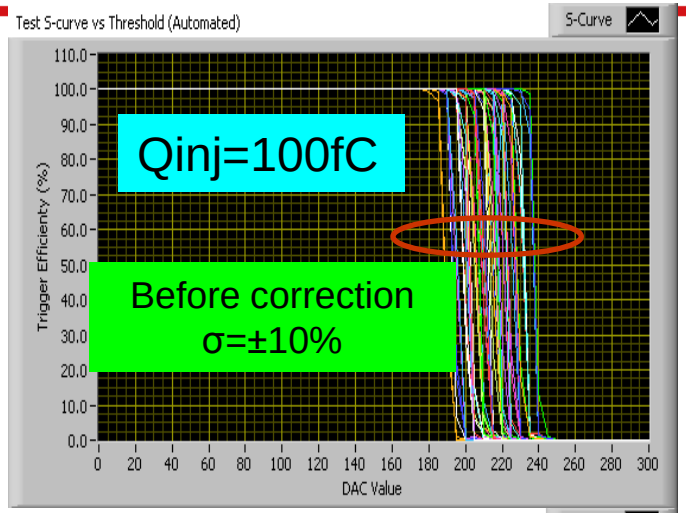
- Store all channels and BCID for every hit in a **127 bit deep digital memory**
  - Data format : 127 (depth)*[2bit*64ch+24bit(BCID)+8bit(Header)] = 20 320 bit

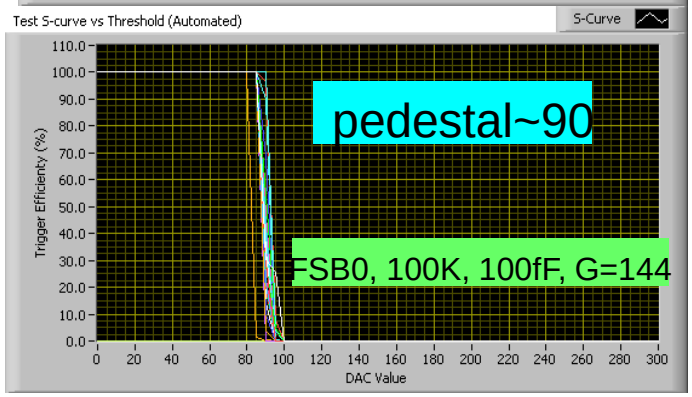
- **872 SC registers**, default config
  - Mask of bad channels

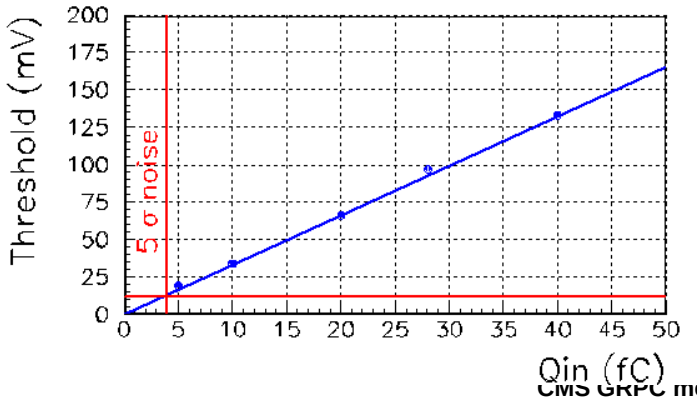
- **Full power pulsing: < 10µW/ch**

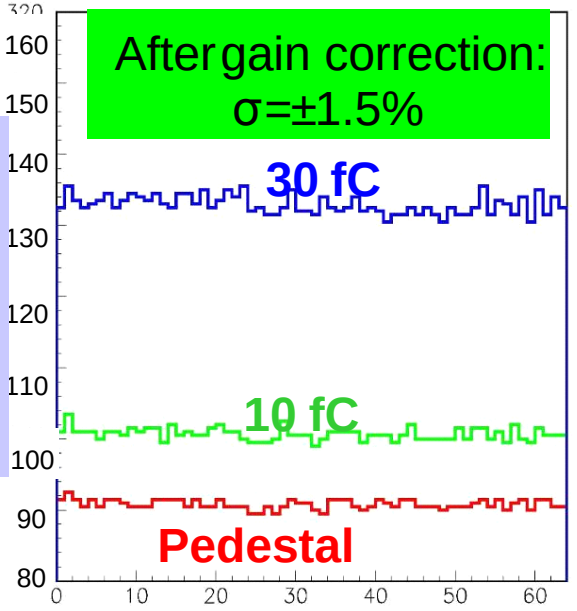


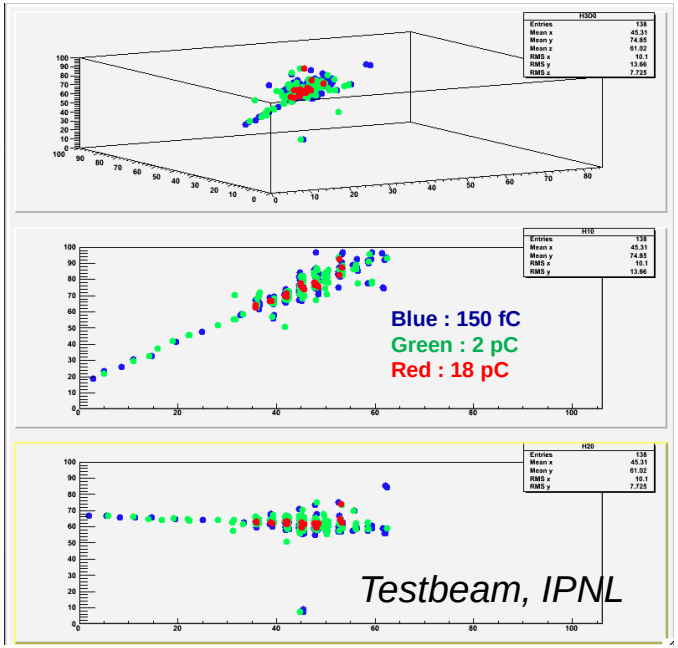
TRIGGER EFFICIENCY MEASUREMENTS





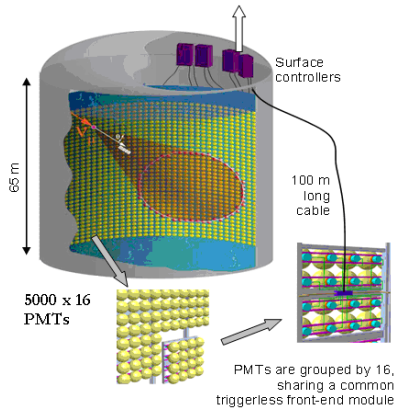






PARISROC for large PMTs

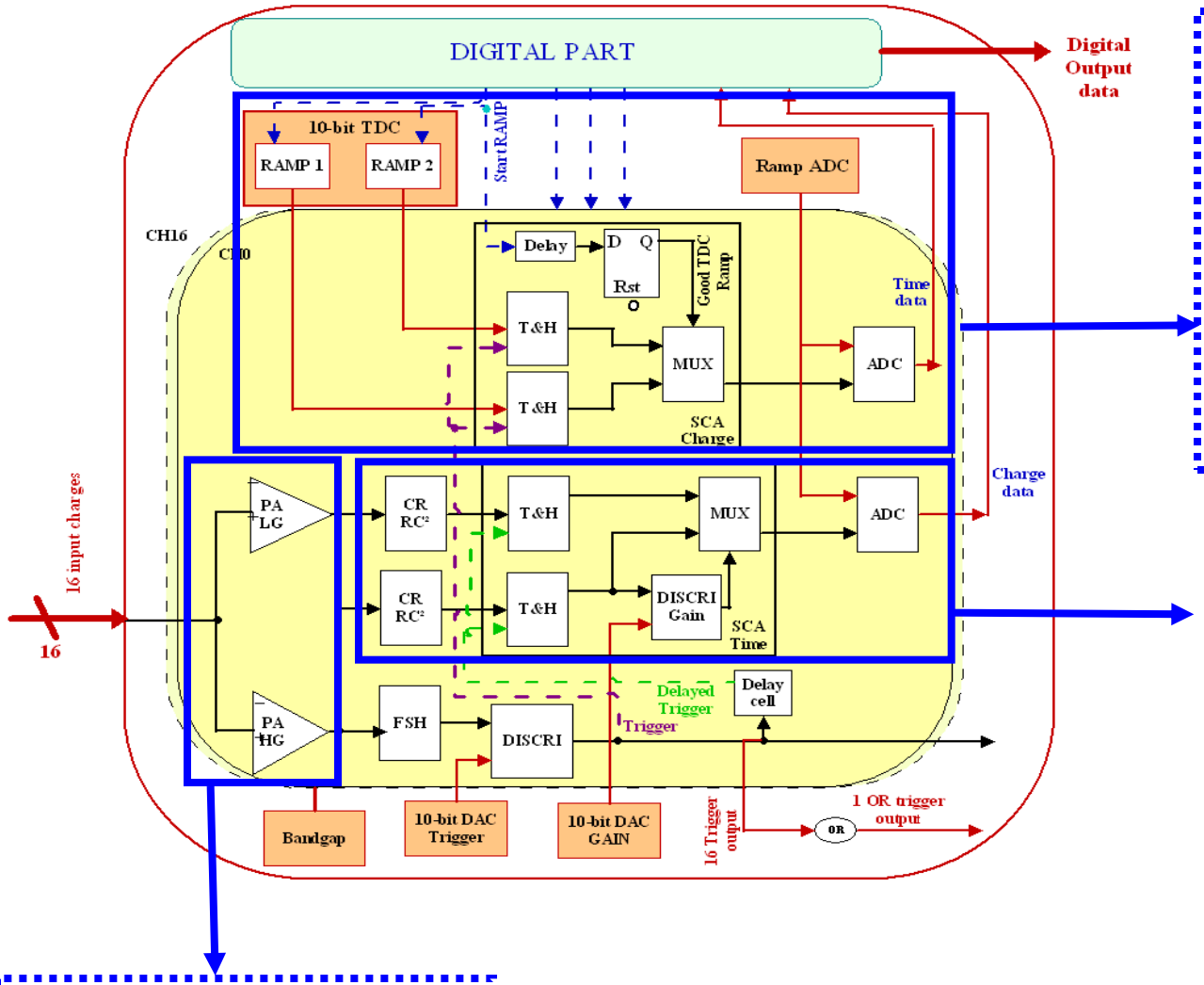
- Photomultiplier Array Integrated in SiGe Read-Out Chip
  - Replace large PMTs (20'') by arrays of 16 smaller ones (12'') , PMm2 project
  - **Smart photodetector**
  - 16 **independent** channels
  - Auto-trigger at 1/3 p.e.
  - Charge (300 pe) and time (1ns) measurement (10-12 bits)
  - Water tight, common high voltage for PMTs
  - Data driven : « One wire out » for DATA and power supplies



- First prototype in 2008
- Second prototype in 2010 (to improve the performances)
- Main applications in large Water Cerenkov
  - **Chip studied by LAGUNA (MENPHYS), LHAASO…**

Demonstrator realized by the IPNO with 16 x 8-inch Hamamatsu tubes

PARISROC: System On Chip



Time measurements

2 systems:

1. Coarse time by 24-bit gray counter (Digital part)
   - working at 10 MHz
   - with 1.67 s of dynamic
   - 100 ns steps
2. Fine time by analog TDC
   - ✓ 100 ns dynamic range
   - ✓ Time resolution: 220 ps
   - ✓ Non linearity: +/- 1ns

Charge measurements

- ✓ Two gain channels to cover the large input dynamic range
- ✓ 2 input preamplifier with adjustable gains (on 8 bits)
- ✓ Shaper with variable shaping time (form 25 ns to 100 ns) and gain
- ✓ Charge resolution: max 0.2 p.e. (32 fC) for 10-bit ADC
- ✓ Dynamic range from 1/3 pe to 600 pe (~ from 50 fC to 100 pC)

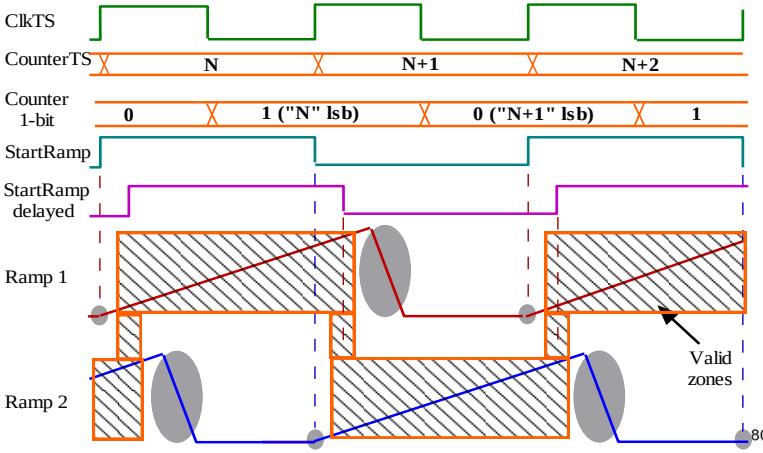
Input stage

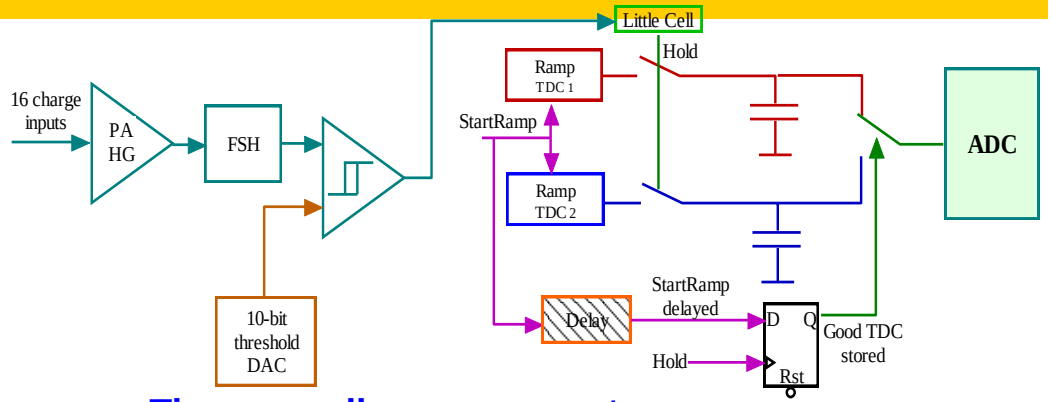
2 input preamplifiers with adjustable gains (on 8 bits)

PARISROC Time measurements

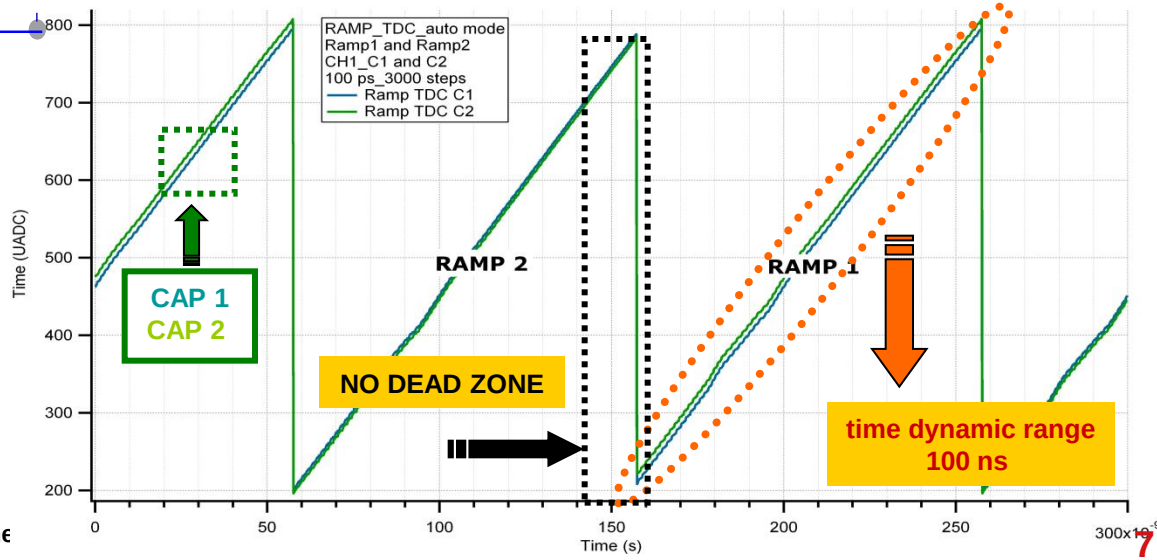
- No TDC integrated in HARDROC
- Time measurements:
  - Ramp TDC: integrated in PARISROC (PMTs) and SPIROC (SiPM)

The TDC ramp has been reconstructed from the time values saved in the analog memory and converted by the ADC (10-bit). The validation of the good ramp is made automatically





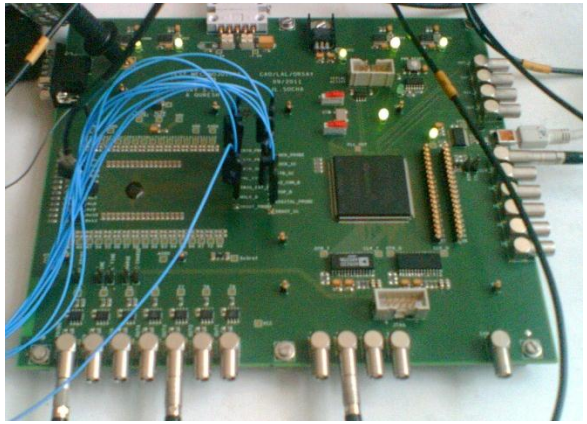
Time overall measurements

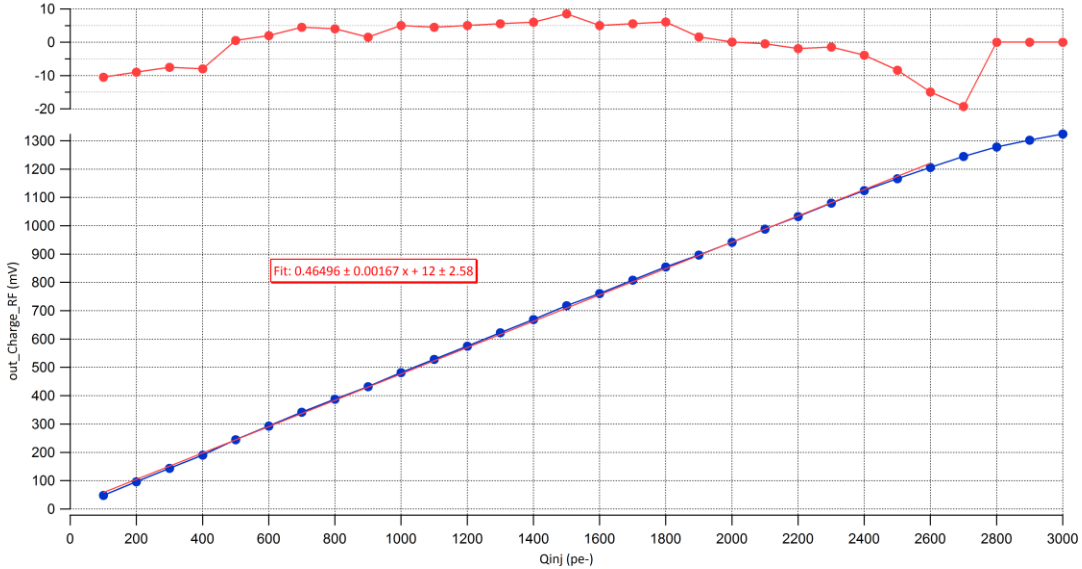


Time dynamic range	100 ns
"Blind zone"	0
linear zone	100 ns
Ramp 1 linear	± 1 ns
Ramp 2 linear	± 1 ns

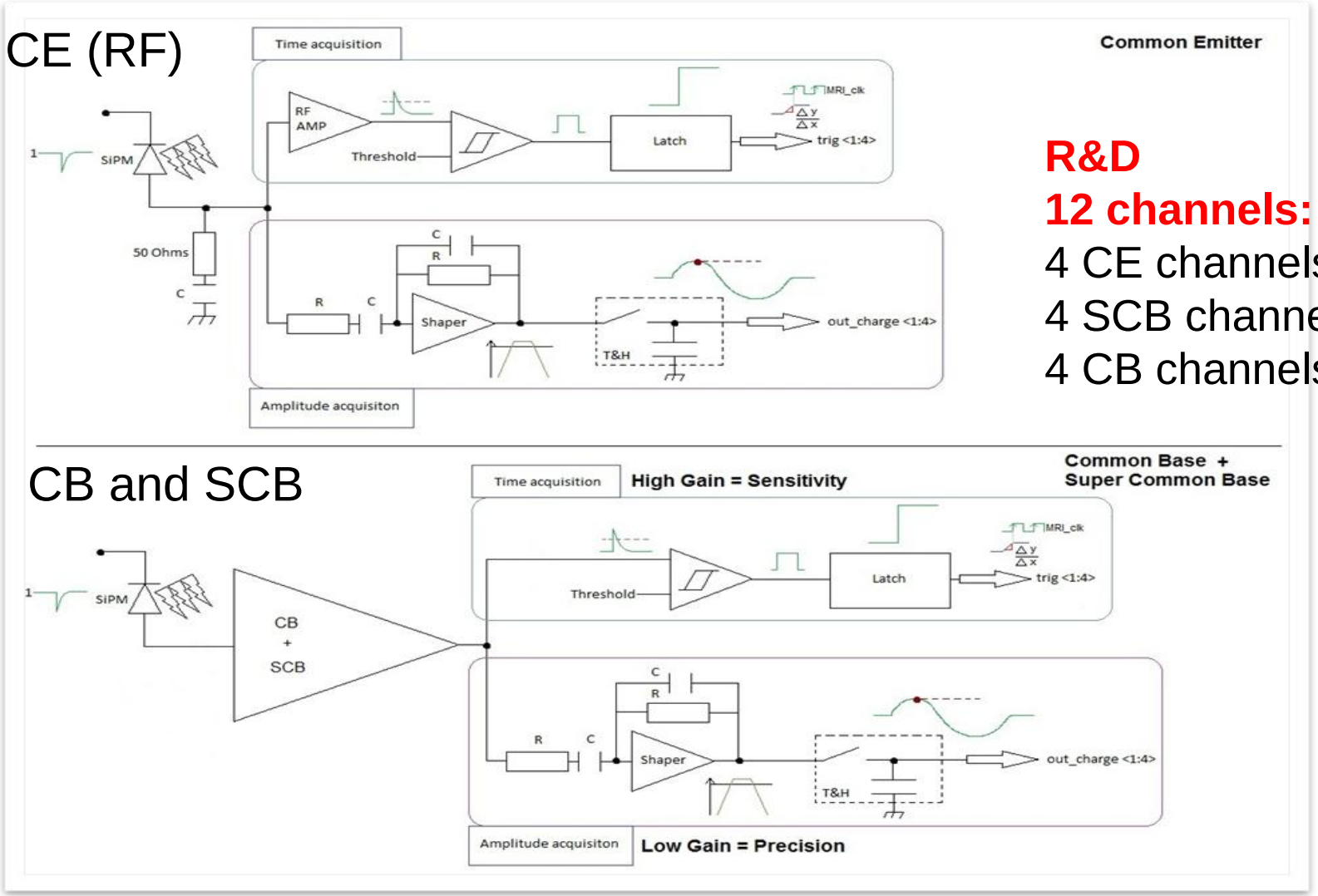
R&D developments => PETIROC

- SiPM readout in 0.35µm SiGe, for physics applications (high resolution time measurements) and therefore also for TOF PET MRI and pre clinical applications
- 12 channels with 3 different architectures (end of 2011)
- High bandwidth preamp (GBWP> 10 GHz), <3 mW/ch, internal TDC (step=25 ps)
- Dual time and charge measurement up to 2500 pe-
- **jitter < 10 ps rms**





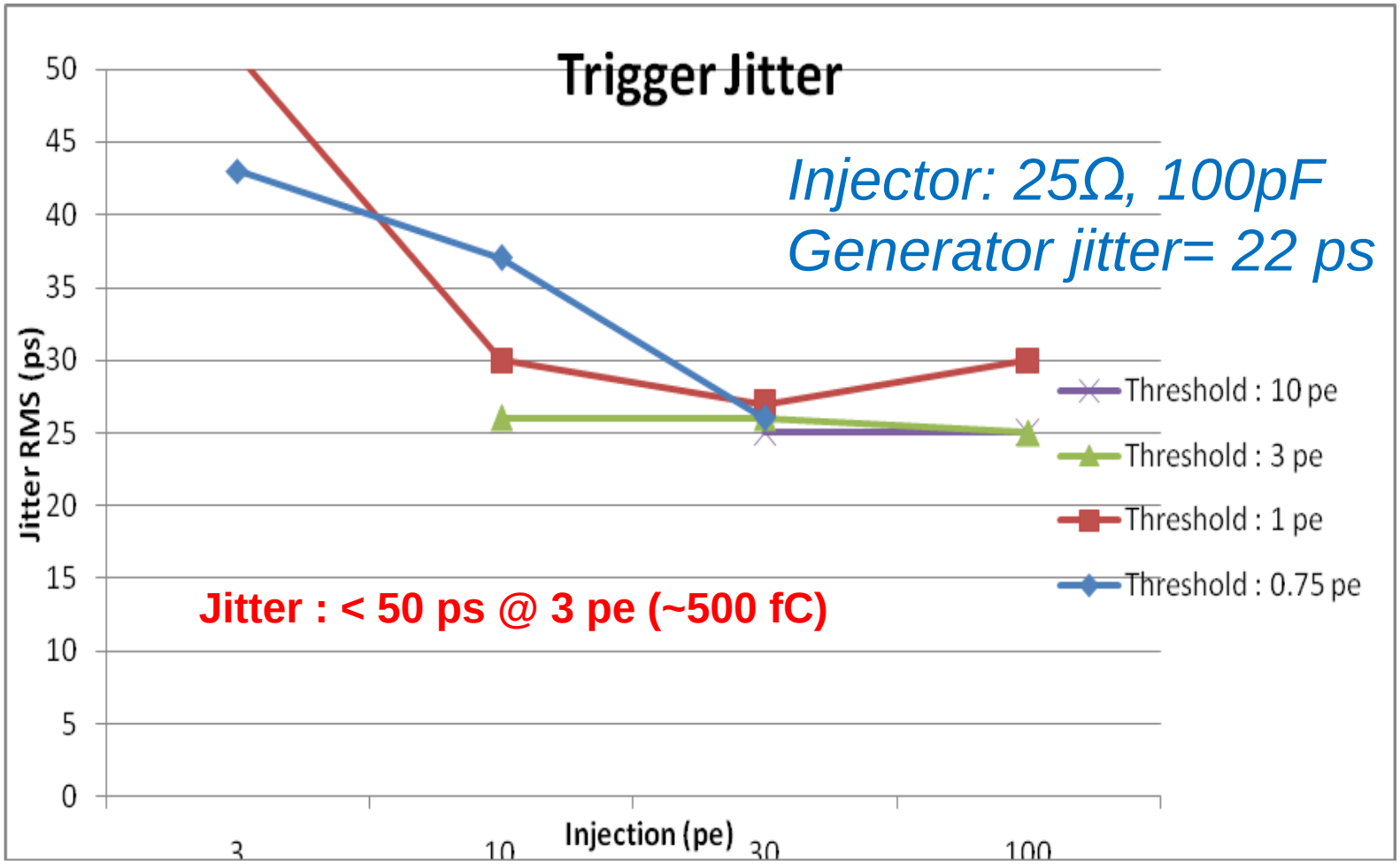
R&D developments => PETIROC



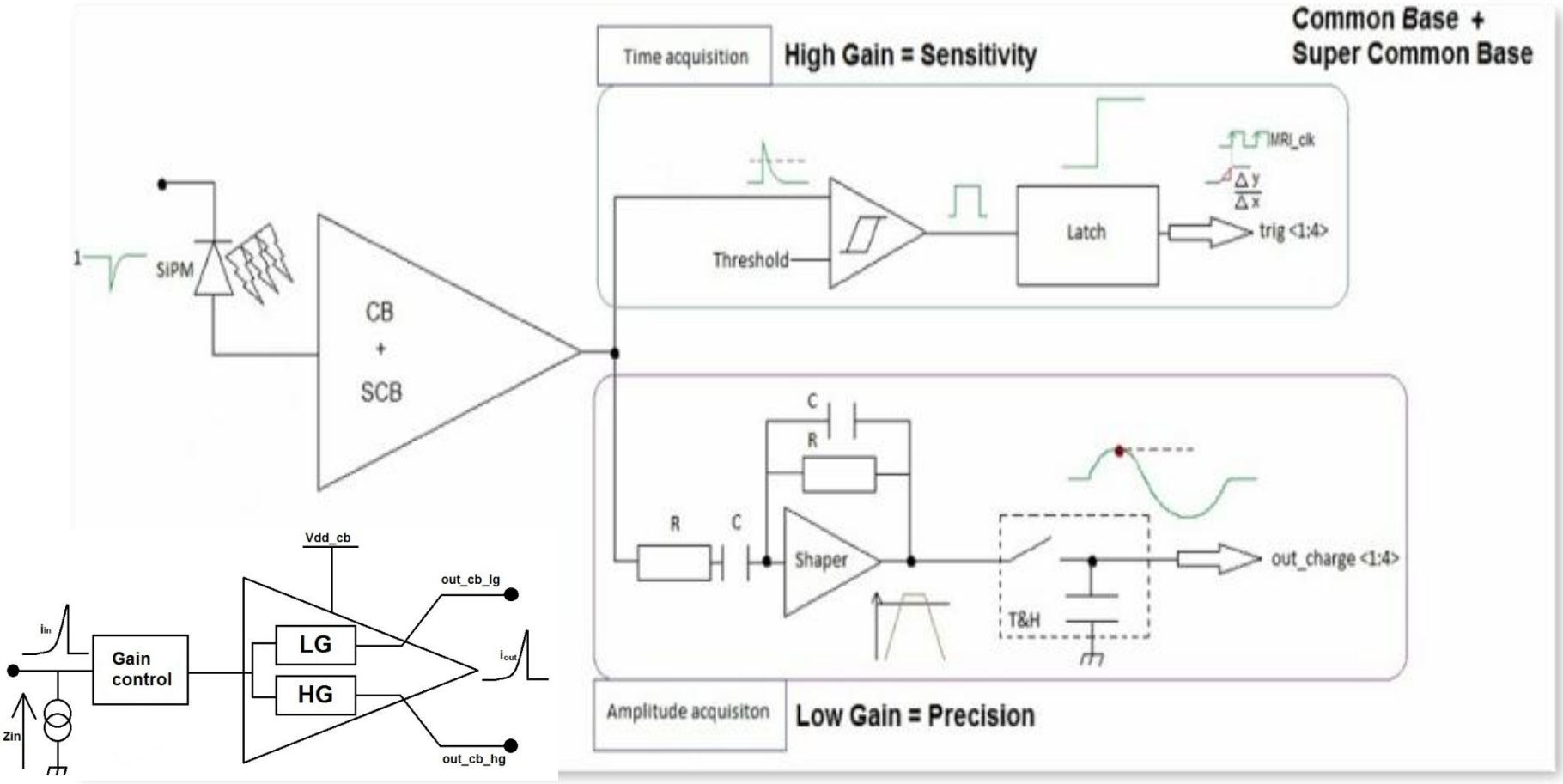
R&D
12 channels:
4 CE channels
4 SCB channels
4 CB channels

PETiROC: PET Integrated ReadOut Chip

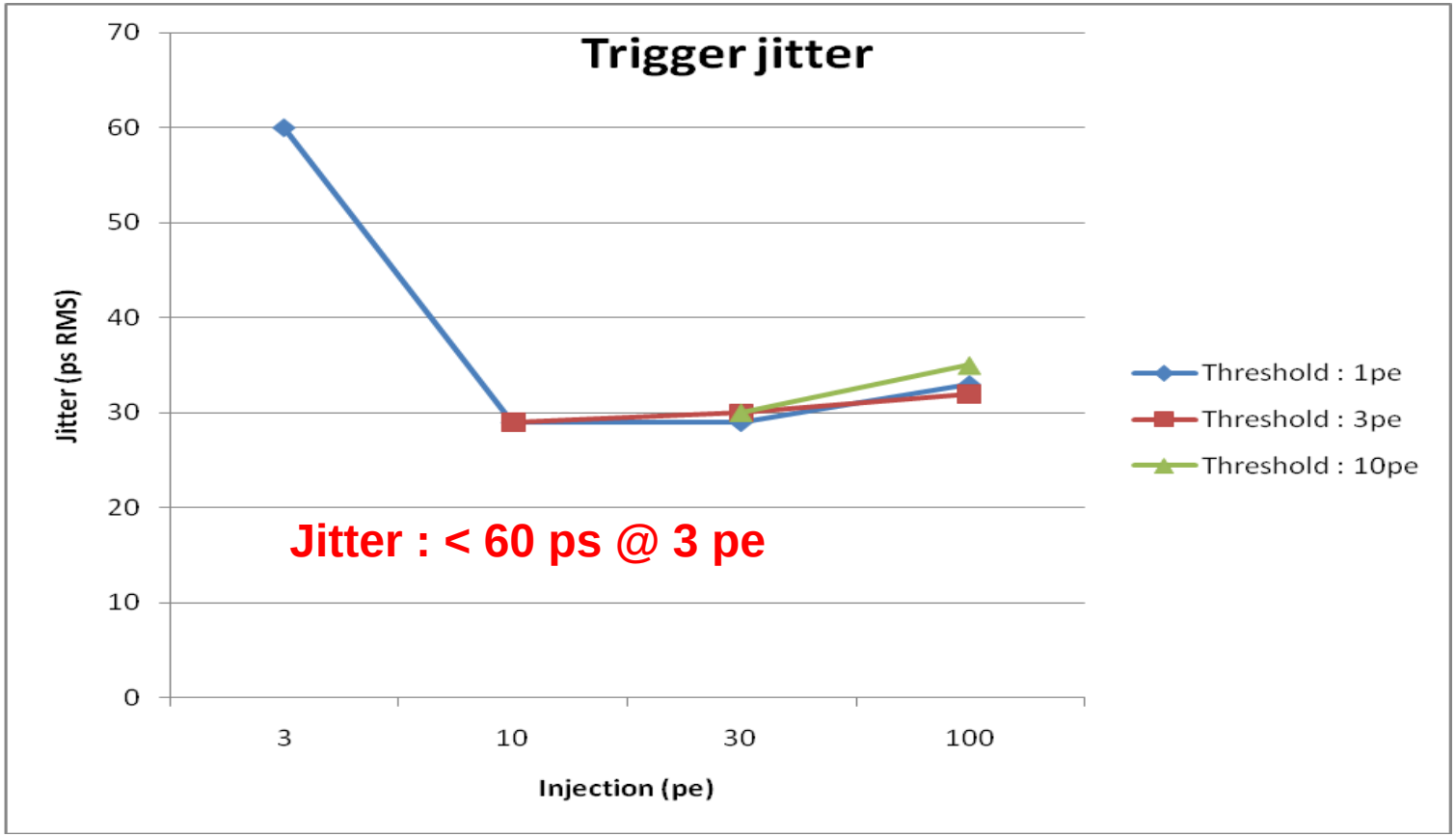
RF amplifier



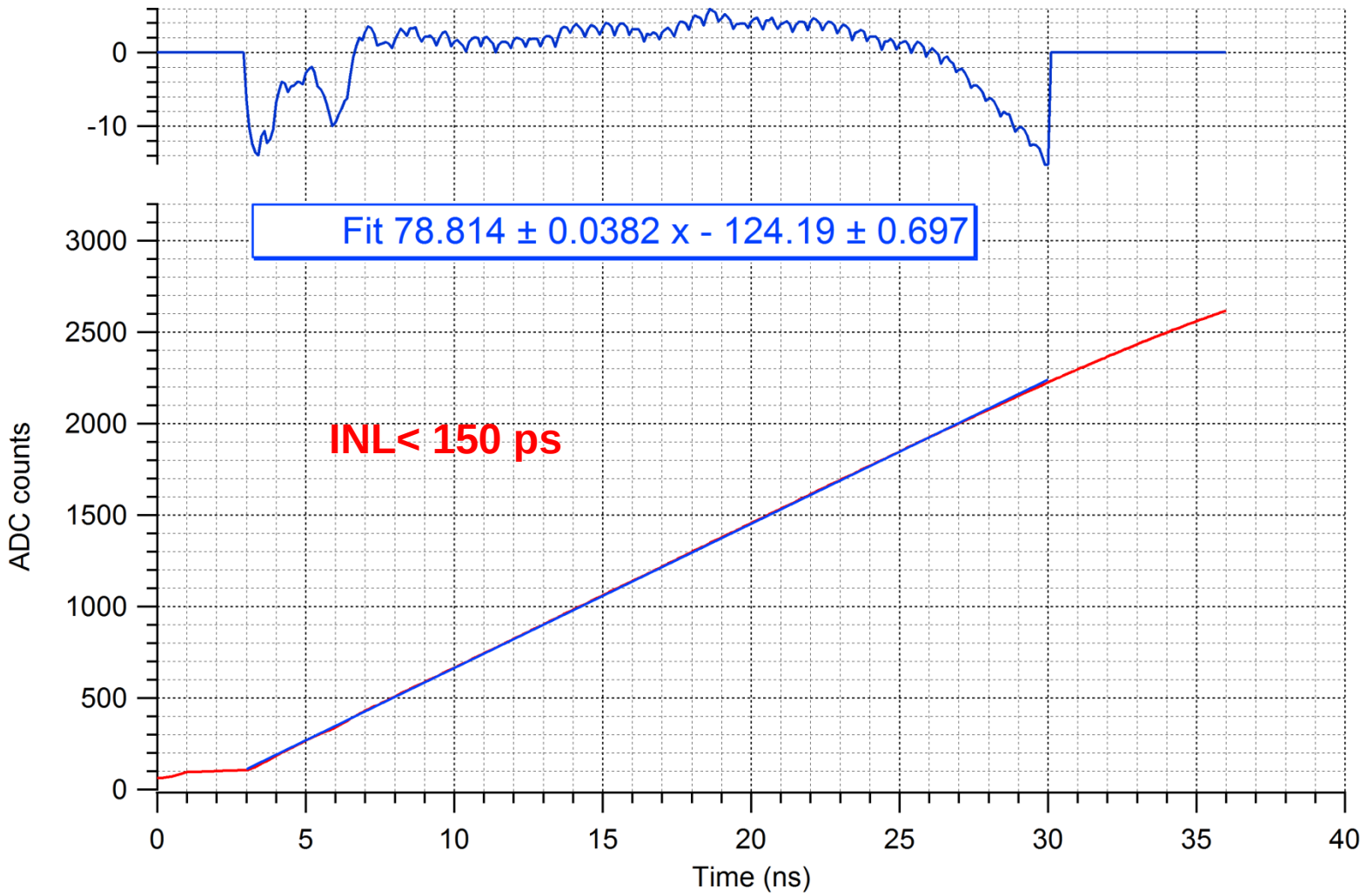
SCB amplifier



SCB amplifier/discri : jitter



TDC linearity



Test bench meas. using a picosecond generator

Testboard #3	RF (Common Emitter)	Common Base	Super Common Base
With 100pf/50 Ohm injector (SiPM emulation)		Vb_cb : 400 #DAC	Vb_scb : 1023 #DAC
Noise floor (pedestal)	185-187 #DAC / 1.196V	216-224 #DAC / 1.259V	340-342 #DAC / 1.514V
Signal value @ 10pe	235 #DAC / 1.300V	137 #DAC / 1.085V	115 #DAC / 1.038V
Signal amplitude @ 10pe (signal minus pedestal)	50 #DAC / 110mV	83 #DAC / 174mV	226 #DAC / 476mV
Gain (mV/pe)	**10.4mV/pe (5 #DAC/pe)**	**17.4mV (8.3 #DAC)**	**47.6mV/pe (22.6 #DAC/pe)**
Jitter - threshold 1 pe @10pe	**13ps RMS**	**6ps RMS**	**8ps RMS**
Jitter - threshold 3 pe @10pe	**8ps RMS**	**6ps RMS**	**8ps RMS**
With 100nF DC block (for voltage gain & BW meas.)	**18mV injection**	**18mV injection**	**7mV injection**
Signal Value	267 #DAC / 1.371V	41 #DAC / 0.884V	192 #DAC / 1.2V
Signal amplitude (signal minus pedestal)	81 #DAC / 175mV	179 #DAC / 375mV	150 #DAC / 320mV
Voltage gain (before 50 ohm bridge => factor of 0 .5)	**4.86 V/V**	**10.4 V/V**	**22.5 V/V**
Bandwidth, after discriminator (Δt 10% T50% meas.)	**Δt : 150ps / 660MHz**	**Δt : 360ps / 280MHz**	**Δt : 400ps / 250MHz**

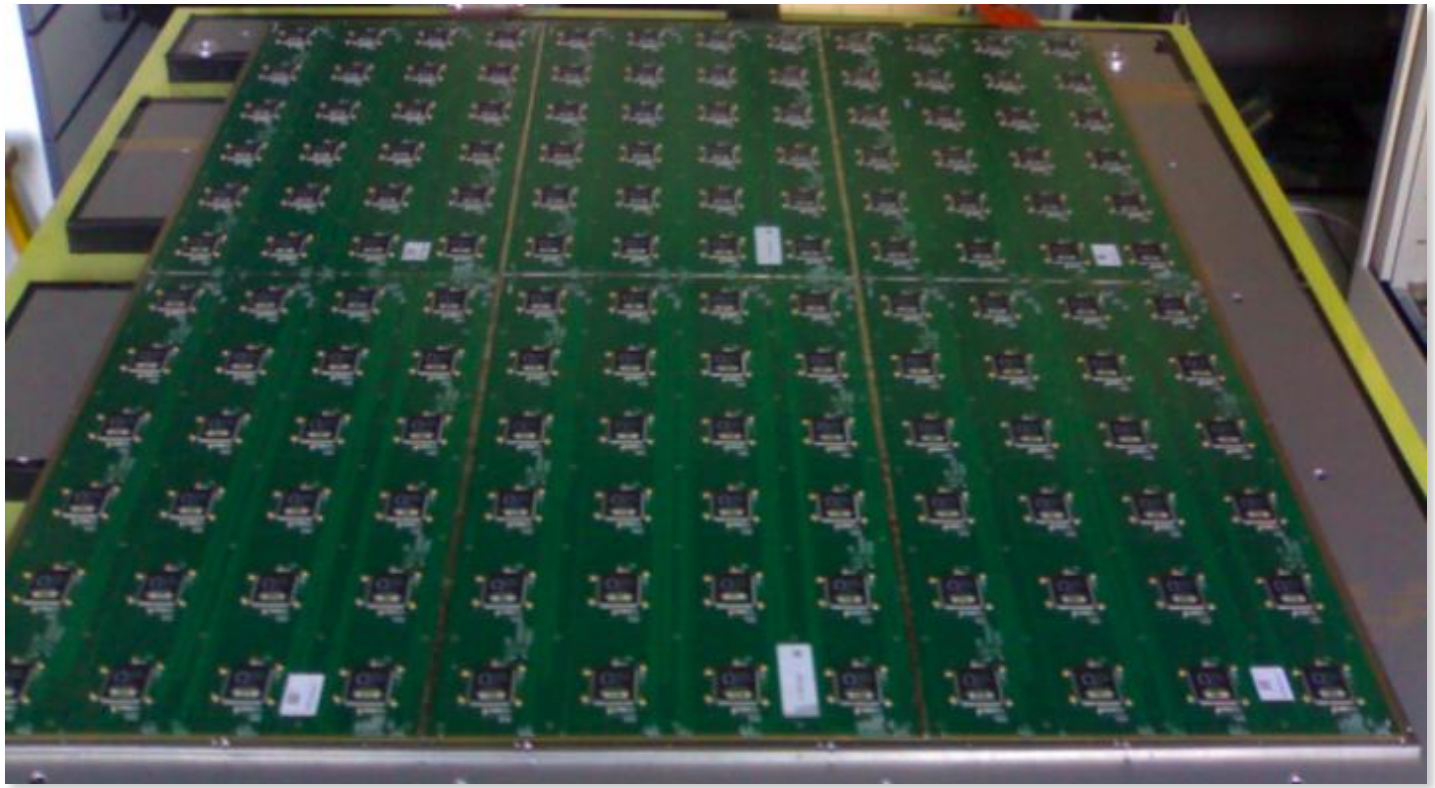
With 1pe-=160 fC

=> DESIGN of PETIROC: 16 channels with RF amplifiers, NO TDC

Conclusion

For High rate GRPC

- Use existing ROC chips:
  - Pads: HR2 + FPGA
  - Strips : voltage preamp , PARISROC
- New ROC chip using FE already integrated and tested in ROC chips (PETIROC)
- Time measurement: ramp TDC of ROC chips or DLL option (MICHRAU micro electronics group Lyon/Clermont)



Backup slides

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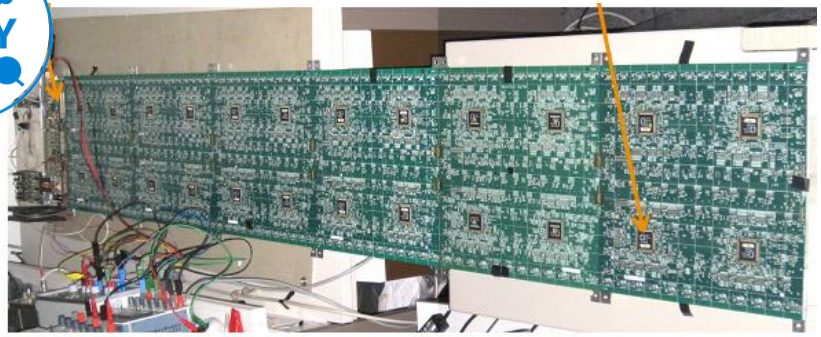
SPIROC: TDC measurements

Two different TDC modes (slow control):

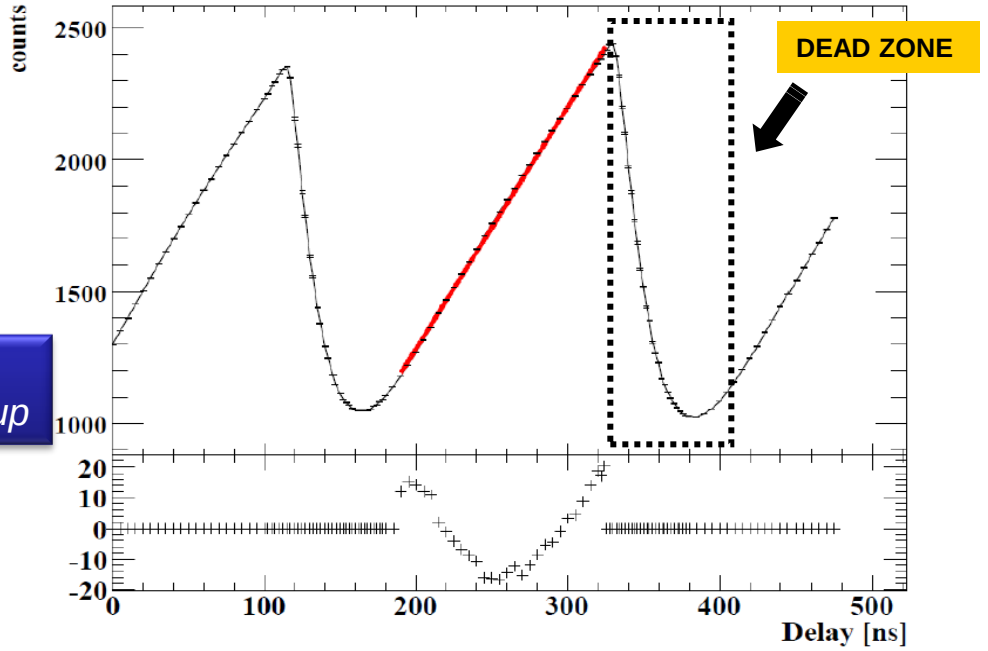
- ILC mode (200 ns to match with the bunch crossing frequency at 5 MHz)
- Testbeam mode (5 µs)

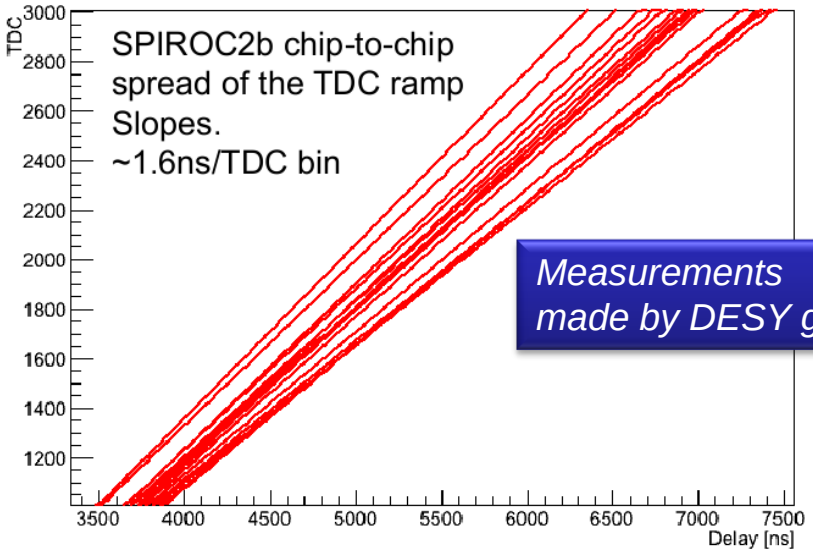
SPIROC2b chip



	ILC mode
Time dynamic range	220 ns
"Blind zone"	100 ns
linear zone	120 ns
Ramp linearity	~ ± 1 ns

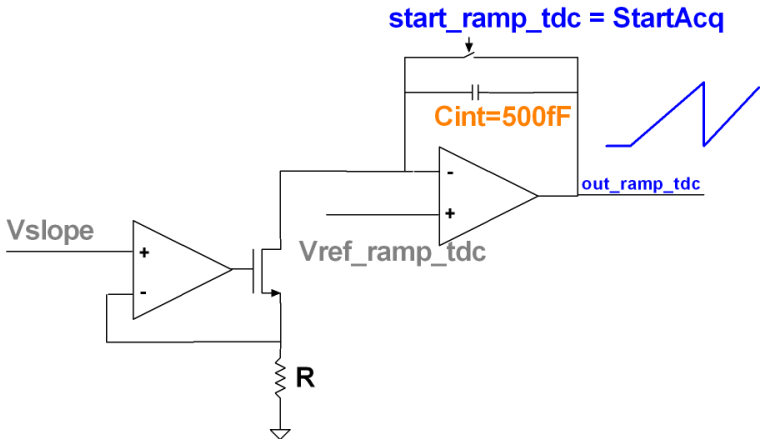
TDC reconstruction in auto-trigger mode by 12-bit ADC
ILC mode

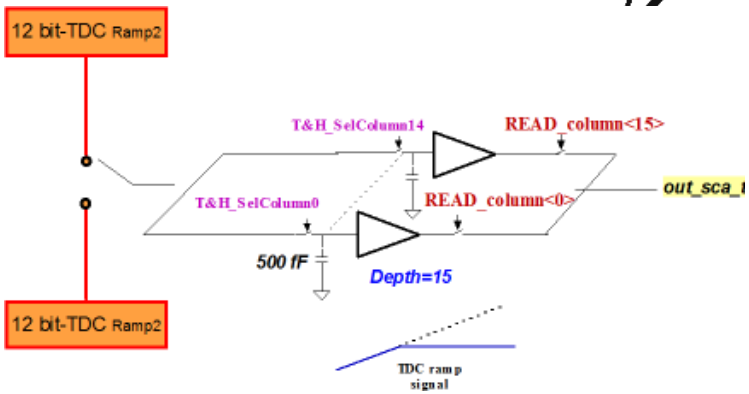


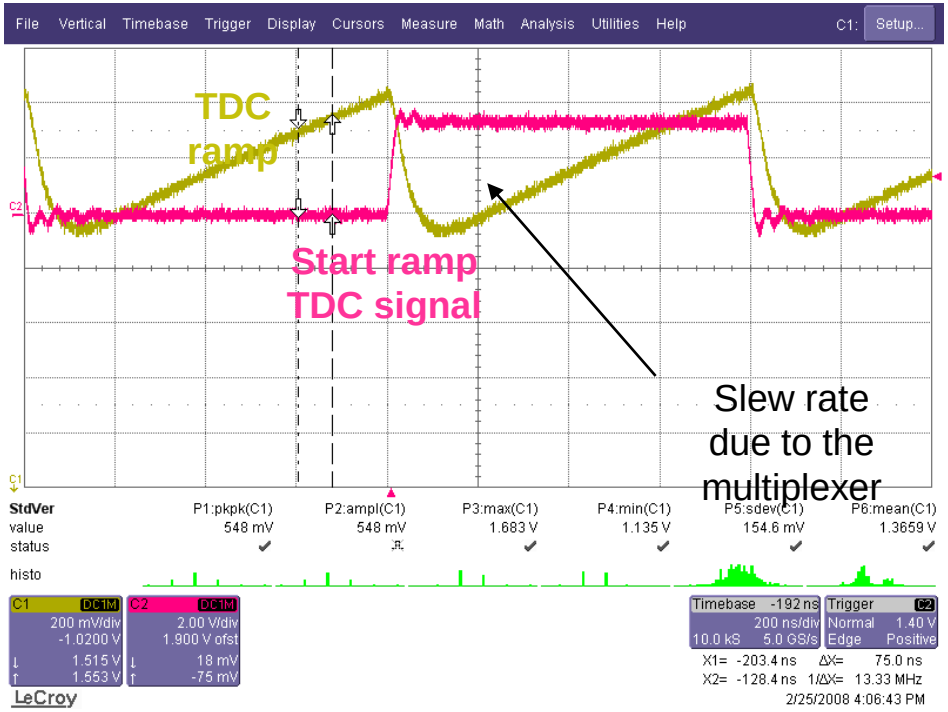


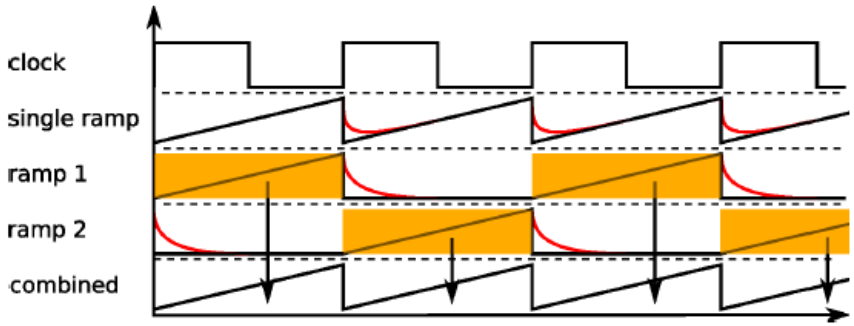
Measurements made by DESY group

SPIROC2b TDC



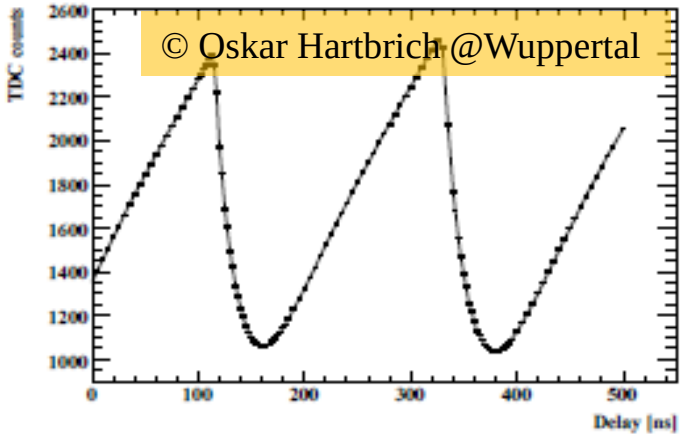






SPIROC 2c: TDC

- SPIROC2B TDC: Dead time due to the mutiplexer



- SPIROC2C TDC
  - To decrease dead time during transition => alternation of a rising and a falling ramp implemented
  - Conservative modification