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Supporting Statistical Semiconductor Device Analysis using EGEE and OMII-UK Middleware

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The only method by which variability in nano-CMOS transistor characteristics (and thus the variability and yield of the circuits making use of them) can be predicted, understood and designed around is through large scale numerical simulation. To capture in detail the statistical parameter distributions in real device architectures requires vast computational resources generating extensive device ensembles. Using resources such as ScotGrid (www.scotgrid.ac.uk), it has been possible, for the first time, to generate an ensemble of more than 100,000 microscopically different 35nm gate length devices –comparable with state-of-art production devices. Early results indicate that designers must assume much larger parameter variations than are currently considered. It is also clear that some of the assumptions underlying present design techniques are no longer valid, due to significant, non-analytic deviations at the extremes of the statistical distribution.

3. Impact

Previously, the sheer number of different device simulations required to properly analyze the statistics of device variability have made solutions impractical with conventional computing resources. However, the availability of HPC resources such as ScotGrid have made such simulations viable. Computation on this scale, however, is not without problems, and whilst using GANGA as a submission interface alleviated difficulties associated with large scale job submission to Globus other difficulties arose resulting in a considerable proportion of rogue jobs. This complicated data management, as it is important to avoid the generation of duplicate devices in order to preserve correct ensemble statistics. In consultation with ScotGrid admins, we have managed to overcome some of these difficulties to produce the first device ensemble of this scale. Work is also on-going exploiting OMII-UK middleware and in particular the use of technologies such as GridSAM for job submission and management.

URL for further information:

http://www.nanocmos.ac.uk/

4. Conclusions / Future plans

Simulation of a 100,000 device ensemble has consumed a considerable amount of computing power - over 11 years of CPU time over the course of approximately 6 weeks. In order to fully understand device variability we must now consider additional physical effects, and simulation of smaller devices. Currently we plan to proceed with the generation of large statistical ensembles for 25, 18, 13 and 9nm devices in order to examine variability at extreme levels of scaling.

Provide a set of generic keywords that define your contribution (e.g. Data Management, Workflows, High Energy Physics)

NanoCMOS transistors, device variability, numerical simulation, OMII-UK, GANGA

1. Short overview

Progressive scaling of CMOS devices has driven the phenomenal success of the semiconductor industry. Silicon technology has now entered the nanoCMOS era with 40nm gate length transistors in production. However the semiconductor industry faces many fundamental challenges which will affect the design of future integrated circuits. The NanoCMOS project aims to apply eScience technologies to this problem. We describe our experiences (good and bad) with EGEE and OMII-UK technologies for this purpose.

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