ATLAS Inner Detector Upgrade for SLHC

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- **Proposed Tracker Layout and Simulations (Radiation and Occupancy)**
- **Sensor and FE Electronics R&D**
- **Microstrip Module and Engineering Concepts**
- **Power, DCS, Opto-electronics, Services, Cooling, …**

Upgrading ATLAS for the sLHC

Trigger Electronics:
- Most front-end electronics can probably stay but need faster clock speed and deeper pipelines
- Extensions to trigger capability required
- Need to maintain L1 output rate (more data per event)
  - Must upgrade detector backend electronics
    - increase bandwidth to deal with more data per event
  - Modify trigger algorithms to deal with high occupancy (and increase thresholds)

L-Ar:
- Performance degradation due to high rates in EndCap.

  (High ionisation gives big voltage drops, electronic is inaccessible, L-Ar boiling!)

TileCal:
- Some radiation damage of scintillators
- Challenging calibration with strong increase in pile-up

Muon systems:
- Degradation in performance due to high rates, in particular in the forward regions:
  - Will need additional shielding for forward region
  - May need beryllium beampipe
  - Aging/radiation damage needs confirmation for SLHC operation
- Huge expense and disruption if chambers need replacement

Inner Detector tracking systems:
- The entire Inner Detector will have to be rebuilt

ATLAS Inner Detector Replacement

**To keep ATLAS running more than 10 years the inner tracker will have to go ...
(Current tracker designed to survive up to 730 fb^{-1} ≈ 10Mrad in strip detectors)**

For the luminosity-upgrade the new tracker will have to cope with:

- **much higher occupancy levels 3000 fb-1**
- **much higher dose rates ~ 300Mrad**

To build a new tracker for 2015, major R&D program already needed.

Steering group (lead Nigel Hessey) and several working groups.

Formal proposal submittal structure.

Timescales:

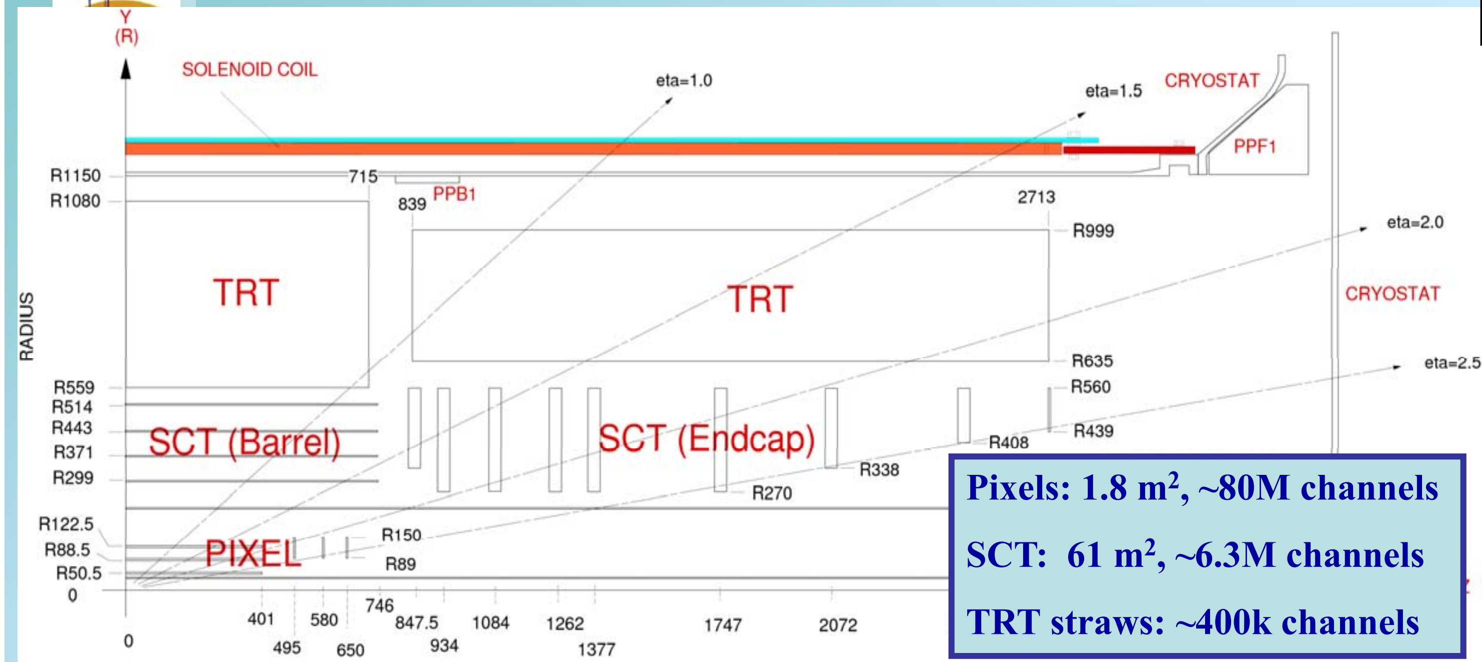
- **R&D leading into a full tracker Technical Design Report (TDR) in 2010**
- **Construction phase to start immediately TDR completed and approved.**

The intermediate radius barrels are expected to consist of modules arranged in rows with common cooling, power, clocking and cooling.

The TDR will require prototype super-modules/staves (complete module rows as an integrated structure) to be assembled and fully evaluated

All components will need to demonstrate unprecedented radiation hardness

Current Inner Tracker Layout

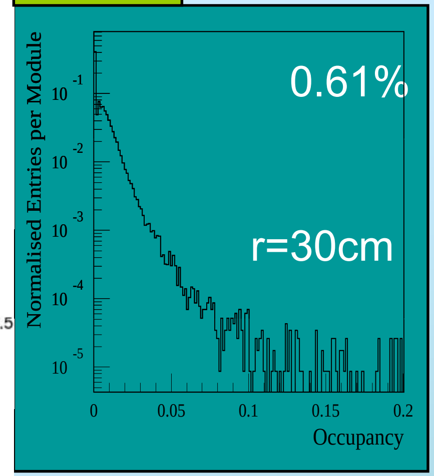


Pixels: 1.8 m², ~80M channels

SCT: 61 m², ~6.3M channels

TRT straws: ~400k channels

ID TDR



Mean Occupancy in Innermost Layer of Current SCT

Pixels (50 μm × 400 μm): 3 barrels, 2 × 3 disks 5cm < r < 15cm

- Pattern recognition in high occupancy region
- Impact parameter resolution (in 3d)

Radiation hard technology: n^+-in-n Silicon technology, operated at -6° C

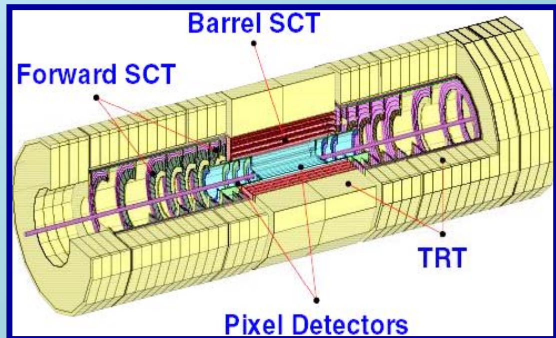
Strips (80 μm × 12 cm) (small stereo angle): "SCT" 4 barrels, 2 × 9 disks

- pattern recognition 30cm < r < 51cm
- momentum resolution

p-strips in n-type silicon, operated at -7° C

TRT 4mm diameter straw drift tubes: barrel + wheels 55cm < r < 105cm

- Additional pattern recognition by having many hits (~36)
- Standalone electron id. from transition radiation

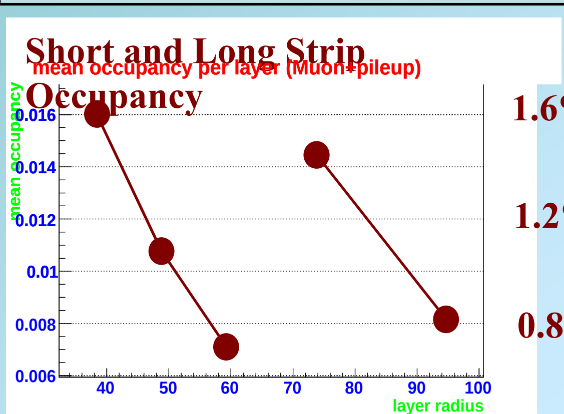


New SLHC Layout Implications

Strawman 4+3+2

Pixels:	r=5cm, 12cm, 18cm, 27cm	z=±40cm
Short (2.4 cm) µ-strips (stereo layers):	r=38cm, 49cm, 60cm	z=±100cm
Long (9.6 cm) µ-strips (stereo layers):	r=75cm, 95cm	z=±190cm

Short and Long Strip Occupancy



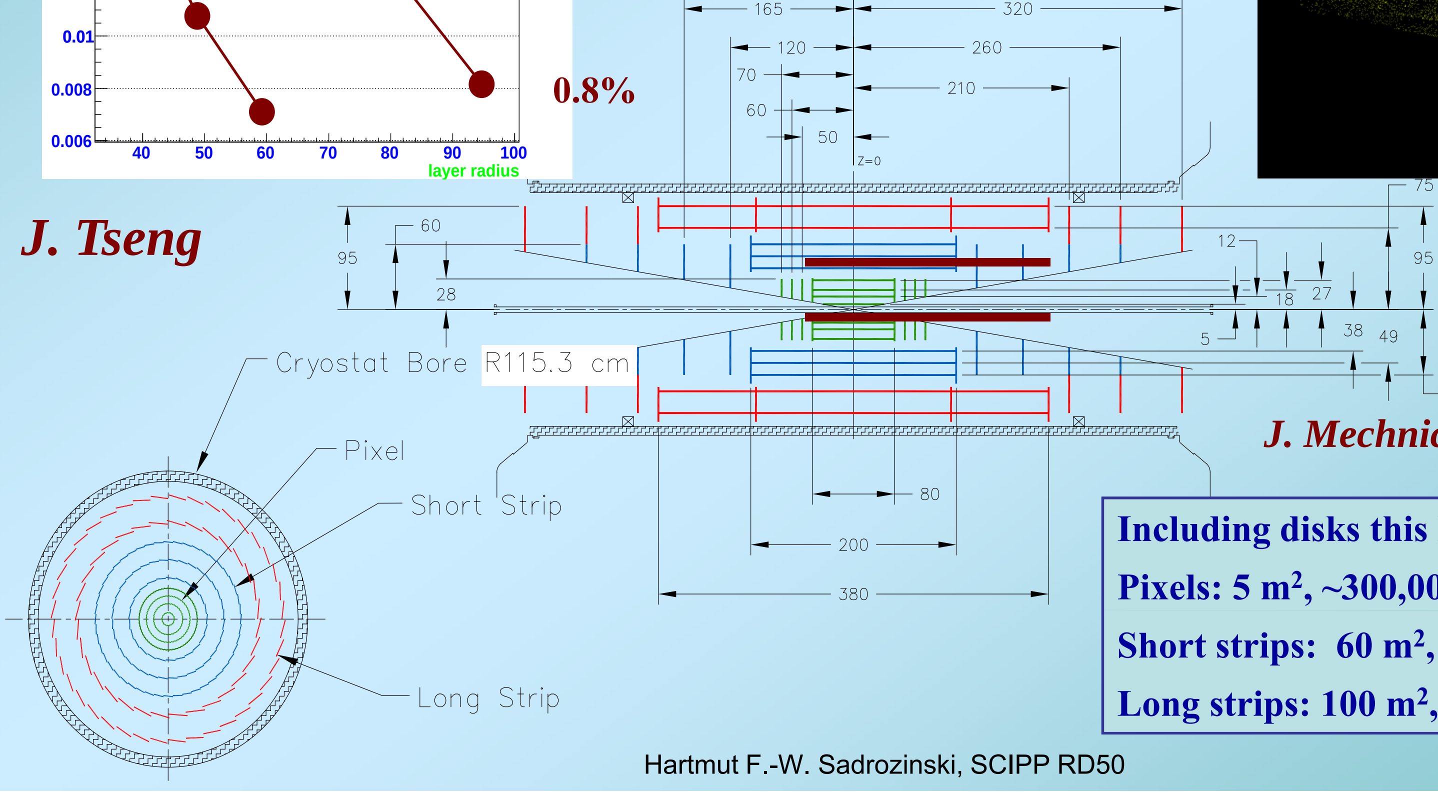
1.6%

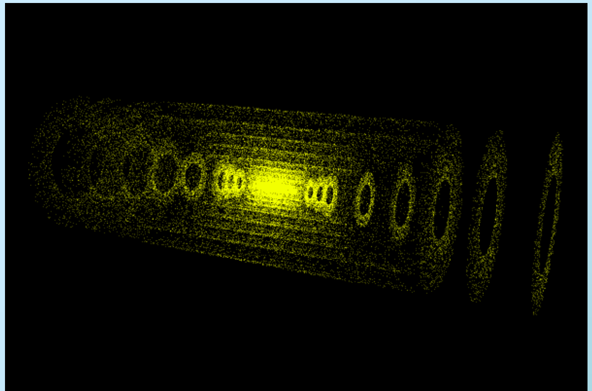
1.2%

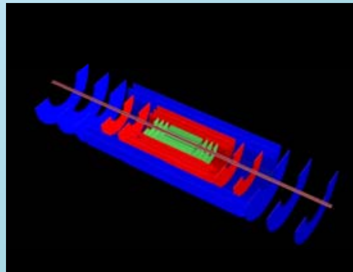
0.8%

Only LO MC (Pythia) . May need to include ×2 safety factor?

J. Tseng







J. Mechnich

Including disks this leads to:

Pixels: 5 m^2, ~300,000,000 channels

Short strips: 60 m^2, ~28,000,000 channels

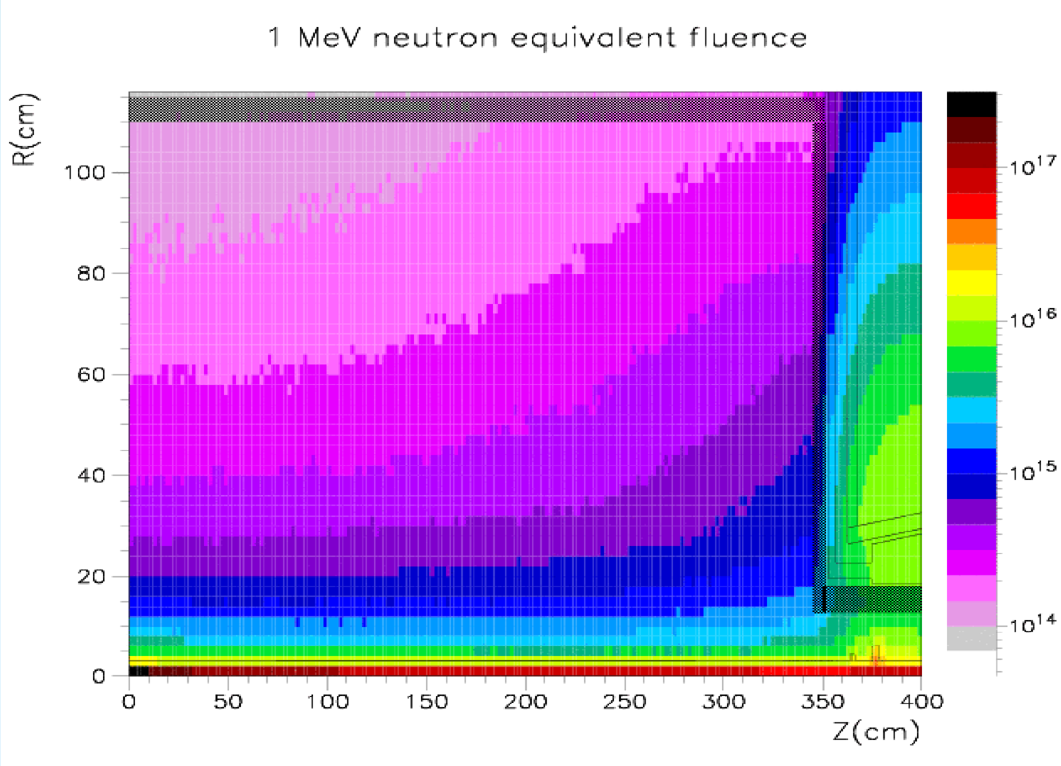
Long strips: 100 m^2, ~15,000,000 channels

Radiation Levels

- With safety factor of two, need pixel b-layer to survive up to $10^{16} n_{eq}/cm^2$
- Short microstrip layers to withstand $9 \times 10^{14} n_{eq}/cm^2$ (50% neutrons)
- Outer layers up to $4 \times 10^{14} n_{eq}/cm^2$ (and mostly neutrons)

→ Issues of thermal management and shot noise. Silicon looks to need to be at ~ -25°C (depending on details of module design).

→ High levels of activation will require careful consideration for access and maintenance.



Quarter slice through ATLAS inner tracker Region, with 5cm moderator lining calorimeters. Fluences obtained using FLUKA2006, assuming an integrated luminosity of 3000fb^{-1}.

Issues of coolant temperature, module design, sensor geometry, radiation length, etc etc all heavily interdependent.

B-layer: Replacement → Upgrade

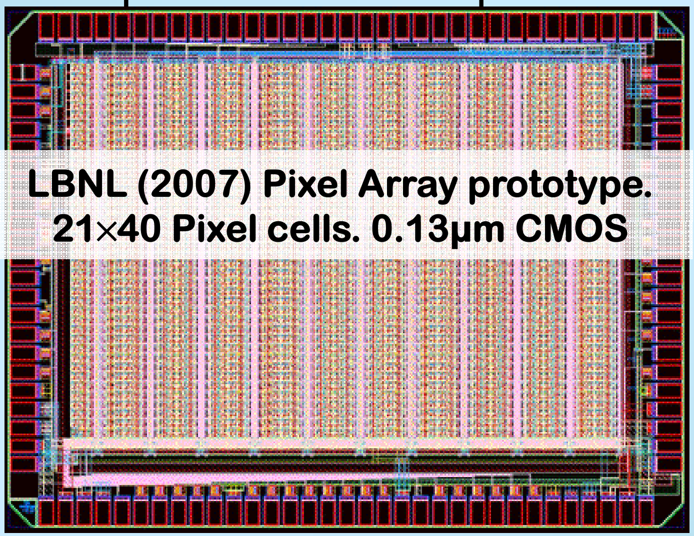
- ATLAS considers to have a B-layer replacement after ~3 year of integrated full LHC luminosity **(2012)** and replace completely the Inner Tracker with a fully silicon version for SLHC (2016).

- The B-layer replacement can be seen as an intermediate step towards the full upgrade. Performance improvements for the detector (here some issues more related to FE chip):
  - **Reduce radius** → Improve radiation hardness (→ 3D sensors, or possibly, thin planar detectors, diamond, gas, …?)
  - **Reduce pixel cell size and architecture related dead time** (→ design FE for higher luminosity, use 0.13 μm 8 metal CMOS)
  - **Reduce material budget** of the b-layer (~3% X_0 → 2.0÷2.5% X_0)
  - **increase the module live fraction** (→ increase chip size, > 12×14 mm^2) possibly use "active edge" technology for sensor.
  - **Use faster R/O links**, move MCC at the end of stave

- The B-layer for the upgrade will need radiation hardness ($10^{15} \rightarrow 10^{16}$ n_{eq}/cm^2) and cope with detector occupancies up to (× 15)

New Pixel FE-ASIC Design

- Design of a new Front-End chip (FE-I4) is going on as a Collaborative Work of 5 Laboratories: Bonn, CPPM, Genova, LBNL, Nikhef
- FE-I4 tentative schedule
  - 9/2007: Architecture definition
  - 10/2007: Footprint frozen
  - 01/2008: Initial Design review
  - 12/2008: Final Design review
- Some prototype silicon made of small blocks and analog part of
- the pixel cell in 0.13 µm.



LBNL (2007) Pixel Array prototype. 21×40 Pixel cells. 0.13µm CMOS

Main Parameter	*Value*	*Unit*
Pixel size	50 x 250	μm^2
Input	DC-coupled negative polarity	
Normal pixel input capacitance range	300Ö500	fF
In-time threshold with 20ns gate	4000	e
Two-hit time resolution	400	ns
DC leakage current tolerance	100	nA
Single channel ENC sigma (400fF)	300	e
Tuned threshold dispersion	100	e
Analog supply current/pixel @400fF	10	µA
Radiation tolerance	200	MRad
Acquisition mode	Data driven with time stamp	
Time stamp precision	8	bits
Single chip data output rate	160	Mb/s

FE-I4 (B-layer Replacement) Specifications: main parameters

3D Silicon Sensors

Charge collection distance reduced
→ reduced charge trapping

ATLAS project	Development, Testing and Industrialization of Full-3D Active-Edge and Modified-3D Silicon Radiation Pixel Sensors with Extreme Radiation Hardness Results, Plans.		
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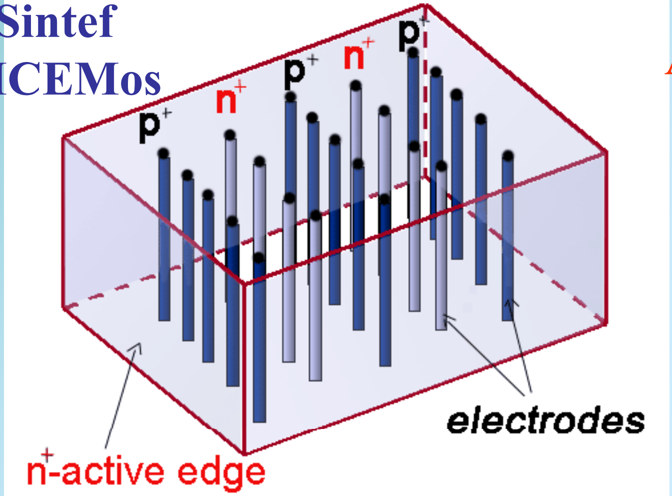
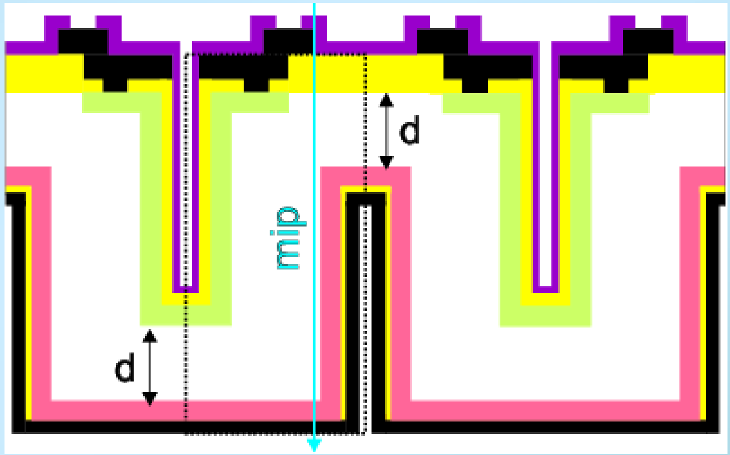
		Modified: 08/03/2007	*Rev. No.:* 2.00

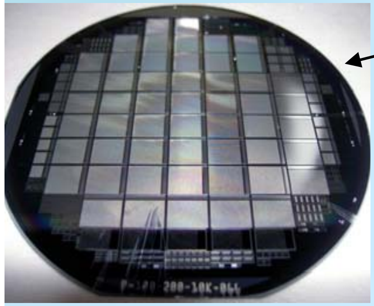
Stanford/Sintef
Glasgow/ICEMos



Alternative geometry with double sided electrodes

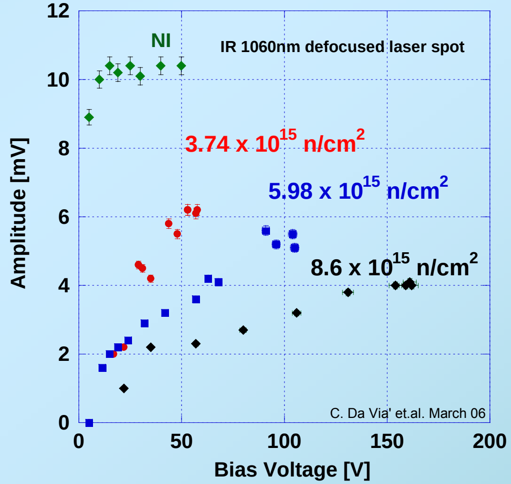


IRST
CNM

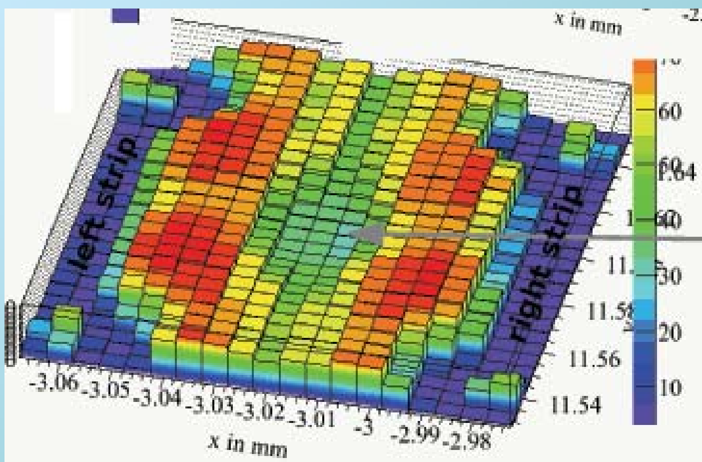


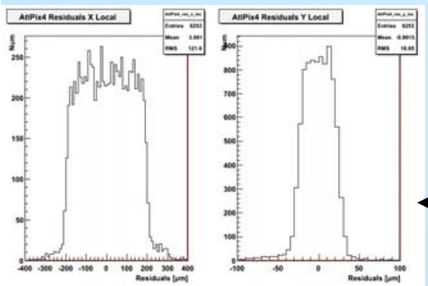
ATLAS pixel fabricated at Stanford

Radiation tests/Praha
CCE(V) with laser



IR scan 3D- SCstrips/ Freiburg



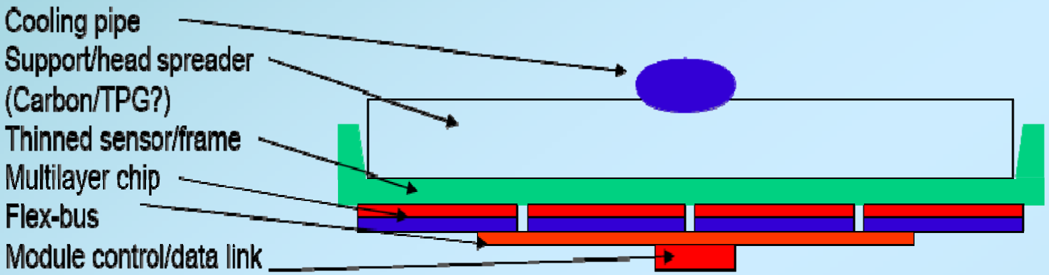


Test beam/data analysis from M. Mathes-Bonn

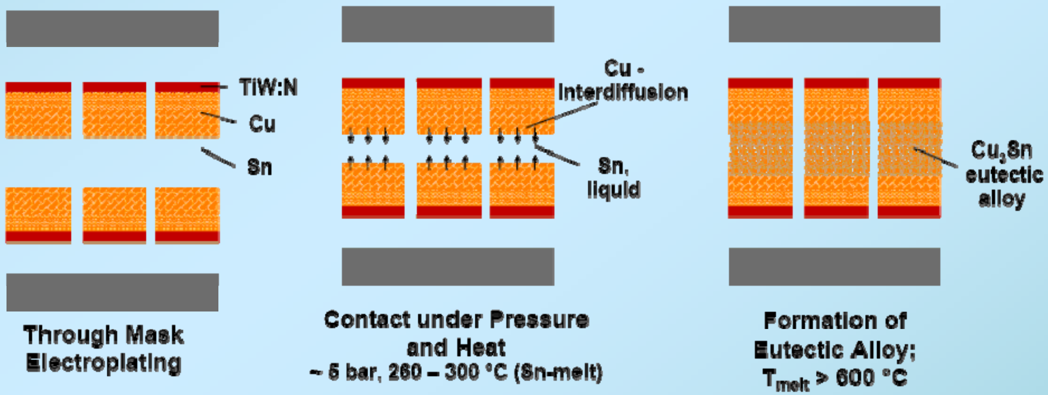
Thin Sensors & Vertical (3D) Integration

- Work already underway in Germany and US
- UK has purchased RD50 wafers for trials adding polyimide layers to Micron sensors
- Survey of companies for MCMD in progress

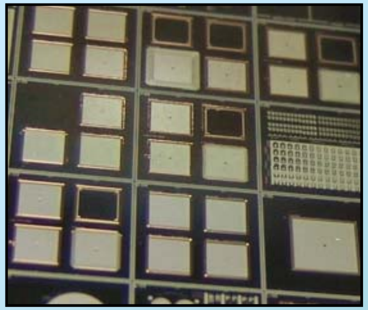
1) Low I_leak, low V_dep
2) Large live-fraction
3) SLID interconnection
4) 3D integration

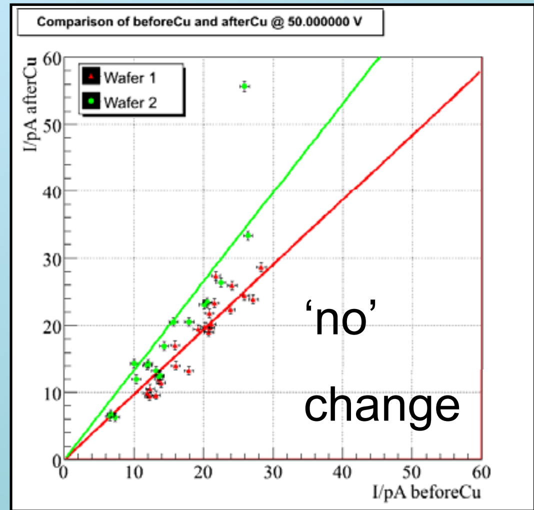


Solid Liquid Interdiffusion (SLID), IZM Munich



First diodes





Conducted by: Bonn, Dortmund, MPI, Oslo, Interon, IZM

pCVD Diamond

Diamond Pixel Modules for the High Luminosity ATLAS Inner Detector Upgrade			
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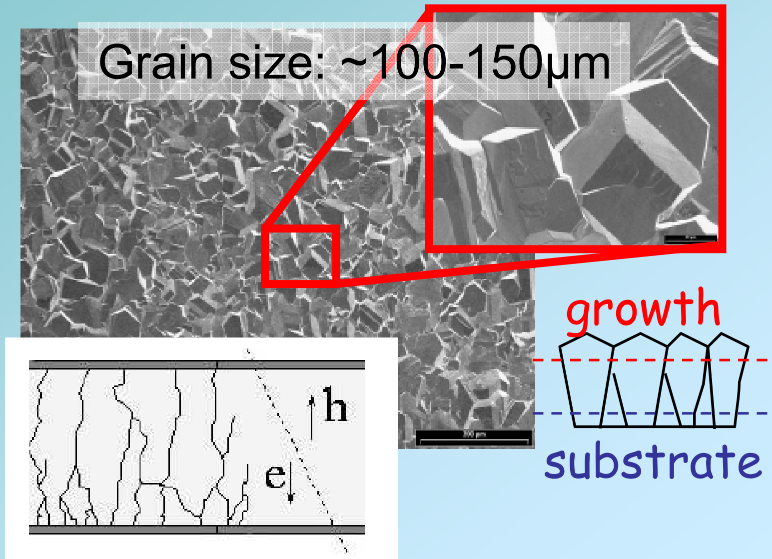
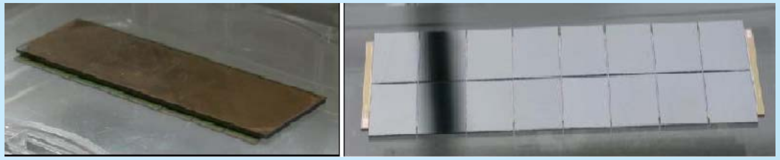
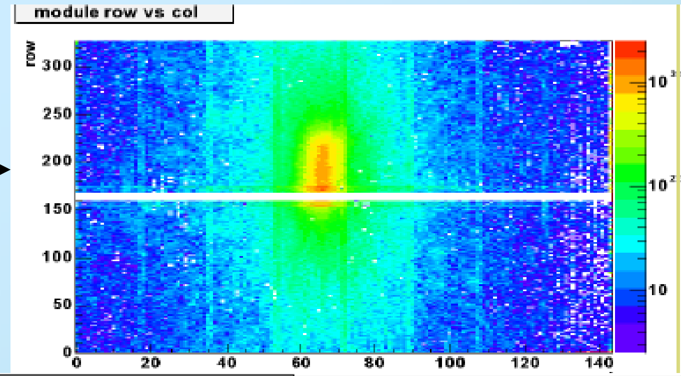


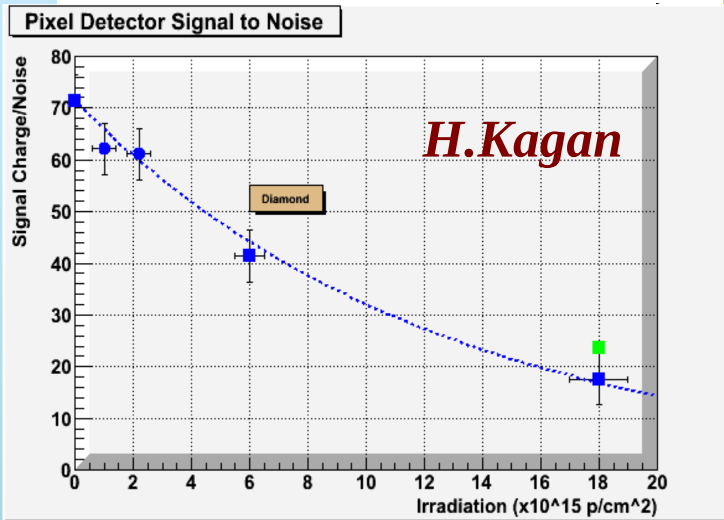
ATLAS pixel module



hitmap

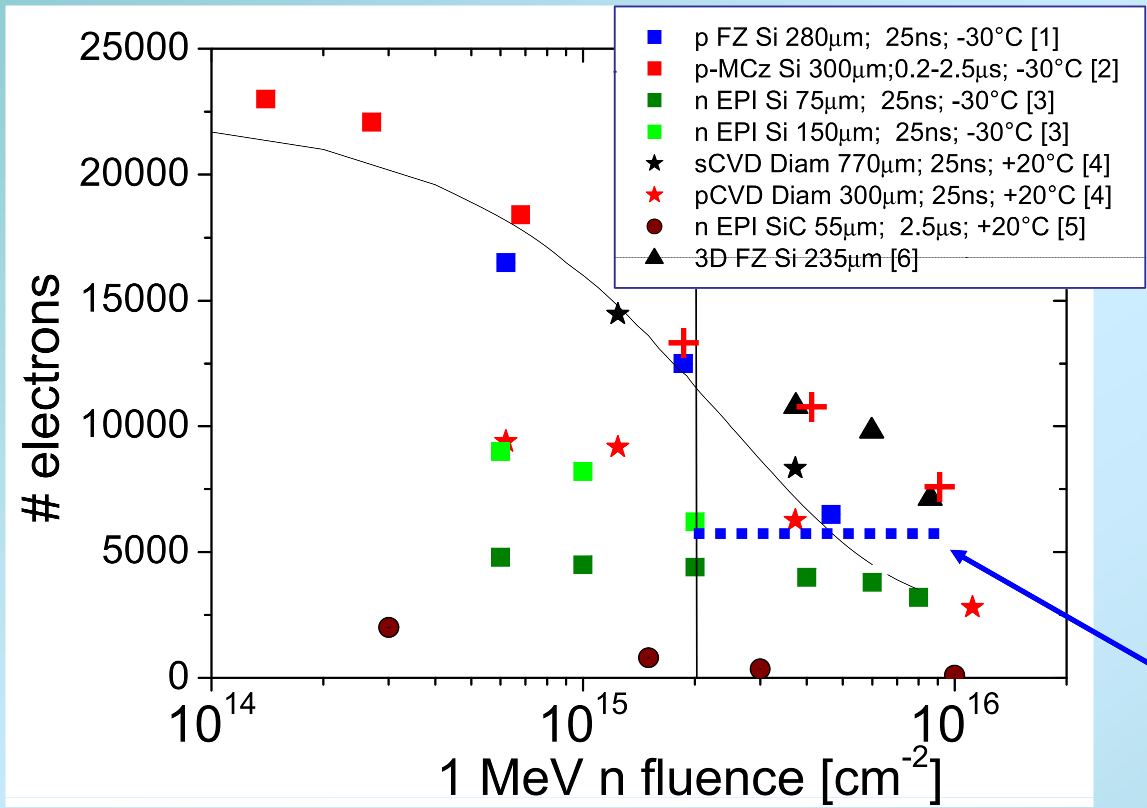


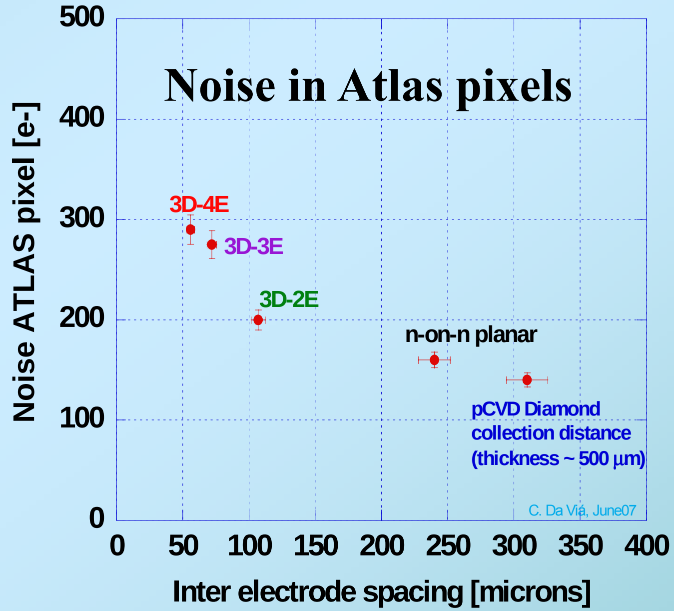
- large band gap and strong atomic bonds promise fantastic radiation hardness
- **low leakage current and low capacitance both give low noise**
- 3 (1.5) times better mobility and 2x better saturation velocity give fast signal collection
- **Ionization energy is high: MIP≈ 2x less signal for same X_0 of SI**
  - –Diamond: ~13.9ke$^-$ in 361 μm (140 enc; bare threshold ~1500e)
  - –SI: ~22.5 ke$^-$ in 282 μm
- Grain-boundaries, dislocations, and defects can influence carrier lifetime, mobility, charge collection distance and position resolution
- Available Size ~2 x 6 cm^2 (12cm diameter wafer; ~2mm thick)



Pixel Signal and Noise

Comparison of measured collected charge on different radiation-hard materials and devices (M. Bruzzi, H. F.-W. Sadrozinski, A. Seiden, NIM A 579 (2007) 754–761)





Pixel Threshold: 20 x noise?
Signal/Noise ~ 40 ?

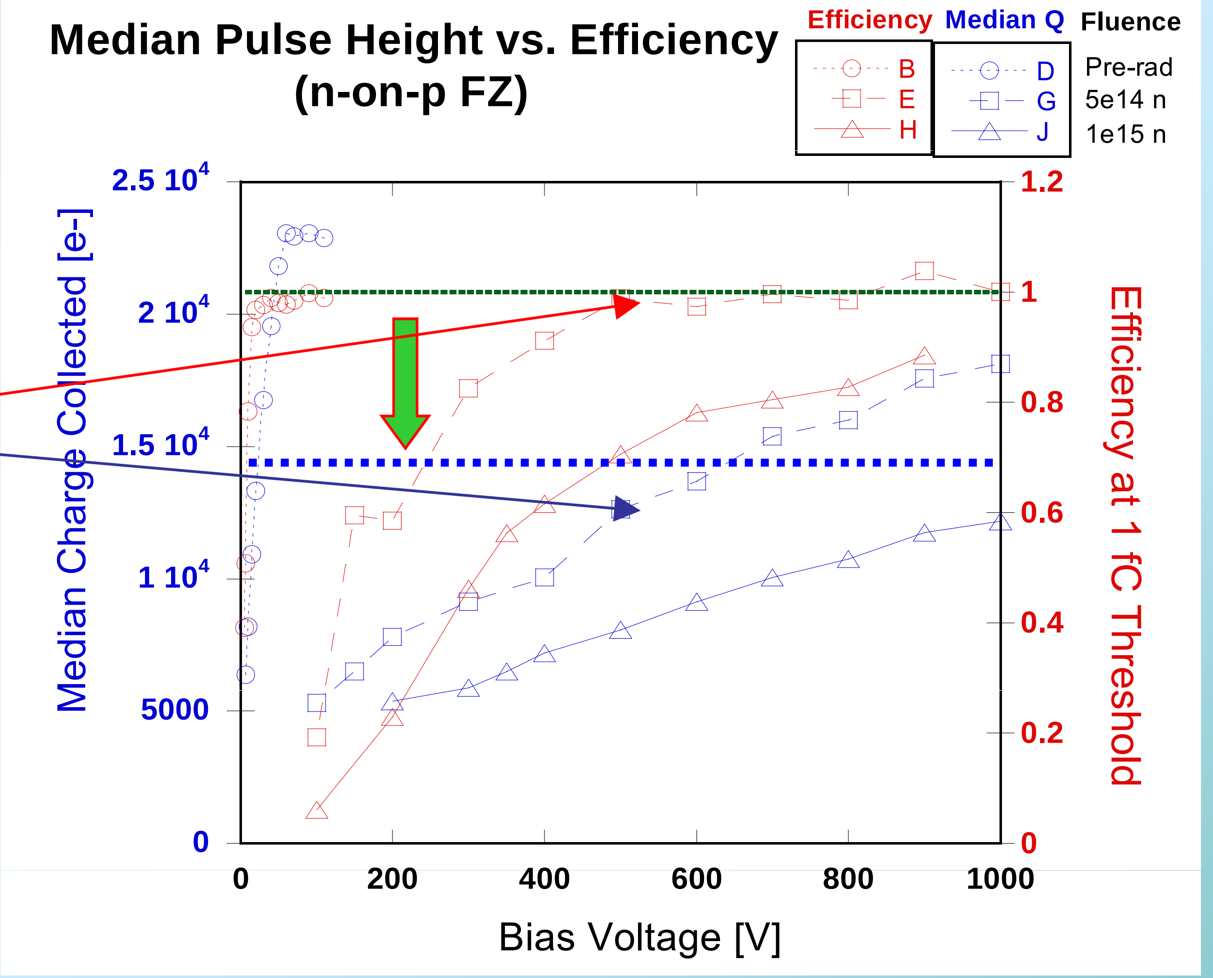
At a fluence of ~10^{15} neq/cm^2,
all planar sensors loose sensitivity: on-set of trapping!

Planar n-in-n or n-in-p:	**Conservative solution but high operating voltages, Protons?**
3D- sensors:	**Highest signal (Efficiency in columns? Commercial fabrication?)**
Diamond:	**Lower currents, low noise (Cost? Uniformity?)**

Comparisons of minimum ionising particle (m.i.p.) CCE(V) and S/N after $10^{16} n_{eq}/cm^2$ needed

Strips: Efficiency vs. Collected Charge

- For tracking sensors with **binary readout**, the **figure of merit** is not the collected charge, but the **efficiency**.
- **100% efficiency** is reached at a signal-to-noise ratio of **S/N ≈ 10**.
- For **long strips** (5e14 cm^{-2}) with a signal of about 14ke, the usual threshold of 1fC = 6400 e can be used.
- For **short strips** (1e15 cm^{-2}) with a signal of about 8ke, the threshold needs to be reduced to about 4500 e, i.e. electronics must be designed for a noise of ~700e.

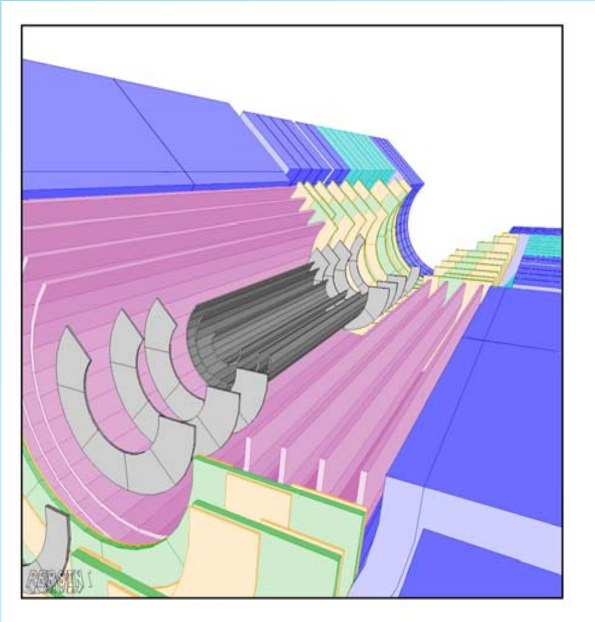


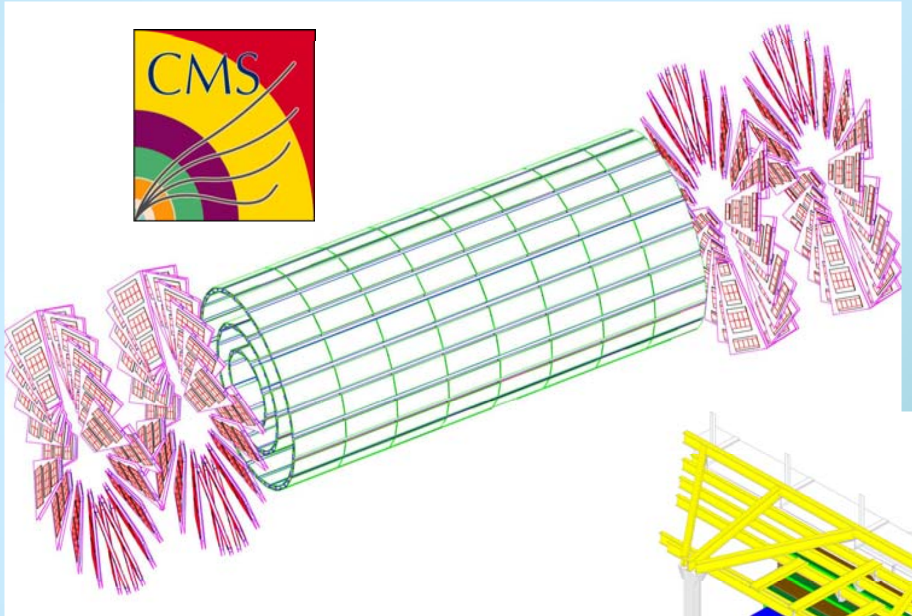
Short strips efficient if threshold can be lowered

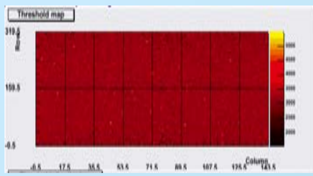
Innermost Detectors at Current LHC

LHC vertex detectors all use n^+ implants in n^- bulk:

- Because of advantages after heavy irradiation from collecting electrons on n^+ implants, the detectors at the LHC (ATLAS and CMS Pixels and LHCb Vertex Locator) have all adopted the n^+ in n^- configuration for doses of $5 - 10 \times 10^{14}\ n_{eq}cm^{-2}$
- Requires 2-sided lithography

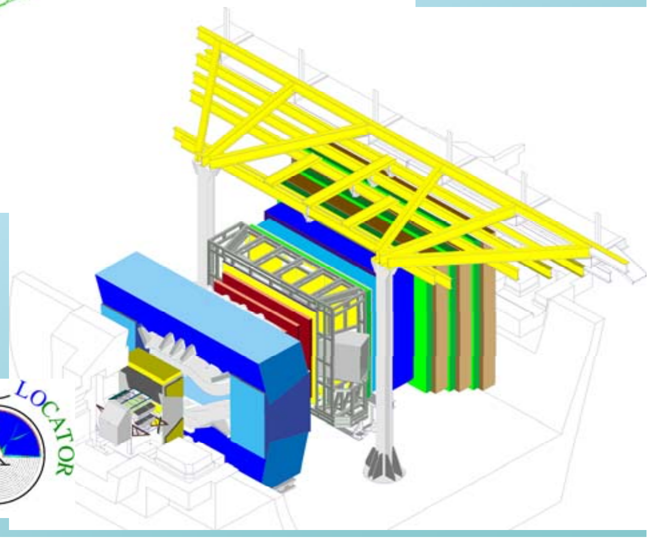






ATLAS 100 million Pixels

LHCb
Vertex Locator
Z(mm)=0-990



SSD Development for ATLAS Upgrade Tracker

Development of non-inverting Silicon strip detectors for the ATLAS ID upgrade			
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		Modified: **18/05/2006**	*Rev. No.:* **1.04**

Institution	P-type SSD	Strip Isolation	HV design	Modules constr.	Mech. Structures cooling	Hybrids,Readout	Electr. Ch	Laser CC	CCE	Trapping	Oper. Par
KEK	x	x	x	x	x	x	x	x	x	x	
Tsukuba						x	x	x	x	x	x
Liverpool	x	x		x	x		x	x	x	x	
Lancaster							x		x		x
Glasgow				x			x	x?	x	x?	
Sheffield					x	x	x		x		
Cambridge						x	x		x		
QML				x			x				
Freiburg				x		x		x	x		
MPI	x	x	x				x				
Ljubljana							x	x	x	x	
Prague							x	x	x		
Barcelona	x	x	x	x		x	x		x		
Valencia	x	x		x		x	x		x		
Santa Cruz									x	x	x
BNL	x	x	x								
PTI	x	x					x	x		x	

ATLAS07 Sensor (HPK) n-on-p FZ

Development of non-inverting Silicon strip detectors for the ATLAS ID upgrade			
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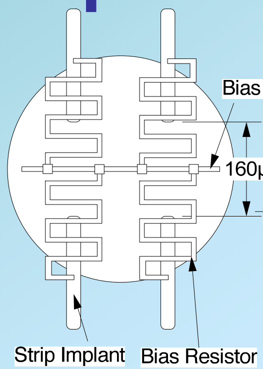
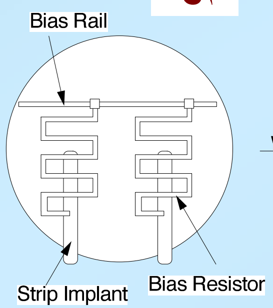
		Modified: 18/05/2006	Rev. No.: 1.04

- Strip segments
  - 4 rows of 2.38 cm strips (each row 1280 channels)
- Dimension
  - Full square
- Wafer
  - 150 mm p-type FZ(100)
  - 138 mm dia. usable
  - 320 µm thick
- Axial strips
  - 74.5 µm pitch
- Stereo strips
  - 40 mrad
  - 71.5 µm pitch
- Bond pads location
  - accommodating 24-40 mm distances
- n-strip isolation
  - P-stop
  - P-spray
  - P-stop + P spray

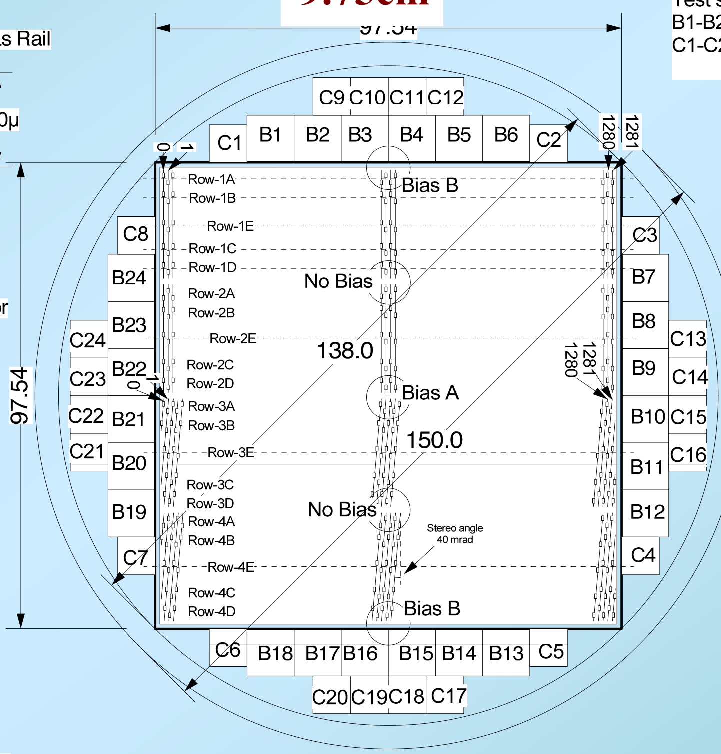


Bias A



Bias B

9.75cm

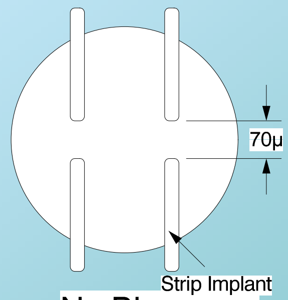


Axial-Stereo Sensor

Test structures (TS):
B1-B24: 1cm x 1cm Miniature sensors
C1-C24: 8mm x 8mm Monitor Diodes
and Vendor TS

Pad distances:
(X=A,B,C,D,E)
1X-2X=23890
1C-2D=27590
1E-2C=31300
1E-2D=35000
1B-2C=38710

Y. Unno



No Bias

Sensors	Preseries		Split1		Split2		Split3		Total
Features	p-stop	p-spray+p-stop	p-stop		p-spray+p-stop		p-spray+p-stop removed		
Wafer	FZ1		FZ1	FZ2	FZ1	FZ2	FZ1	FZ2	
Main sensors	6	6	35	40	8	13	14	13	135
Miniature sensors (Zone1,2,3 inclusive)	72	72	420	480	96	156	168	156	1620
Test structures	12	12	20	20	20	20	20	20	144
Monitored diodes	12	12	20	20	20	20	20	20	144
Total	102	102	495	560	144	209	222	209	2043

Microstrip Front-end ASIC (ABCn) Status

Front-End	Opt. short strip done Layout started	33mA/chip ✓ 750enc (2.5cm strips) Final S/N > 10 ✓
Back-End	Main change in DCL block to handle 160MHz	92mA/chip at 2.5V estimated
Powering	Integrated shunt regulators possible	Current limits to impose uniformity
Floor Plan	First Checks now	7.5mm by 6±1mm
P&R	Examples with pipeline and derandomizer OK	
Submission	Scheduled January 2008	Deliver by April

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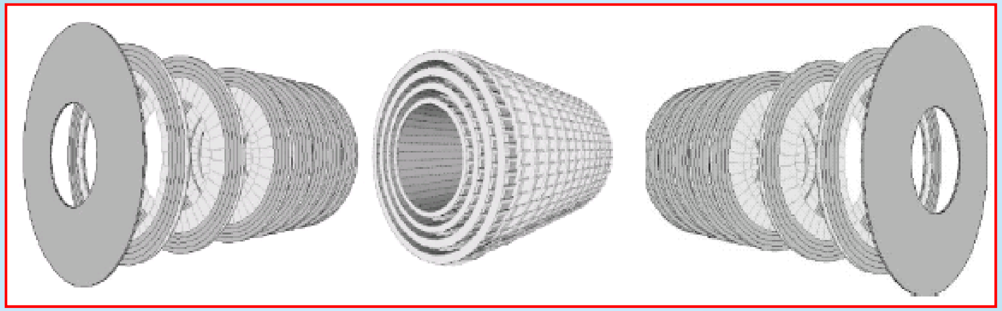
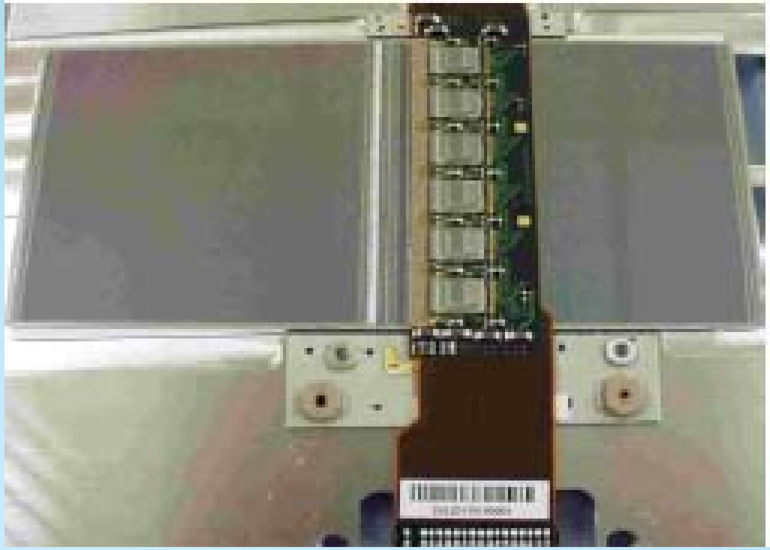
Current SCT ATLAS Module Designs

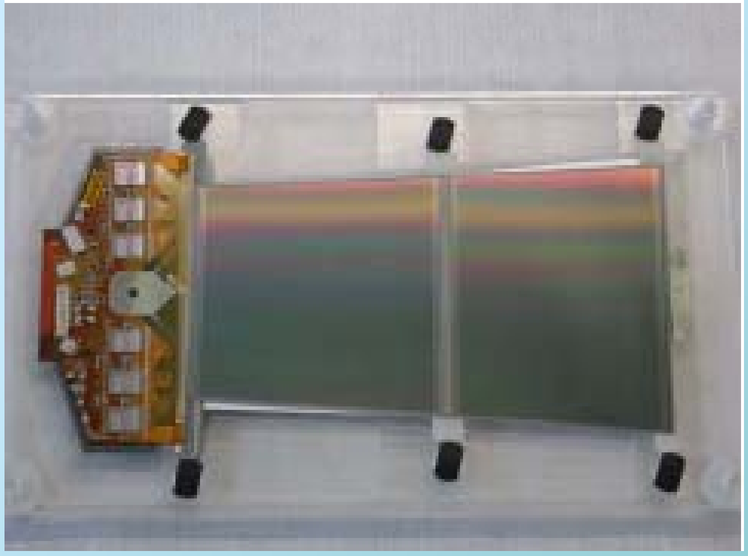
ATLAS Tracker Based on Barrel and Disc Supports



Effectively two styles of modules (with 2×6cm long strips)



Barrel Modules
(Hybrid bridge above sensors)

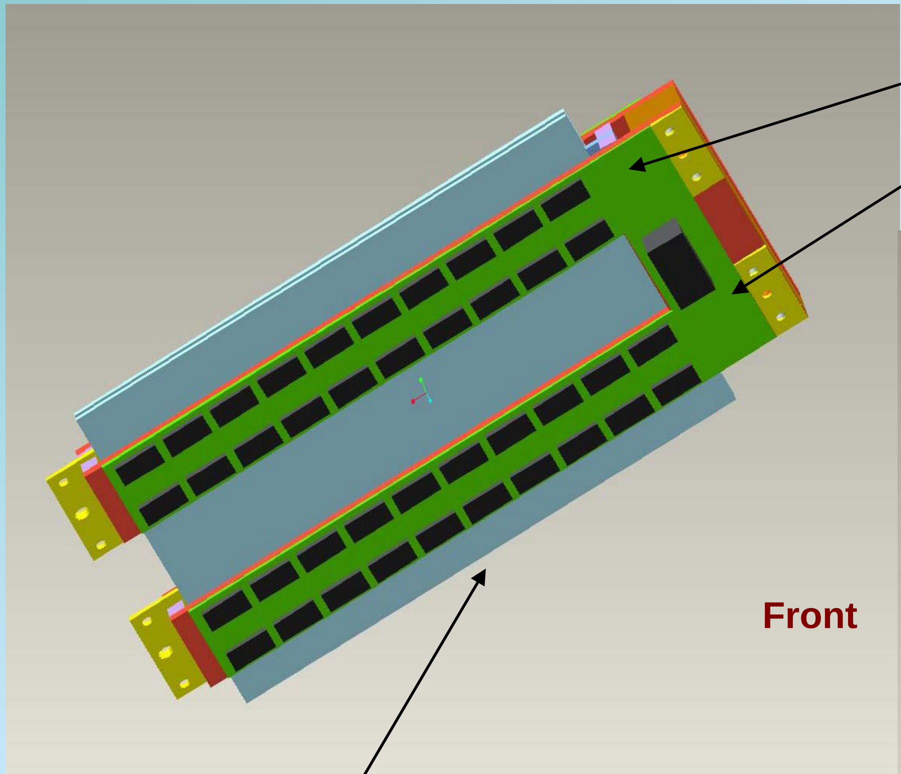


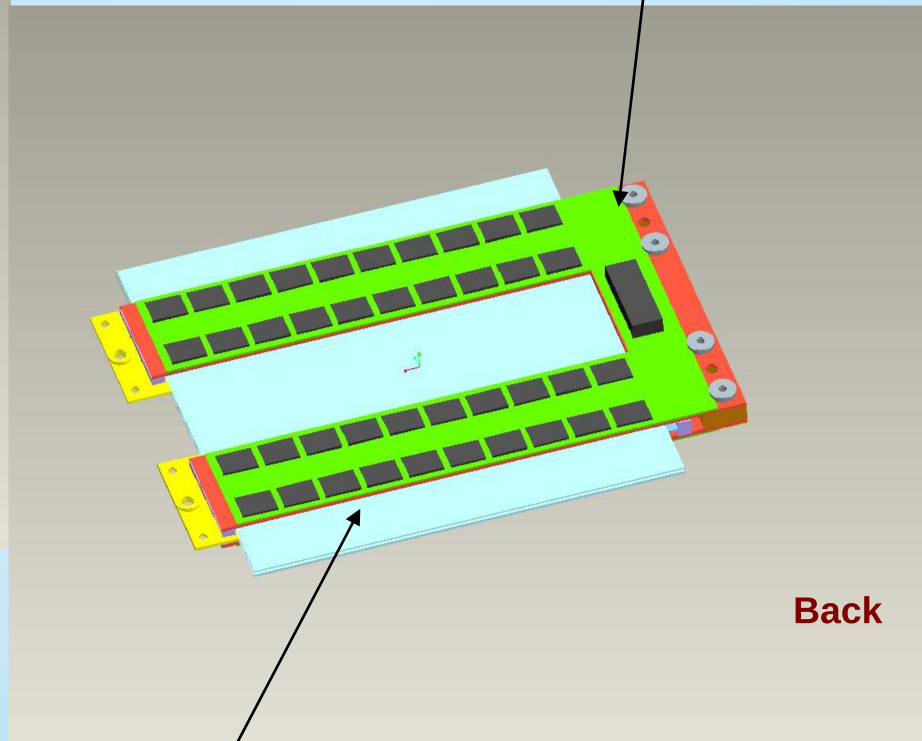
Forward Modules
(Hybrid at module end)

Super-LHC Double Sided Module

Sets of 10 FE Chips in 4 rows
Sets of 10 FE Chips in 4 rows

Module Controller Chip





2 single-sided 10cm square detectors mounted back-to-back around a high thermal conductivity base board

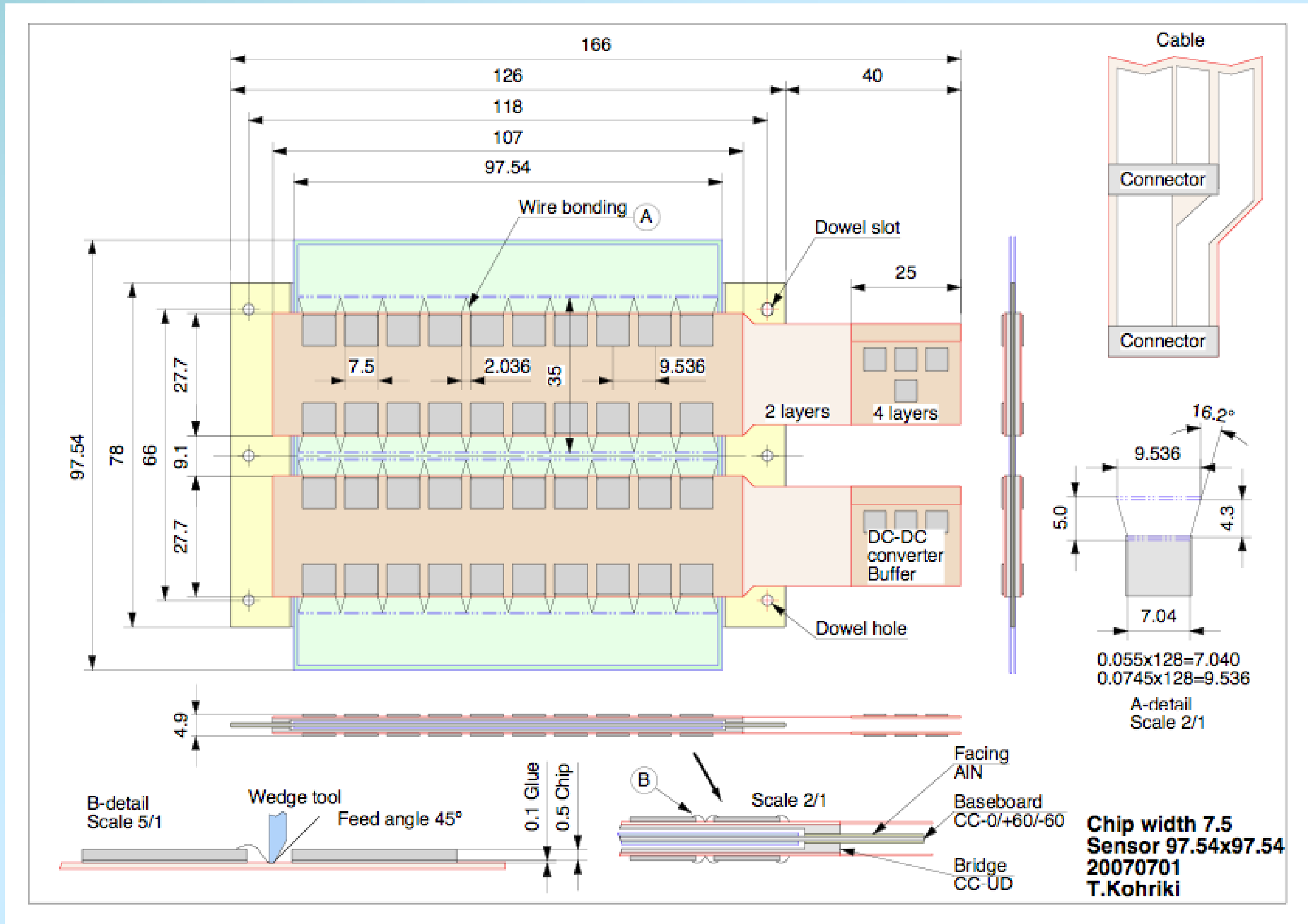
Each detector has 4 rows of 1280 2.4cm long striplets

The Multi-layer kapton circuit in green is the “hybrid” which busses signals to/from/between the microchips and provide the electrical services to the front end electronics

Wire bonds connect the electronics to the hybrid and provide the high density connections down from the front-end to the 4 pad rows on the detectors

Double-sided Hybrid Designs - KEK

Four hybrids/module,
four connectors/module square sensors (9.754 cm x 9.754 cm)



Y. Unno

SLHC module - Optimization

FEA thermal analyses using ANSYS

Need cooling from both ends (current ATLAS single-ended cooling)

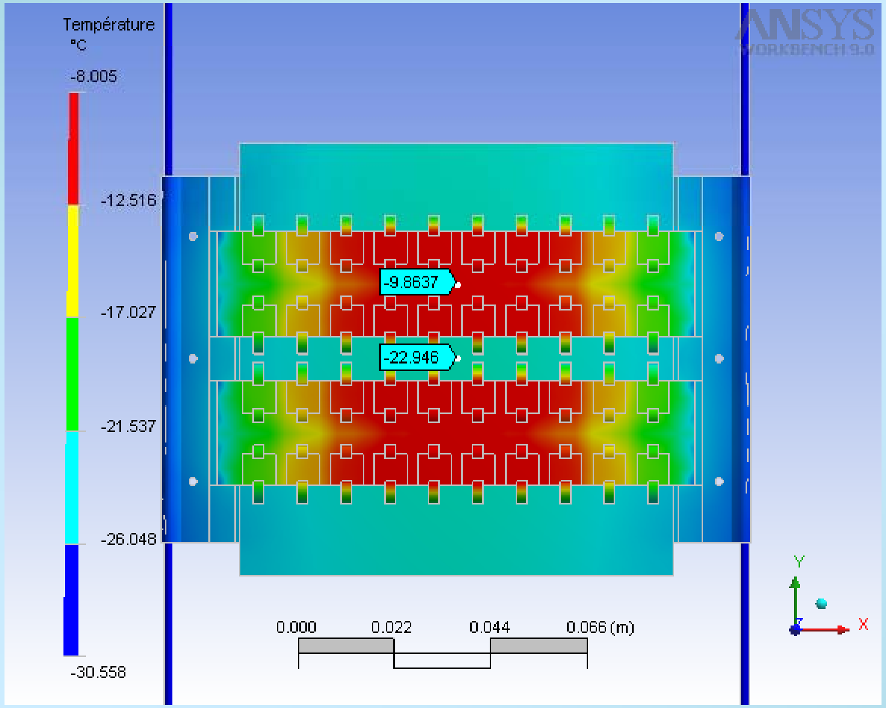
(2-dimensional calculation)

• 0.1mm thick thermal grease around cooling pipe (2W/m/K)

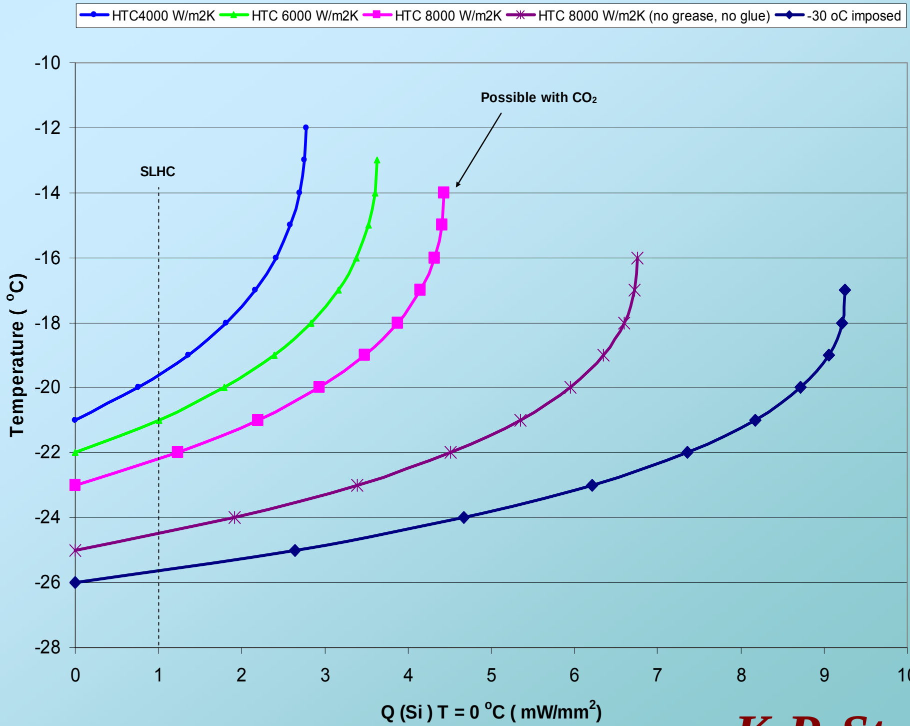
•Dead air between sensor and hybrid (0.024W/m/K)

Thermal distribution

2mW/ch, HTC 8000 W/m²K, -30 ºC, Q (Si) = 0

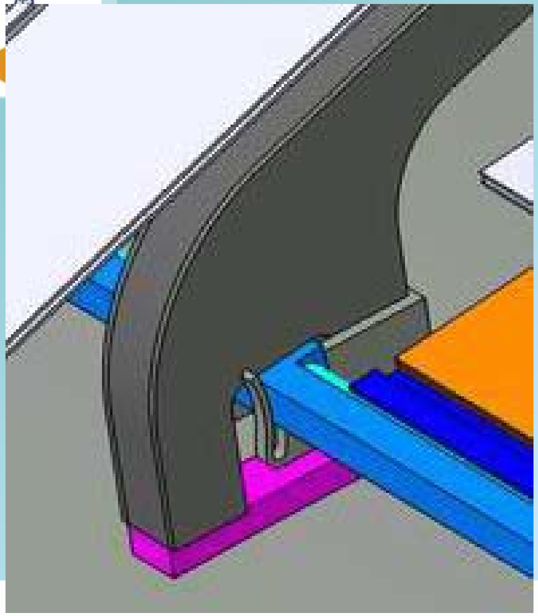


Runaway simulations for different cooling systems (cooling -30 ºC , 2mW/ch)



K-P. Streit

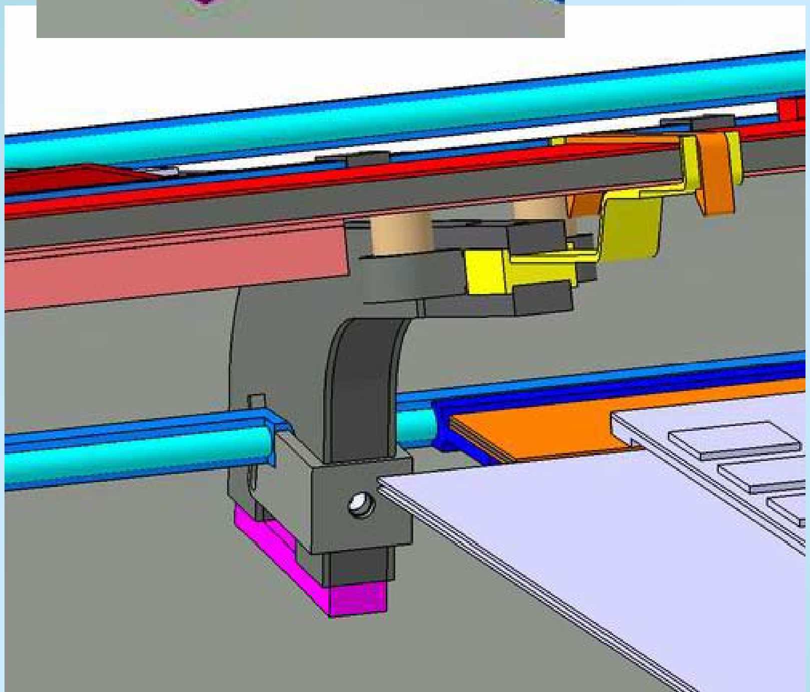
Individual Module - Direct Mounting

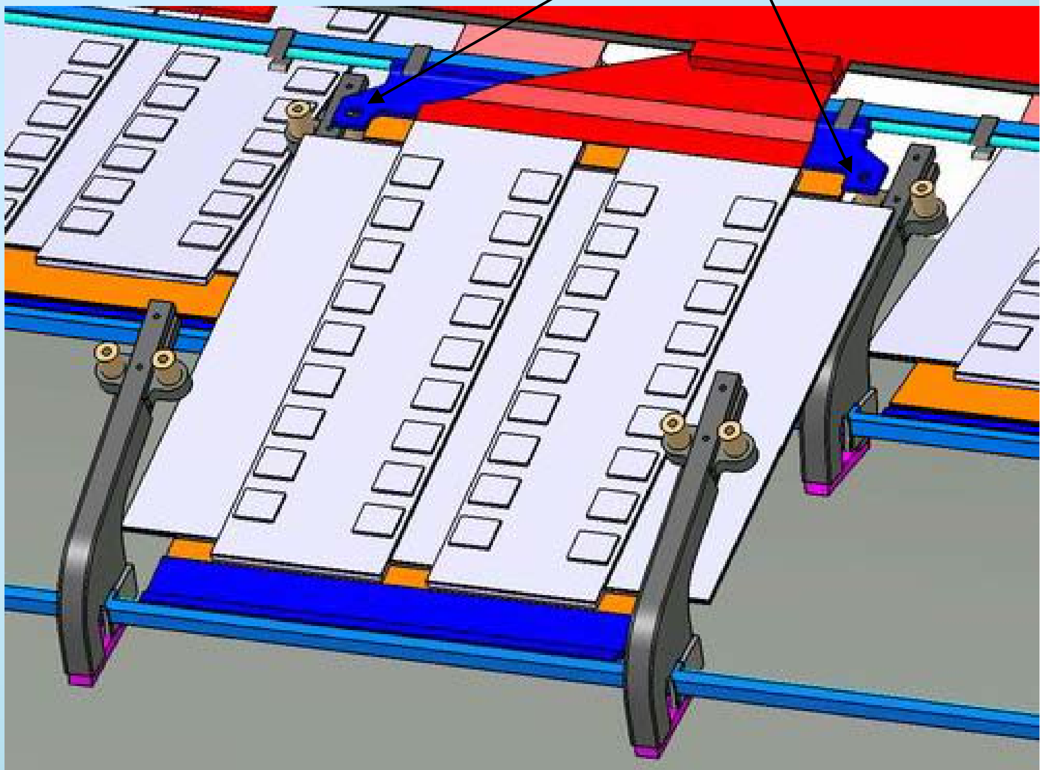


- 3rd “point” is defined by the pipe
- Cooling block is set with 2 fixation points on the pig-tail side
- 1 bracket is holding 2 neighboring modules
- The bottom left pipe is embedded in the brackets and must be assembled before the module.

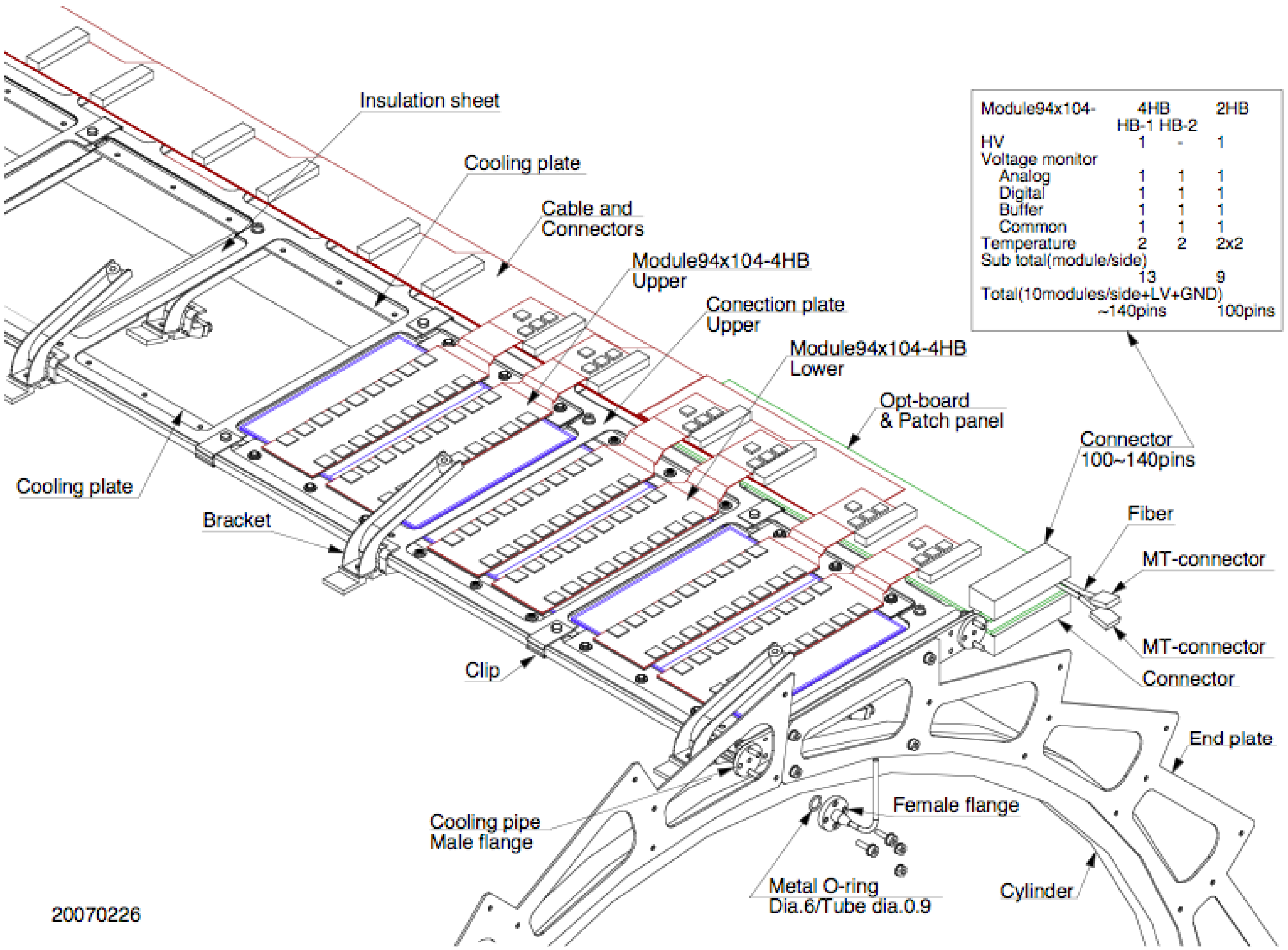
2 fixed mounting points

Y. Unno





Super-Module on Cylinder



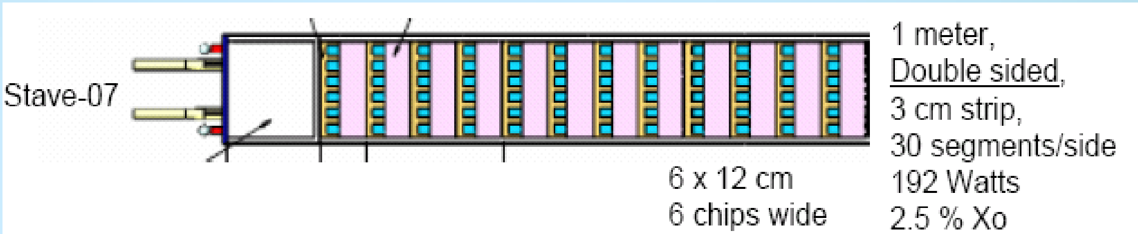
Module94x104-	4HB HB-1	4HB HB-2	2HB
HV	1	-	1
Voltage monitor			
Analog	1	1	1
Digital	1	1	1
Buffer	1	1	1
Common	1	1	1
Temperature	2	2	2x2
Sub total(module/side)	13		9
Total(10modules/side+LV+GND)	~140pins		100pins

Y. Unno

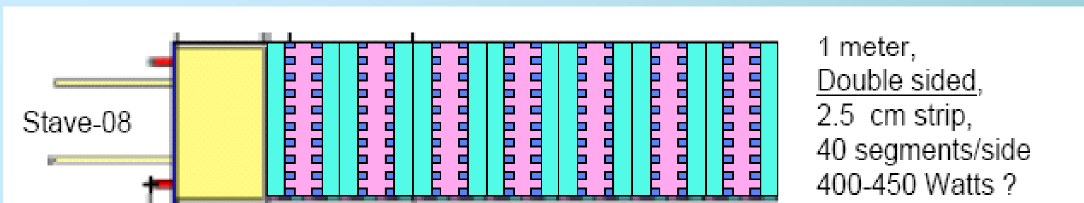
Stave Module Concept

- The "stave" concept has hybrids glued to sensors glued to cold support
- A first prototype version based on the CDF run-IIb concept but using ATLAS ASICs already exists

- A 6-chip wide version (Stave 2007) will use short p-in-n sensors and incorporate many of the final proposed, mechanical, thermal, electrical, serial powering and read-out features.

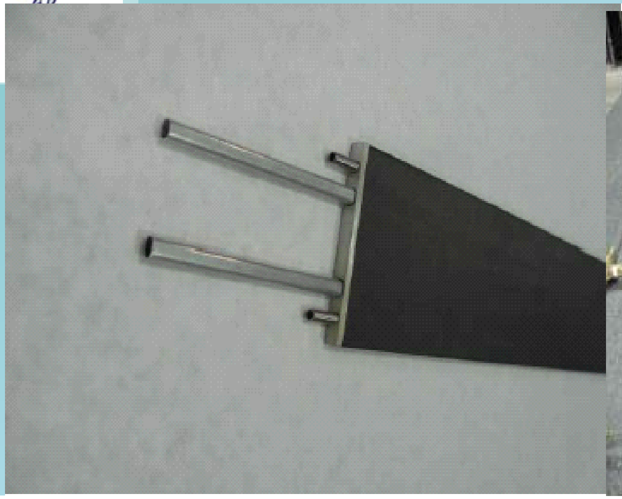


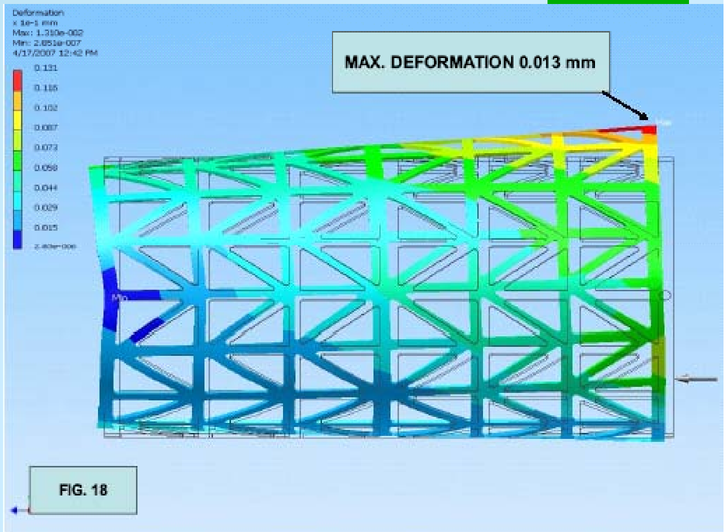
- Stave core fabrication, BeO hybrid design, cooling concepts and automated assembly nearing completion.
- 10 chip wide version under development

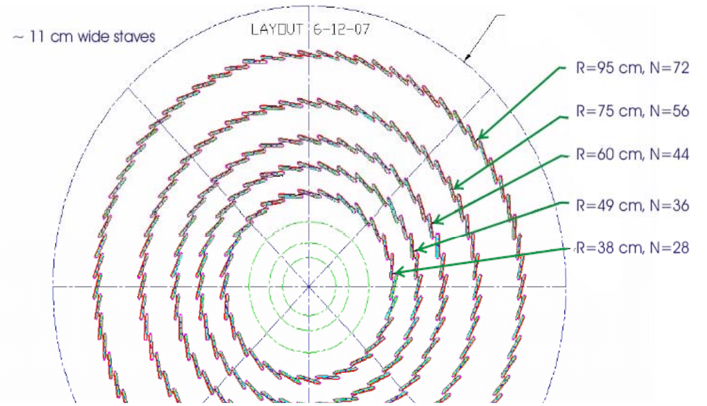


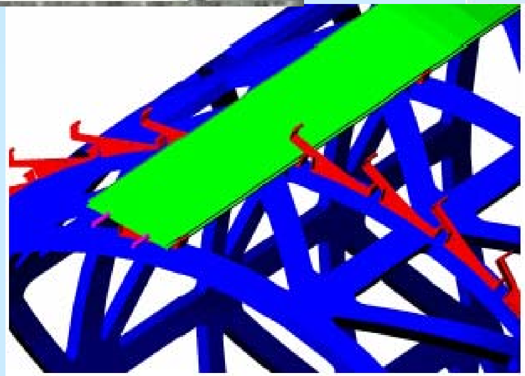
C. Haber

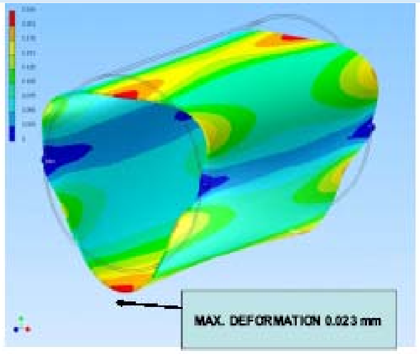
Stave R&D



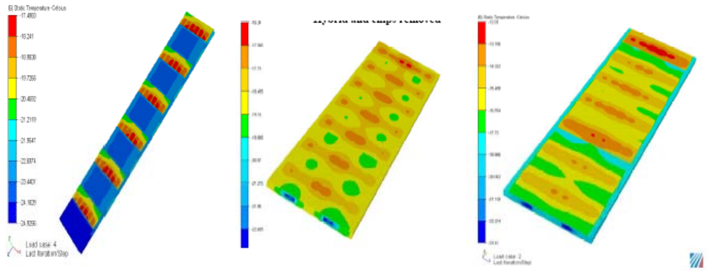




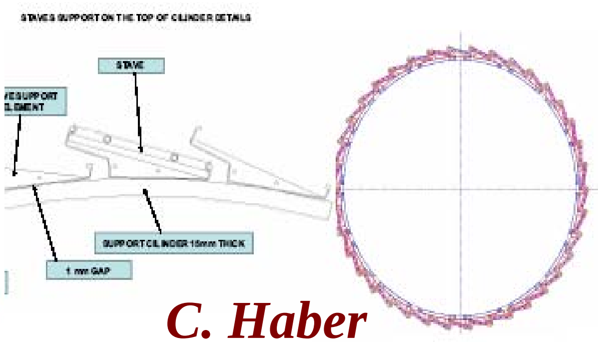


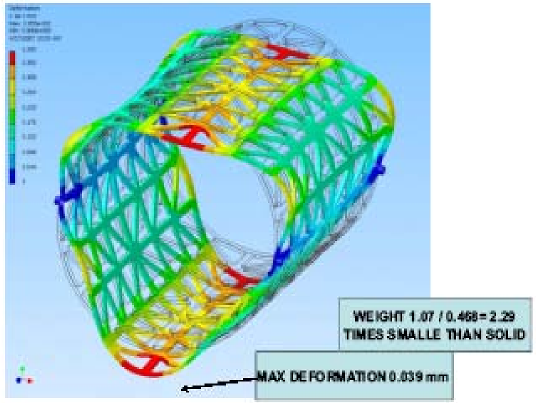


Single sided DS low cable TC DS high cable TC



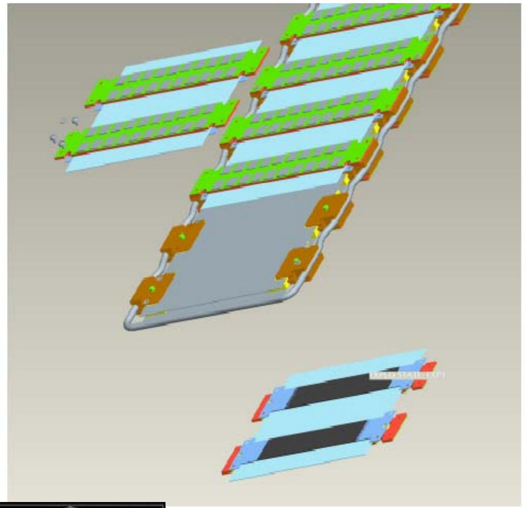
-17.5 C Chip/Silicon -23.5 C -12.6 C Chip/Silicon -13.6 C -16.7 C Chip/Silicon -17.4 C

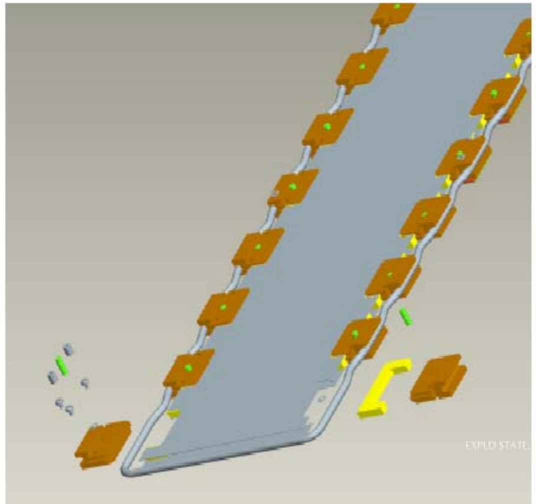




C. Haber

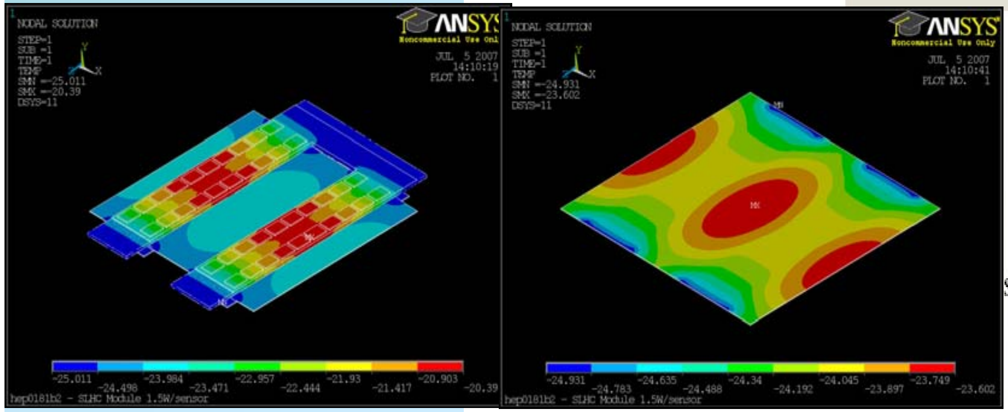
Single-sided Stave Concept



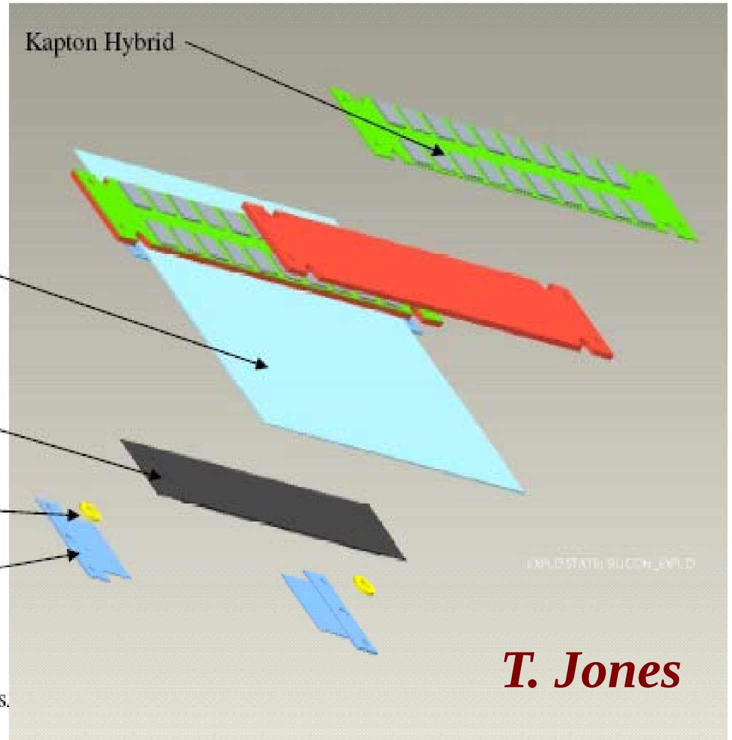


Bridged hybrid assemblies on cooled support

1.5W/Sensor
Max Chip temp: -20.4C
Max Silicon Temp: -23.6C
Temp Gradient over Si: 1.33C



Possible Demountable Module/Stave Concept (single-sided assembly step)



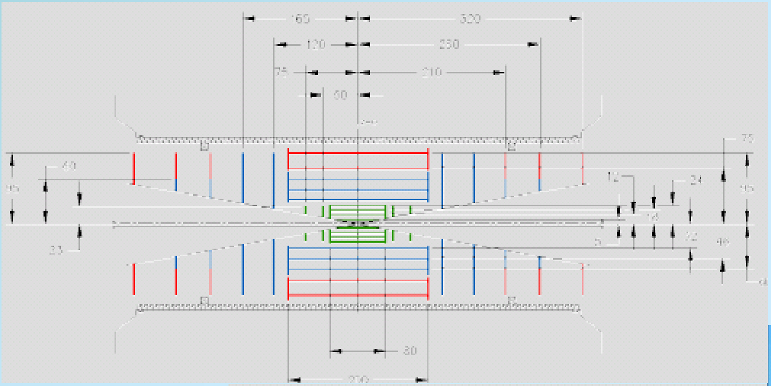
- Single sided silicon module.
- Alumina and TPG heat spreader, spliced as in ATLAS module.
- Integral precision location washers (holes and slots)
- Carbon Carbon hybrid base, with added non conductive spacers.

T. Jones

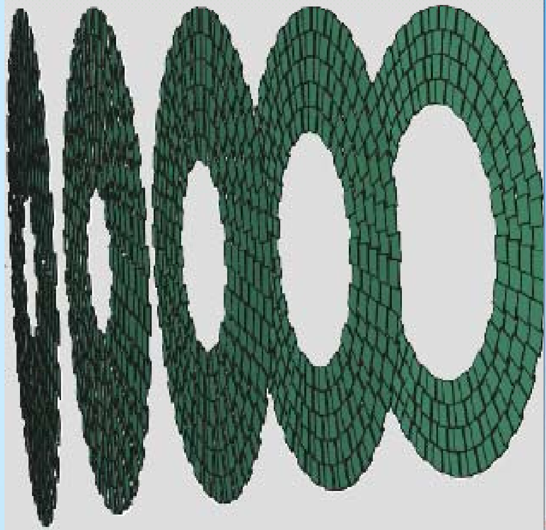
Forward Module Concepts

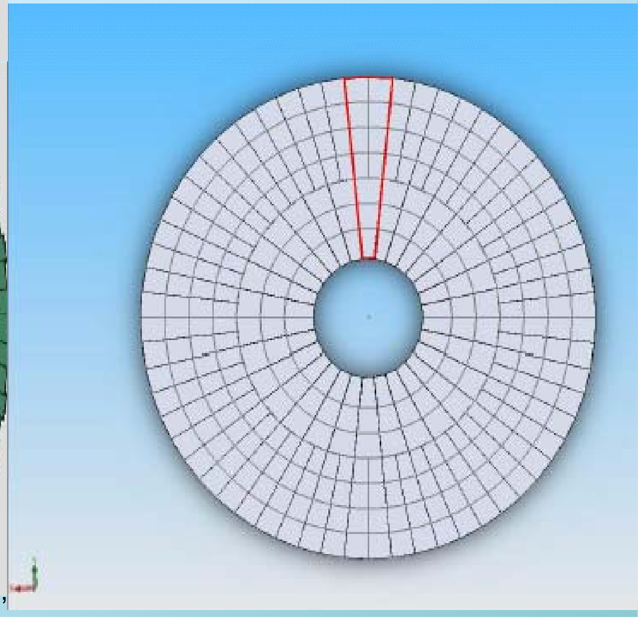
- As for current ATLAS SCT, Forward Modules likely to require several different wedge shaped sensors
- 5 discs on each side with outer radius 95cm and inner radii from 30cm

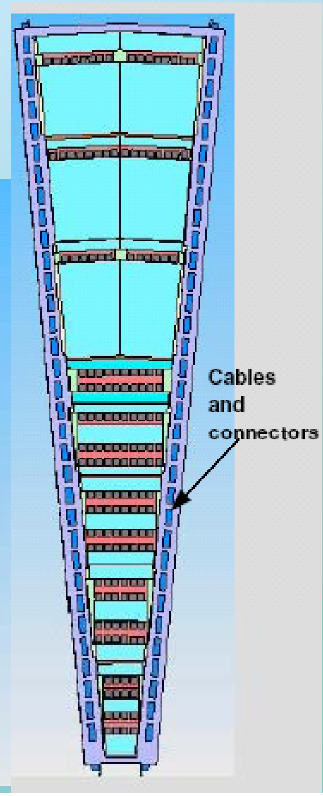
Can consider super-modules/staves or individual modules as now



Mean pitch about 80μm as at present





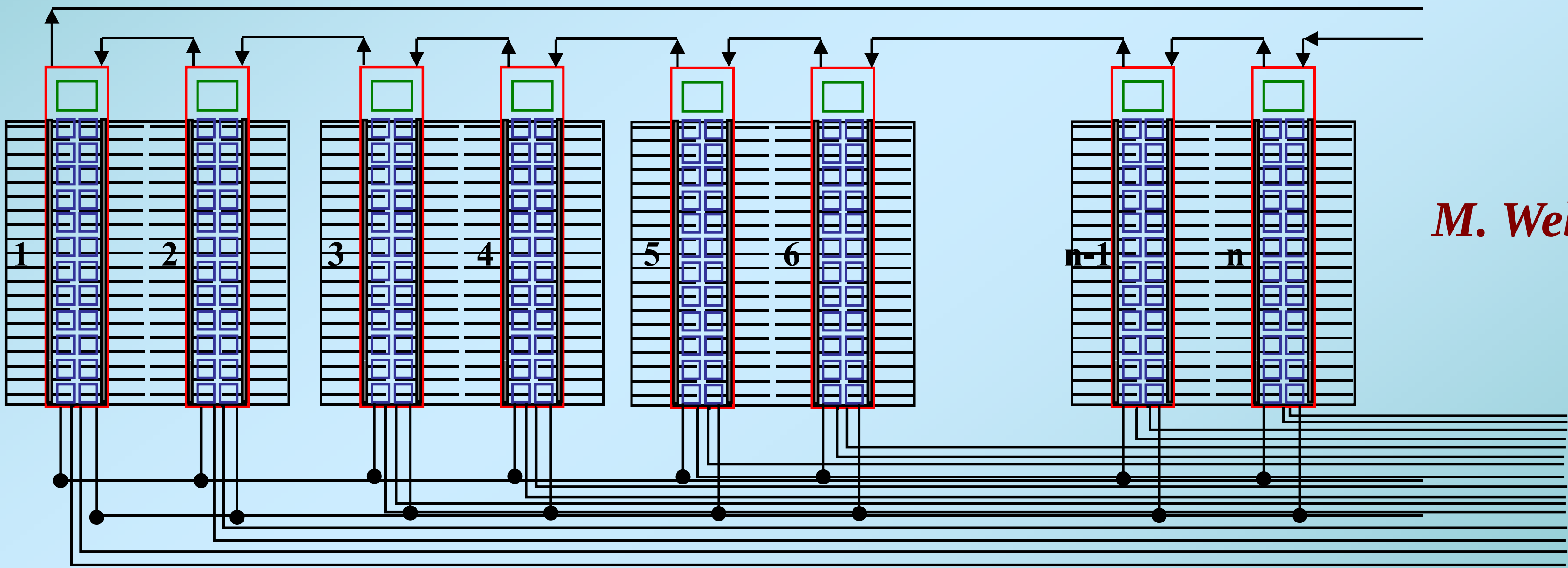


C. Lacasta

Powering Issues

V_{ABC-N} = 2.5 V; I_{Hybrid} = 2.4 A; 20 hybrids. **Low V + High I ➔ I^2R losses in cables**
(Want power transmission at High V + Low I)

Serial Powering: n=20; $I_H = I_{PS} = 2.4$ A; $V_{PS} = nV_{ABC-N} = 50$ V
Also saves factor ~8 in power cables/length over SCT
- Need detailed studies of failure modes and recovery



M. Weber

DC-DC Conversion : n=20; g =20; I_{PS}= n/g I_H = 2.4A; V_{PS}= gV_{ABC-N}= 50V
Parallel powering also saves factor ~8 in power cables as for Serial Powering
- Issues with switched capacitors (noise?) and need for custom design to get large g

(Independent powering with DC-DC costs too many cables)

Total Microstrip Power

	BIS	BOS	ECA	ECB	Total
Power [kW]	71.8	45.7	18.3	18.3	154.2
	47%	30%	12%	12%	

- Going to P_{chan} = 2mW → P_{total} = 120kW,
- Several contributions missing (SMC, Opto-converter, DCS, etc…)
- Best guess (strips) P_{total} = 150kW within ±40kW (2-3×SCT).
- Dominated by barrel (even if BOS shortened).
- Investigating cooling using C_3F_8 (again), C_2F_6 or CO_2
- Reuse of existing services could represent a major challenge

G. Viehhauser

Conclusions

- **Activities in many areas still just starting with emphasis on completion and commissioning of current ATLAS Detector**
- **Management structure includes Upgrade Steering Group, Upgrade Project Office and 8 working groups in the area of the tracker replacement alone**
- **Major recent tracker workshops include: Genoa (18/7/05 - 20/8/05), Liverpool (6/12/07- 8/12/07) and Valencia (10/12/07- 12/12/07)**
- **Some impressive progress, but still plenty to do and not so much time to do it …**

  ATLAS Inner Detector Technical Design Report now 10 years old
  http://atlas.web.cern.ch/Atlas/GROUPS/INNER_DETECTOR/TDR/tdr.html
- **For more material of past internal meetings see ATLAS *indico* pages**
  http://indico.cern.ch/categoryDisplay.py?categId=350