Thin planar pixel detectors for highest radiation levels

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Institutes: CERN, Univ. Dortmund, Univ. Freiburg, Univ. Hamburg,

J. Stefan Inst. Ljubljana, MPI Munich

Embedded within an ATLAS-Proposal for 3D integration

Study of charge collection before and after radiation on pixelated readout nodes with different geometries and different sensor thicknesses – Check out the limits of planar detectors

Status and plans

11th RD50 Workshop
CERN
Nov. 2007

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The Challenge

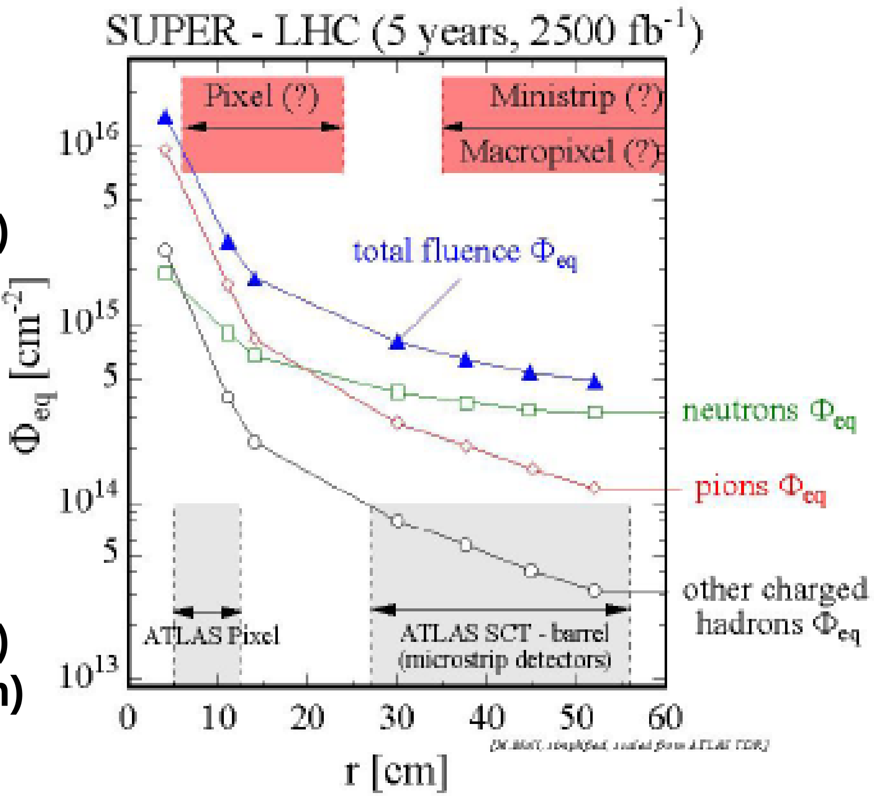
Expected conditions at LHC and sLHC

LHC:

- **Start 2008**
- **L = 10^{34}cm^{-2}s^{-1}**
- **Integrated Luminosity: 500 fb^{-1} (10y)**
- **Fluence: 3×10^{15}cm^{-2} (1 MeV n, 4cm)**
- **Multiplicity: 0.5-1 k tracks/event**

sLHC:

- **Start 2016**
- **L = 10^{35}cm^{-2}s^{-1}**
- **Integrated Luminosity: 2500 fb^{-1} (5y)**
- **Fluence: 1.6×10^{16}cm^{-2} (1 MeV n, 4cm)**
- **Multiplicity: 5-10 k tracks/event**



New detector concepts needed

Motivation for Thin Detectors

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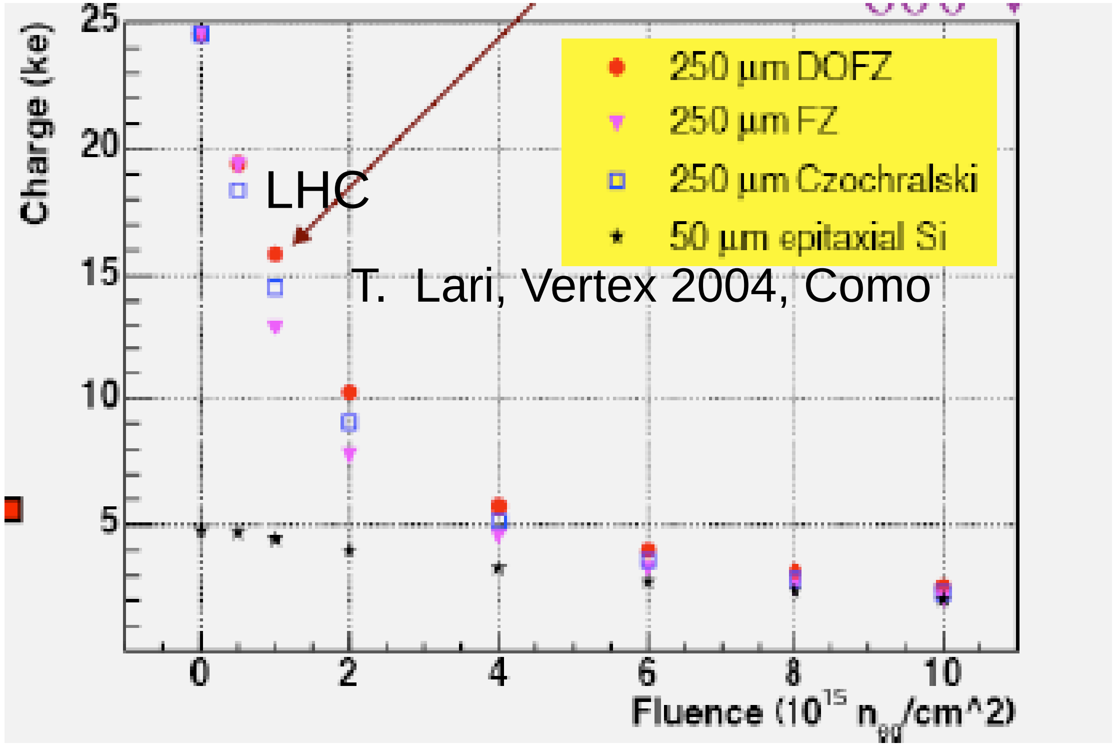
After 10^{16} n/cm^2:

- V_{dep} > 4000V (250 μm) -> operate partially depleted.
- Large leakage currents.
- Charge loss due to trapping (mean free path ~ 25 μm).
- $l_e > l_h$ (need n-in-n or n-in-p) to collect electrons.



No advantage of thick detectors ->thin detectors: low V_{dep}, I_{leak} (and X_0)
However: small signal size is a challenge for the readout electronics

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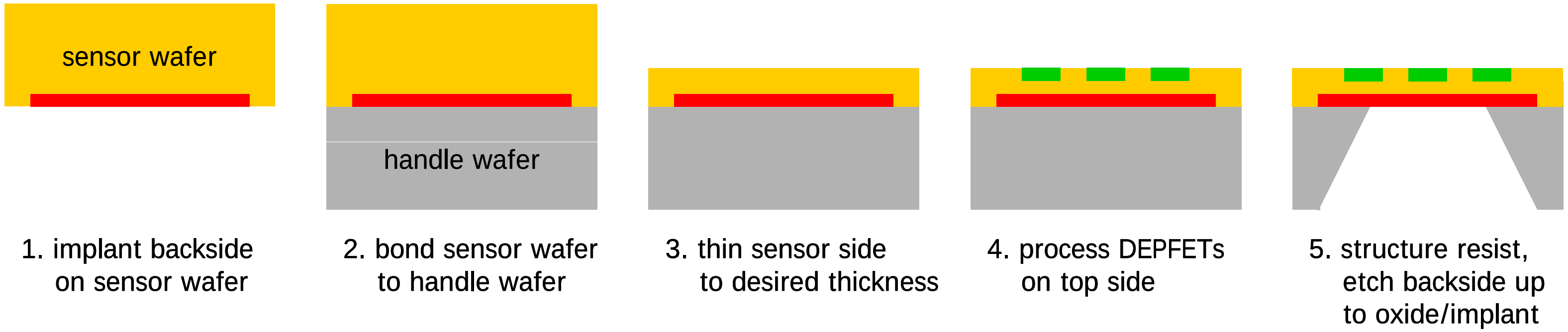
Thinning Technology

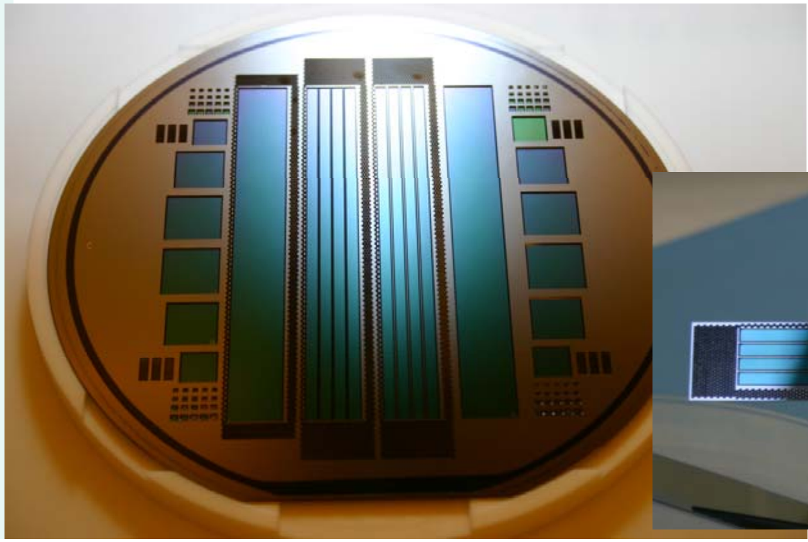


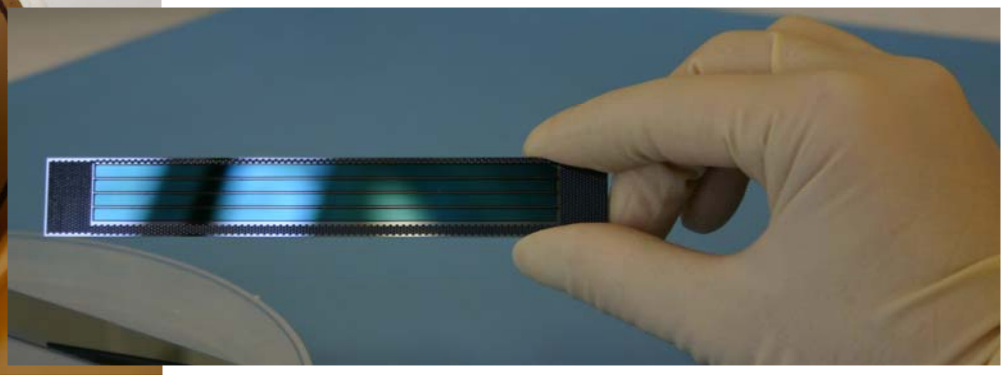
- Sensor wafer: high resistivity d=150mm FZ wafer.
- Bonded on low resistivity “handle” wafer”.
- (almost) any thickness possible

Thin (50 µm) silicon successfully produced at MPI.

- MOS structures
- diodes

-No deterioration of detector properties, keep I_{leak} <100pA/cm^2





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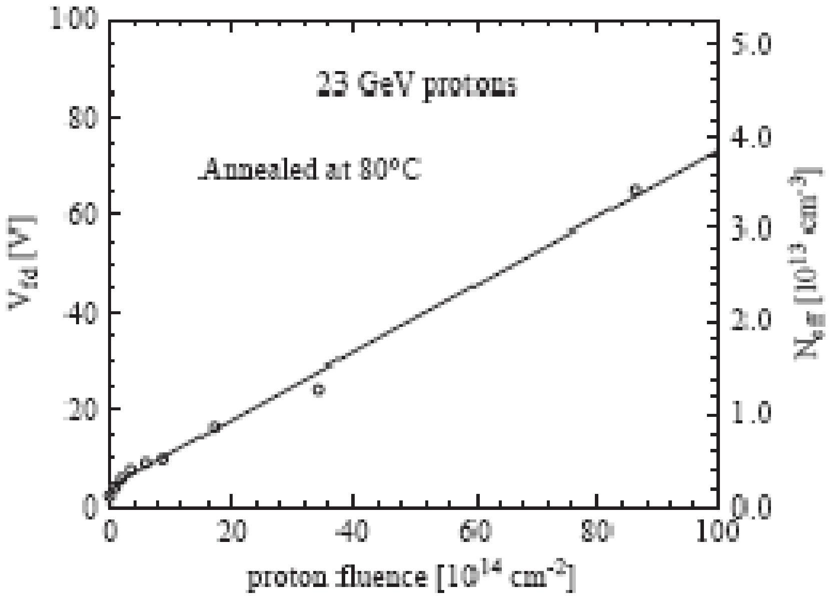
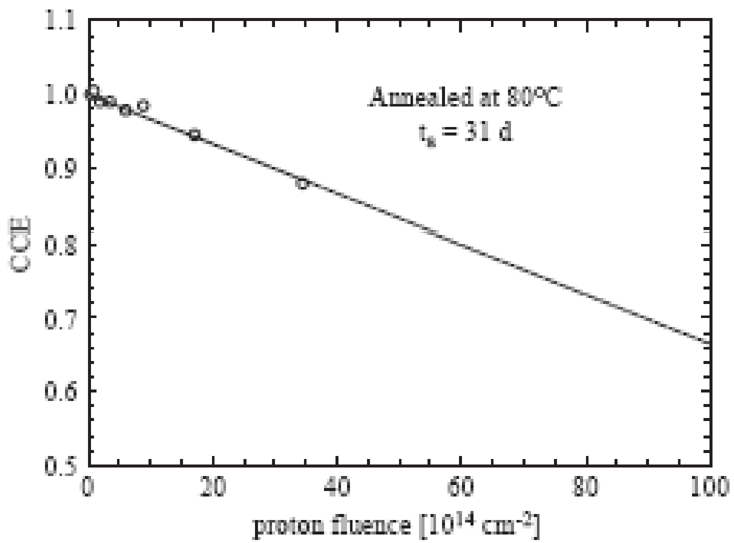
Measurements (V_{dep}, CCE)





Fretwurst et al. NIM A 552 (2005):
After short term annealing:

V_{dep} < 100V at 10^{16} 1/cm^2.

However, detectors need to be kept cold (reverse annealing!).

Leakage currents:
α(80°C, 8min) = 2.4 x 10^{-17} A/cm.

CCE ~ 66% @ 10^{16} p/cm^2 (extrapolated).

Similar to results from epi-material (G.Kramberger):

3200e (62% average),
2400e (60% most prob).

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Electric field and drift velocity

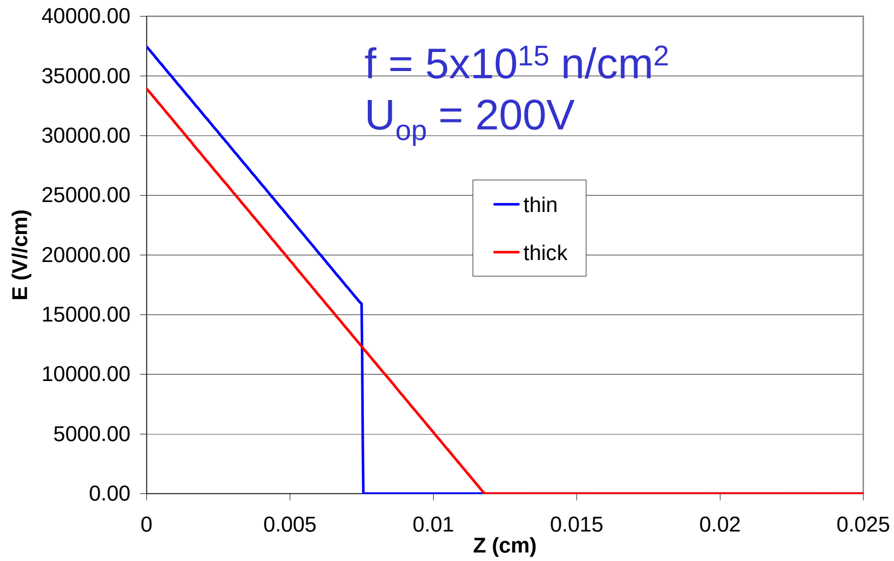
Is there an advantage of thin detectors compared to thick detectors operated partially depleted?

At the same voltage thin (=over depleted) detectors have a higher electric field than thick (= partially depleted) detectors

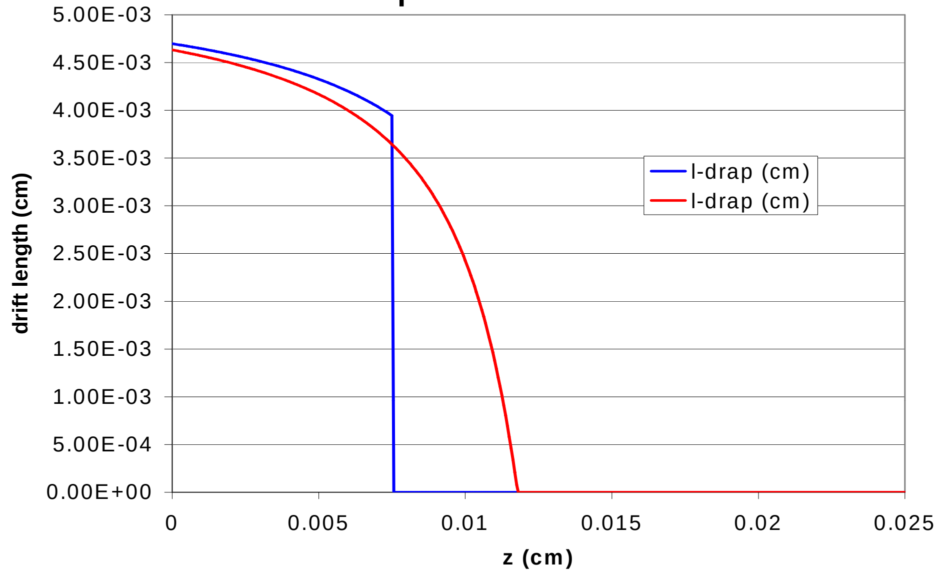
⇒Higher drift velocity
⇒Better CCE

(however $v_{drift} \sim v_{sat}$)

In addition the depleted volume of thick detectors is larger
⇒Larger leakage currents (shot noise, heat)
⇒Additional volume does not give a signal ($l_{drift}<z_{dep}$)



Simplified!



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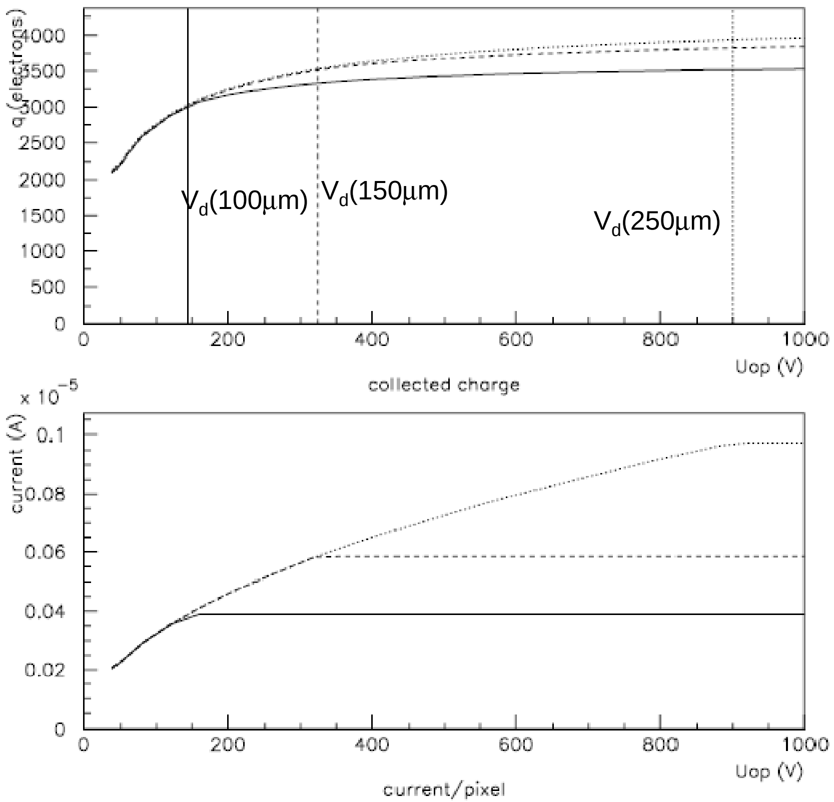
Charge Collection

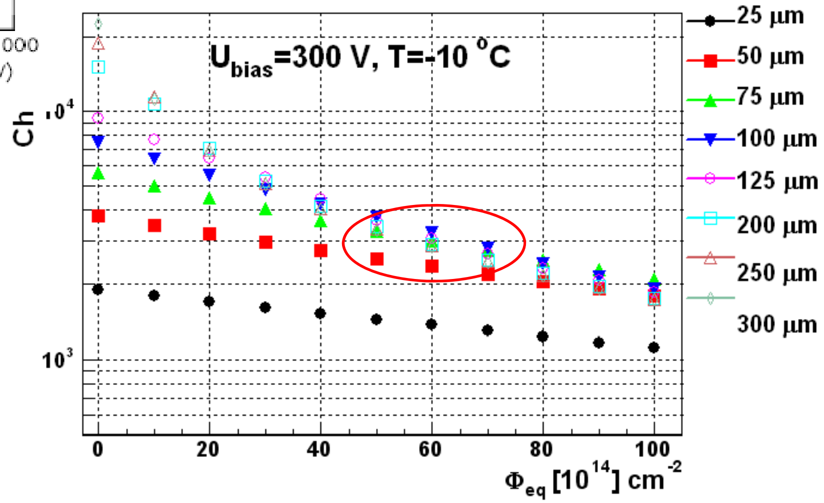


Irradiation to $5x10^{15}$ n/cm^2

Thicknesses: 100 µm V_d=150V
150 µm V_d=325V
250 µm V_d=900V

At 350 V the 100 µm detector should collect 95% of the charge of the thicker detectors but at much less leakage current!

The example above assumes a planar diode.
For segmented detectors CCE is affected by the weighting field.
Signal (thin) > signal (thick) possible!
(G. Kramberger)



QV plots (Simulations) – different detector thicknesses
G. Kramberger (Schloss Ringberg 2007)

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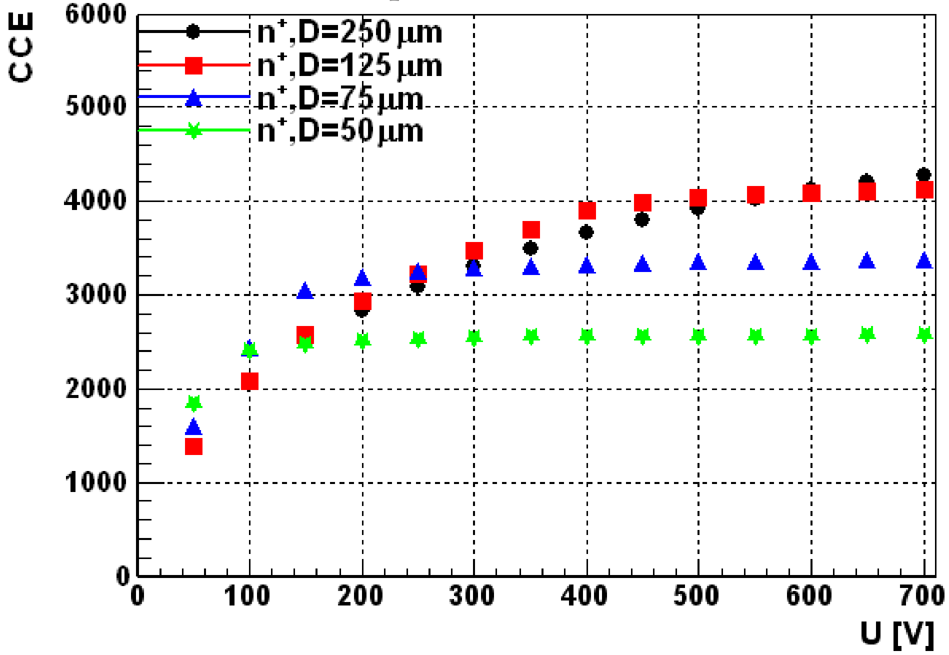
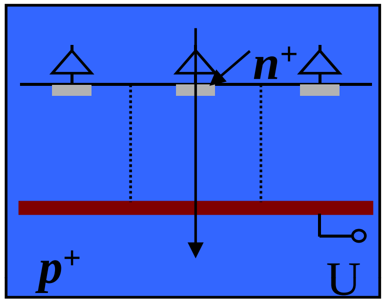
$\Phi_{eq}=5\cdot10^{15}\ cm^{-2}$





- Similar Q-V characteristics up to full depletion!
- Thinner sensors are beneficial at lower voltages – the more voltage you can apply the more beneficial are thicker detectors

Trapping induced charge sharing (G. Kramberger)

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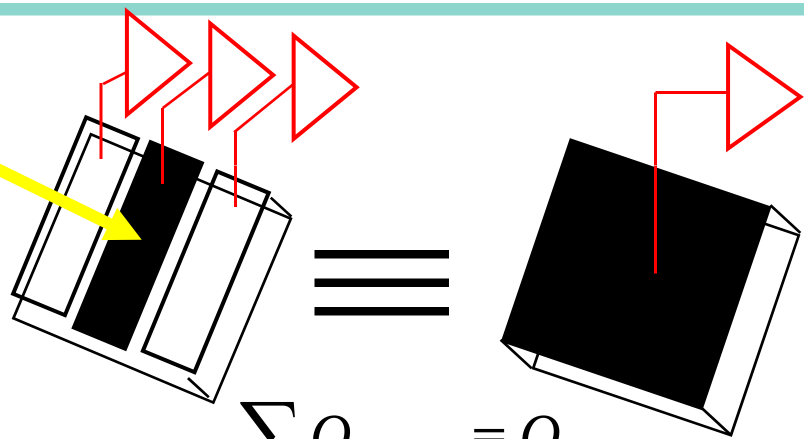
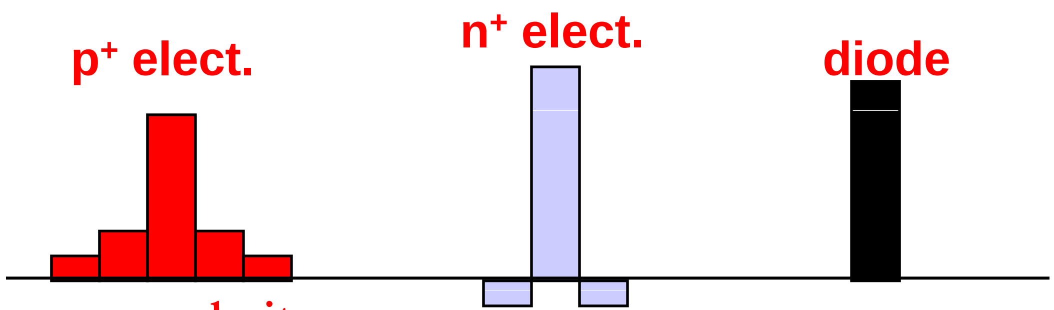
electrode hit in the center by ionizing particle



$$\sum_{\substack{all\,electrodes \\ (pitch-implantwidth)\to 0}} Q_i \equiv Q_{diode}$$



same polarity

$Q_{hit} < Q_{diode}$

↓

wider clusters

opposite polarity

$Q_{hit} > Q_{diode}$

↓

larger signals

Need to study signal sharing and resolution in pixel detectors

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Status: Wafer Procurement

SOI wafer (Tracit/Soitec): 6” (backside porcessed, bonded, thinned and delivered)

thickness	type	Resistivity (Ohm.cm)	#
75	p	>2000	11
150	p	>2000	12
75	n	340	11

Epi-wafer (ITME): 4” ordered, delivery in about 4 weeks

thickness	type	Resistivity (Ohm.cm)	#
50	p	150	9
75	P	300	9
150	P	1200	9

Bulk: p-type

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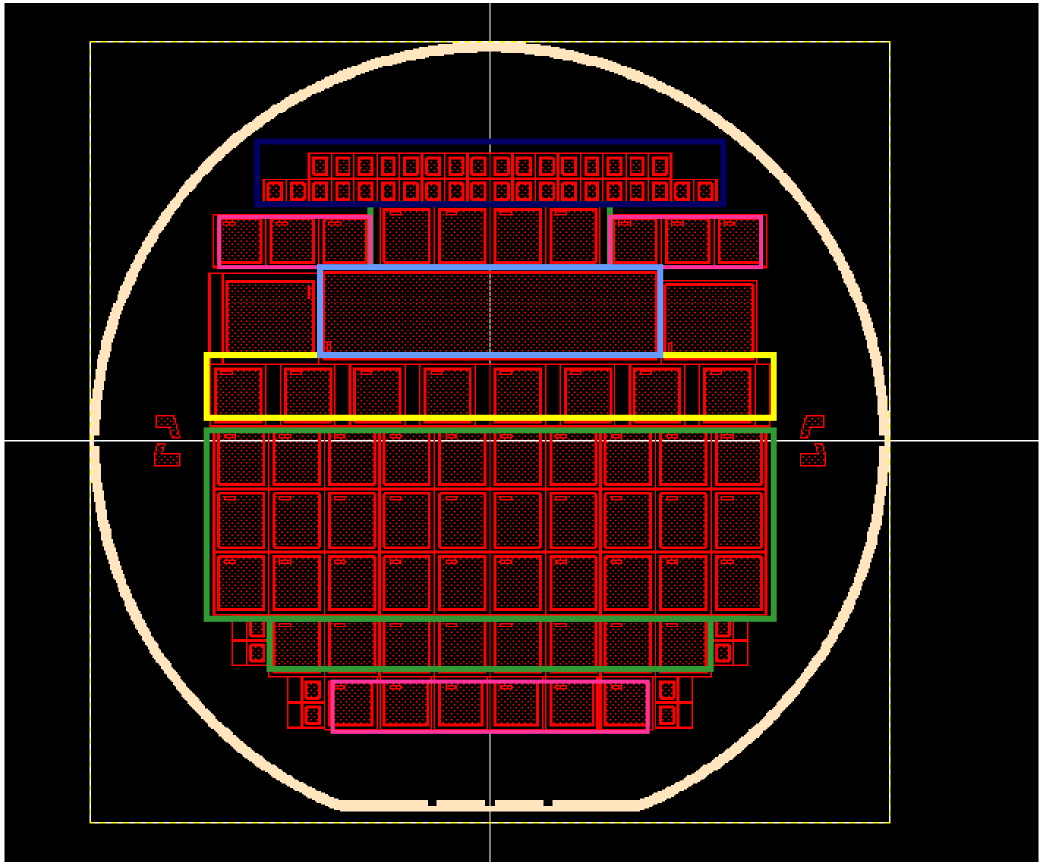
Status: Wafer Layout (6” SOI)



42 cells 10.5 x 11.9 mm^2

10 different micro-strips versions + test-structures

12 diode cells

10.0 x 10.0 mm^2

8 pixel cells – ATLAS geometry to be read out by a single FE chip – designed for SLID interconnection

ATLAS module, to be connected to the FE with bump-bonding

Pixel cells to be read out by a FE chip by INTERON (Norway)

Pixels follow ATLAS layout:, 160 x 18 pixel 50 x 400 mm2 for FEI3 chip
10 x 10 pixel arrays with smaller pith (50x200, 100, 50) for special simple readout chip
Ministrips to be read by ALTAS SCT128 chip
Diodes

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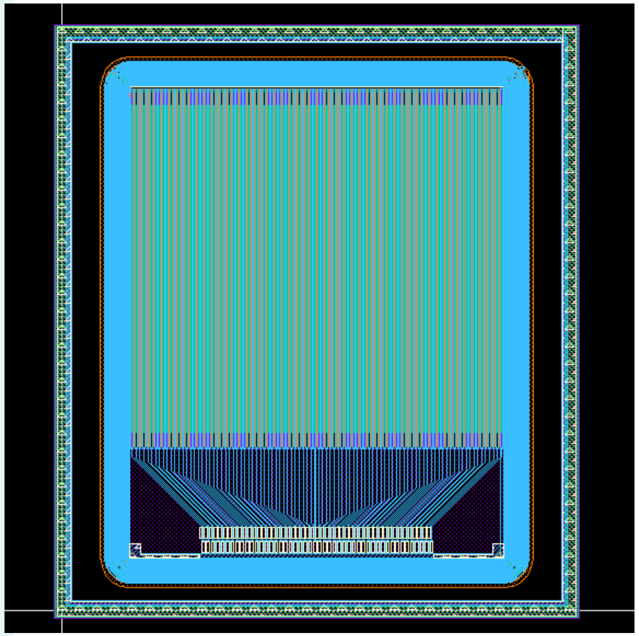
Layout of Microstrips

SOI & EPI: 4 copies/wafer

Strip pitch (µm)	n+ implantation width (µm)	p-spray moderation width (µm)
50	30	10
50	30	No
80	30	10
80	30	no

SOI: 3 copies/wafer

Strip pitch (µm)	n+ implantation width (µm)	p-spray moderation width (µm)
50	24	10
50	30	6
50	36	6
80	20	No
80	20	24
80	30	24

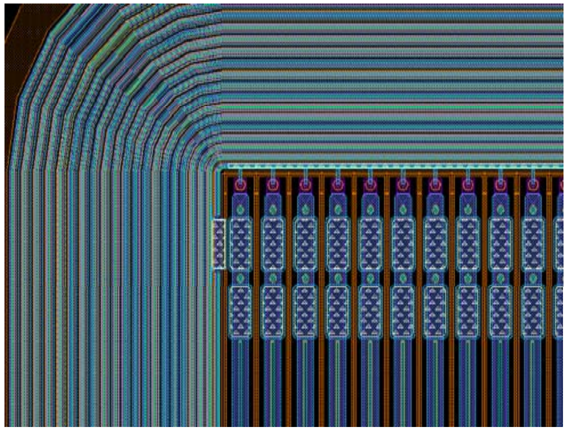


DC coupled

Punch through biasing for testing

96 strips (80 µm pitch)

L=7.5 mm



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Layout of Test Diodes

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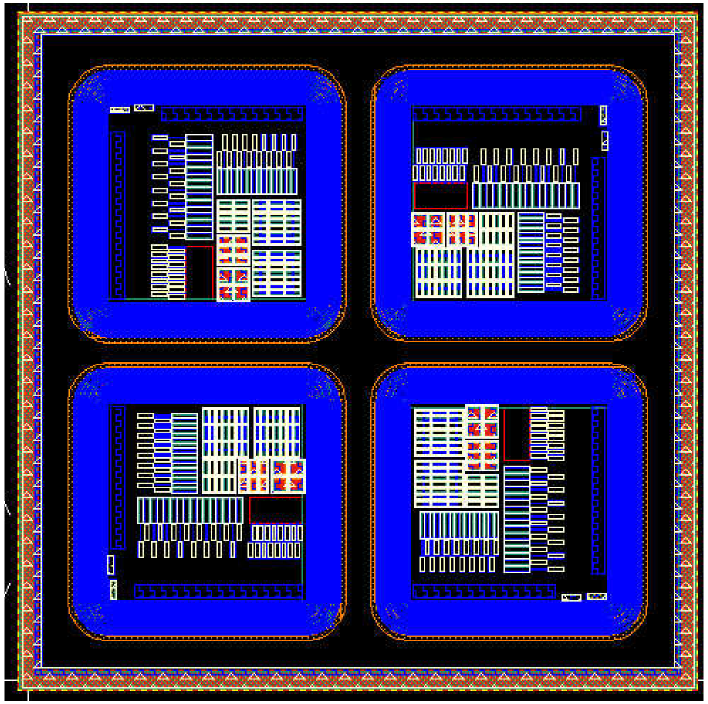
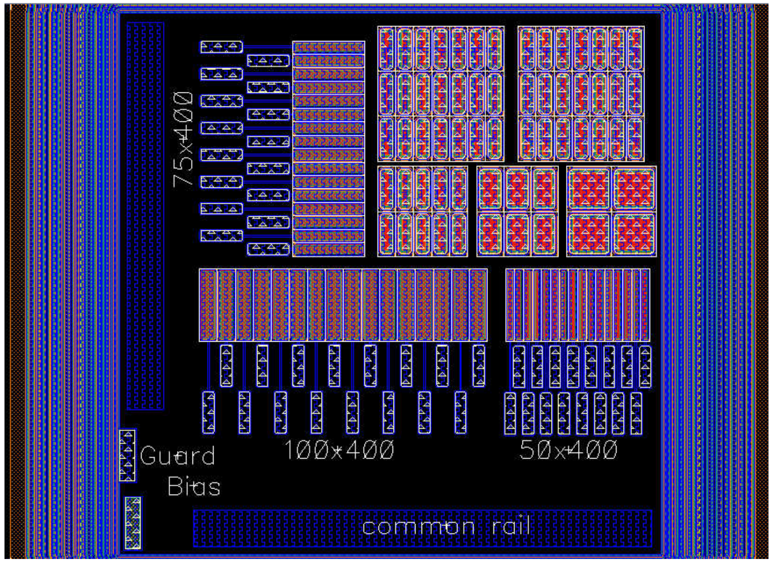
16 Frames for diodes and simple structures

4 identical frames for "Ljubljana style" structures (with for variants each)

12 frames for "Hamburg style" diodes (propose 4 identical copies/wafer)





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Epi wafers

Contains a subset of the test structures (only 4”):

- diodes
- mini-strips (most promising variations only)
- pixel test structures (Gregor)
- no ATLAS pixel and 3D-integration structures

Layouts transfered to CIS

Parameters need to be defined (CIS specific)

Order needs to be placed

How many?

How many variants?

Deadline for decisions: Delivery of epi-wafers due end of November!

Processing (SOI)

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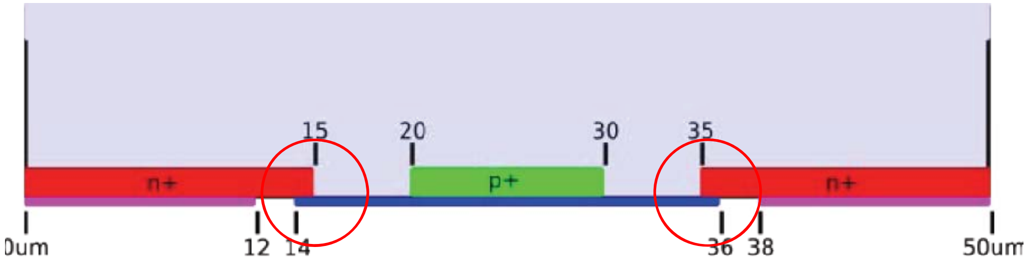
Limitation: 12 Wafers

Nr	Type	thickness	P-spray	Planned use
1	N	75	ATLAS (high)	Irrad
2	N	75	ATLAS (high)	SLID/irrad
3	N	75	ATLAS (high)	SLID/irrad
4	N	75	ATLAS (high)	SLID/irrad
5	P	75	Low	Irrad
6	P	75	Low	SLID/irrad
7	P	75	High	Irrad
8	P	75	High	SLID/irrad
9	P	150	Low	SLID/irrad
10	P	150	Low	Bump/irrad
11	P	150	High	Irrad
12	p	150	High	Bump/irrad

Irrad: can be used immediately for irradiations
SLID/irrad: first processed for inteconnection, irradiation later
Bump/irrad: first processed for bump bonding, irradiation later

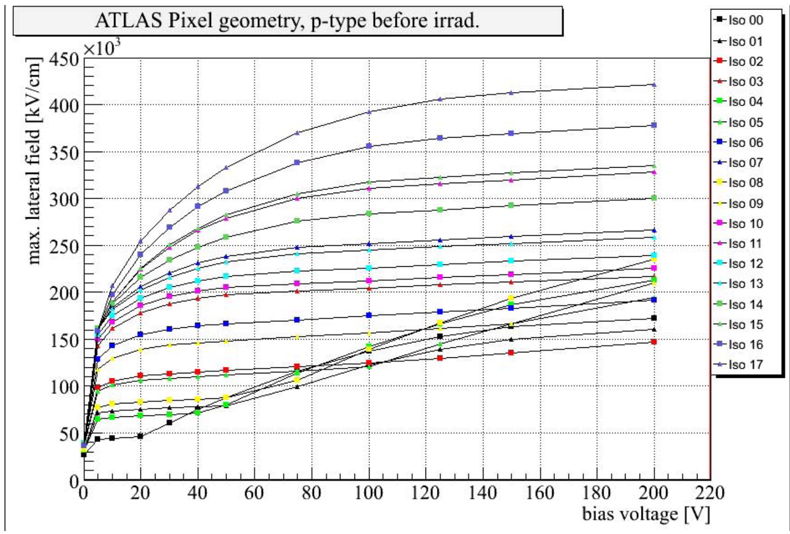
Simulations

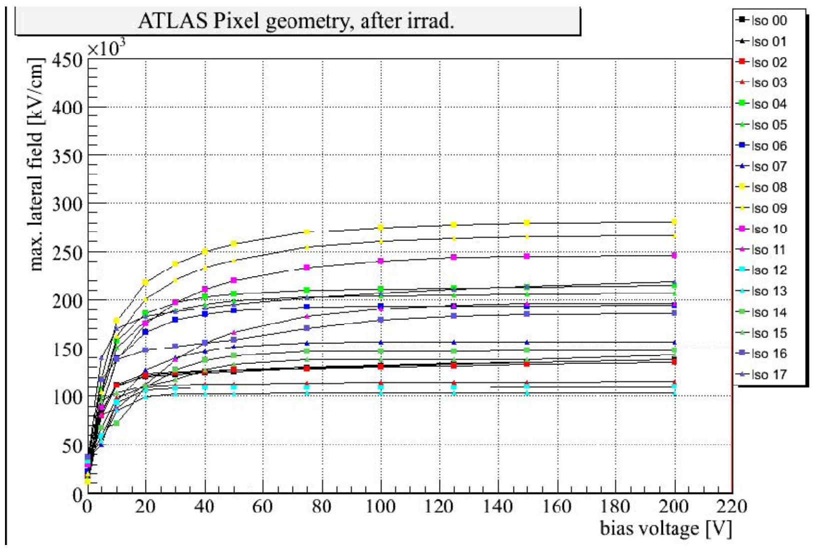
Simulation of electrical fields due to p-spray (M. Beimforte)



high fields at edges of n-implant
Depending on p-spray dose

p-substrate most critical before irradiation! -> chose two different p-spray doses





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Irradiation Program

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Boundary conditions:

P-type

Per thickness and p-spray variant: : 4 identical copies/structure immediatly

4 identical copies/structure later

N-type

Per thickness: 4 identical copies/structure immediatly

12 identical copies/structure immediately

Proposal: first step: unirradiated (reference) + 3 proton irradiations

second step: neutrons, gammas(?), additional proton doses

protons: 1E15, 3E15, 1E16 ? (or lower for 150 μm?)

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Schedule

- Begin of pre processing July 07 (definition of chips active areas for backside implantation)
- Waferbonding: done
- Final design: in two weeks
- Production start: December 07
- First samples: Spring of 2008
- All samples: 2^{nd} half 2008

- Schedule irradiations in 2008!

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Summary

Thin detectors

- **Keep V_{dep} low.**
- **Keep I_{leak} low (power).**
- **Reduce X_0** (if this is not an issue: backside etching not necessary, simpler fabrication)

- **Results on radiation hardness and CCE encouraging.**
- **Large scale industrial production possible.**
- **Thickness can be adapted to radius (fluence) -> parameter!**

R&D topics:
- **Make real pixel detectors.**
- **Irradiations, measurement of CCE.**
- **Optimize thickness**
- **Charge sharing.**
- **Optimize production process**

Status
- **SOI wafers delivered**
- **EPI wafers ordered**
- **Design of teststructures almost finalized**
- **SOI wafers to be processed soon (MPI HLL)**
- **EPI processing at CIS to follow**