40 MHz analogue readout for strip detectors

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- Motivation
- The Beetle chip
- The TELL1
- Stand-alone system
- Software issues
- Test beam experience
- Outlook

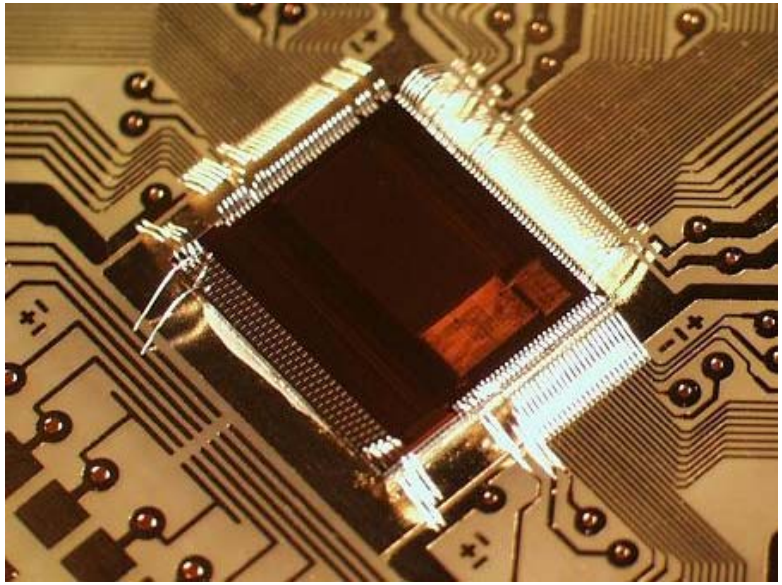
University of Glasgow

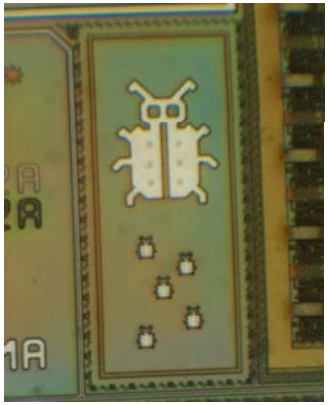
SLHC prototyping with LHC components

- Many types of R&D strip detectors on the market.
  - FZ, MCz, n-in-p, n-in-n, p-in-in, 3D silicon …
- Aimed for (S)LHC experiment upgrades and similar applications.
- Need to investigate their performance within a realistic system
- Lots of 'left-overs' from LHC detector constructions
  - Readout chips
  - Hybrids
  - DAQ components
  - Software

The Beetle chip

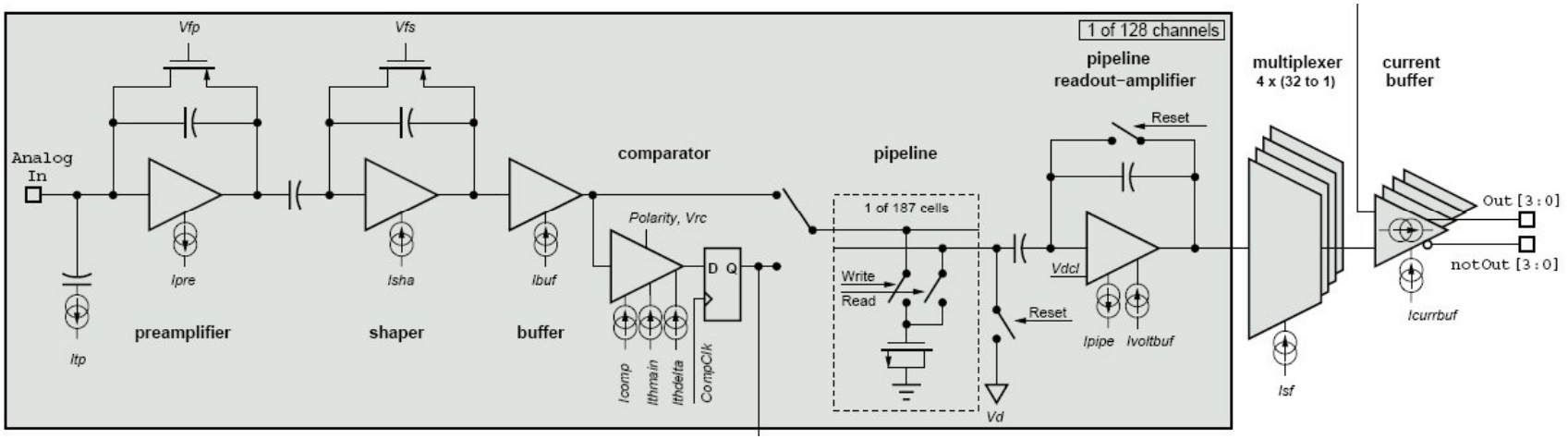
- Designed by the ASIC laboratory of Heidelberg
- Common read-out chip for LHC
  - Produced in quantities sufficient for detector replacements plus R&D needs



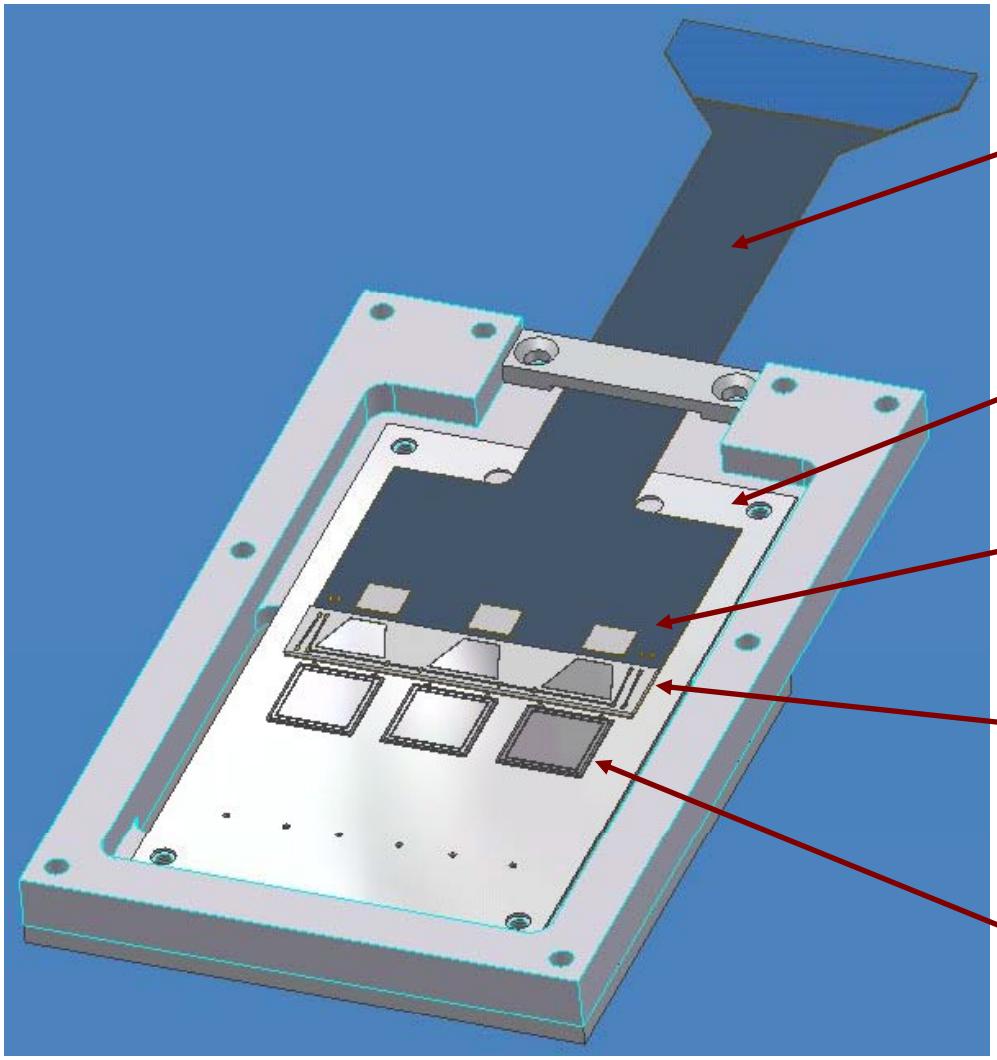


The Beetle chip - Features

- Designed for both electron and hole read-out
- Pre-amp and shaper with configurable integration time.
- Binary read-out in parallel to analogue
- Analogue pipeline – with configurable length
- Analogue data out on 4 serial links per chip
- 900 ns to read out one event – 1.1 MHz L0 trigger rate



The generic R&D modules



Pre-production hybrids from LHCb Inner Tracker

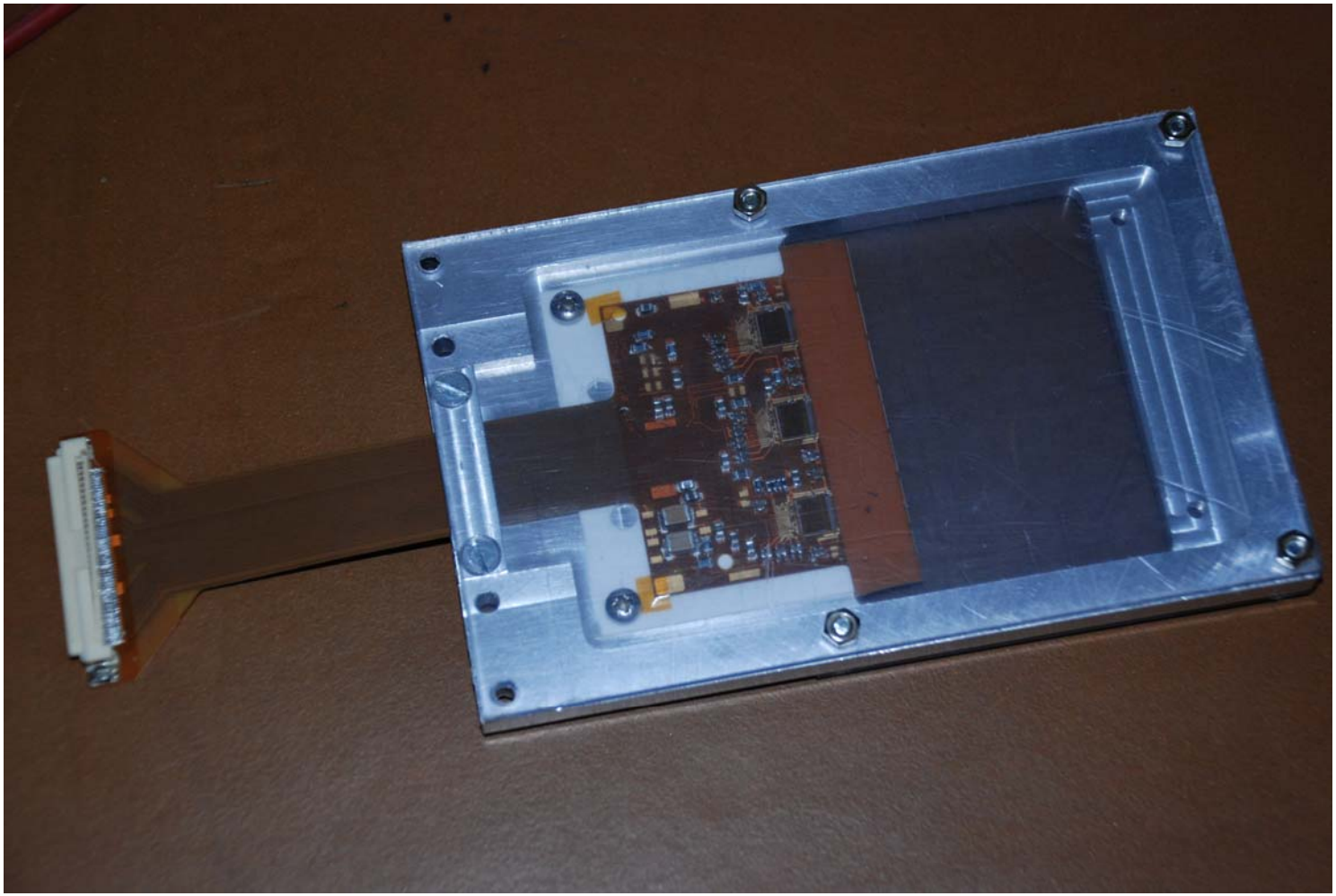
Aluminia baseboards (96% Al_2O_3, Coors Tek)

Beetle chips

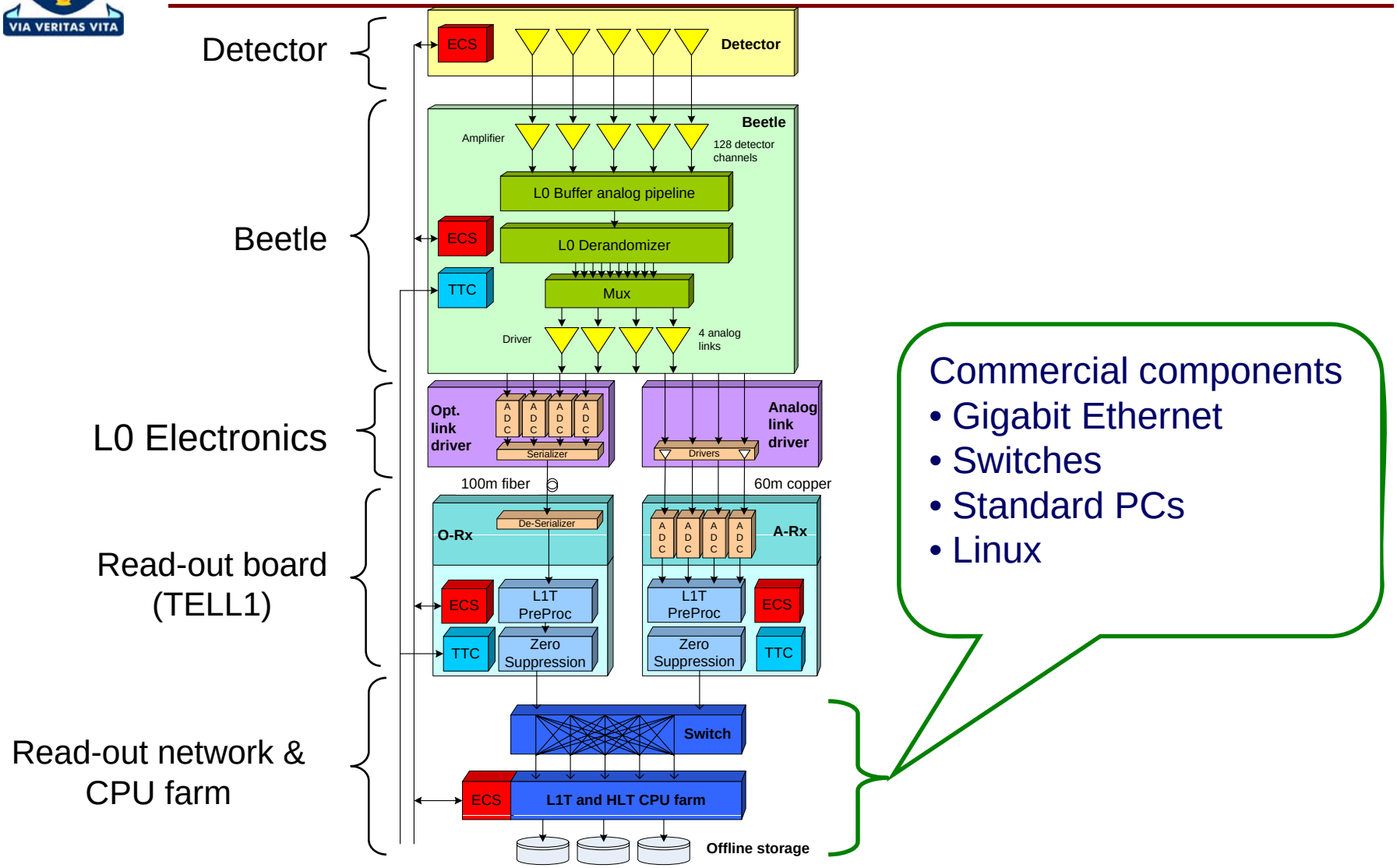
Pitch Adaptors (produced in Glasgow)

Sensors

R&D module -IRL



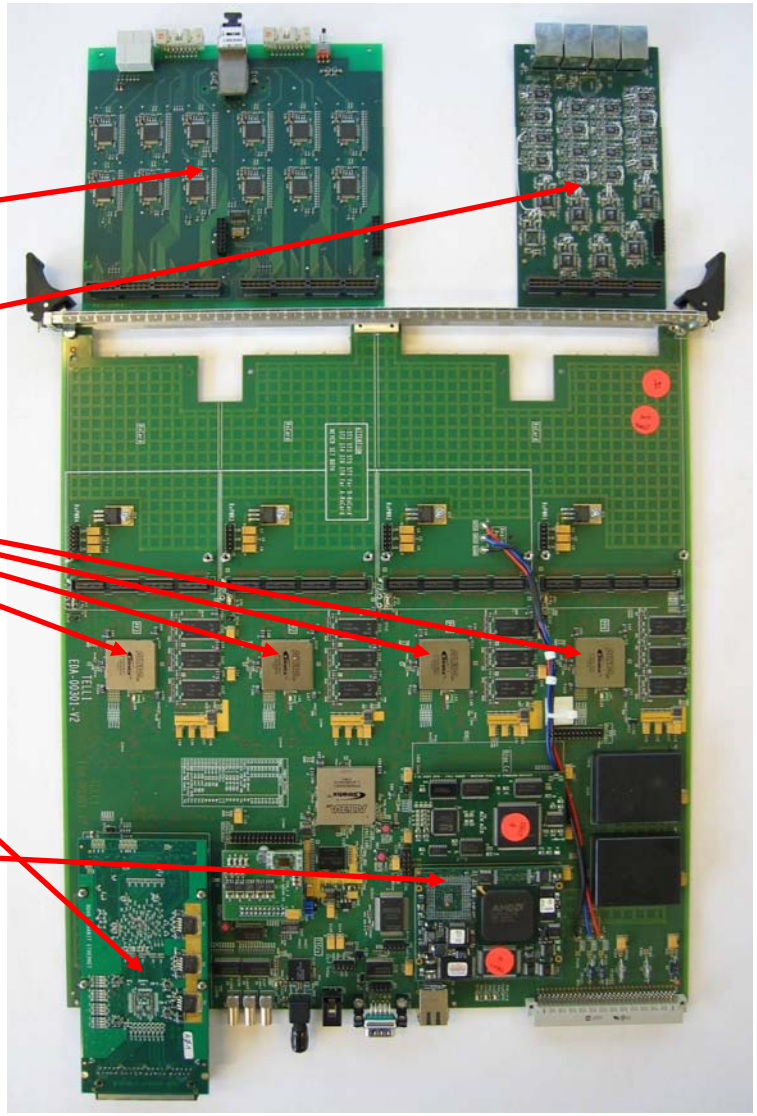
The LHCb read-out system



Commercial components
- Gigabit Ethernet
- Switches
- Standard PCs
- Linux

The TELL1

- Two types of custom made inputs
  - digital, optical
  - analogue, electrical
- On-board signal processing
- Standard Gigabit Ethernet ports output
- Control via Credit Card PC (linux)



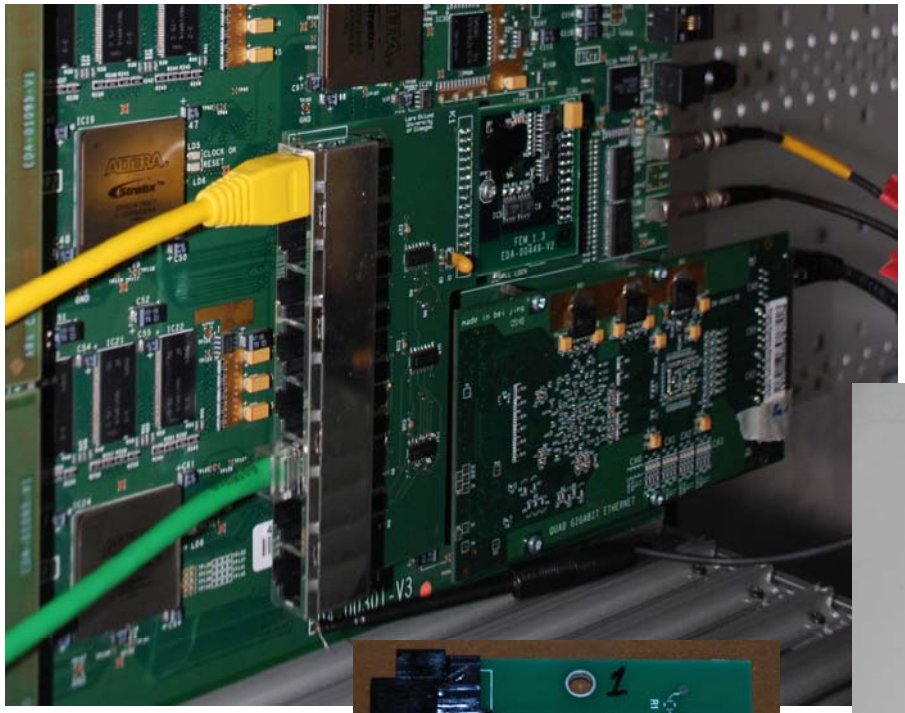
Stand-alone system (1)

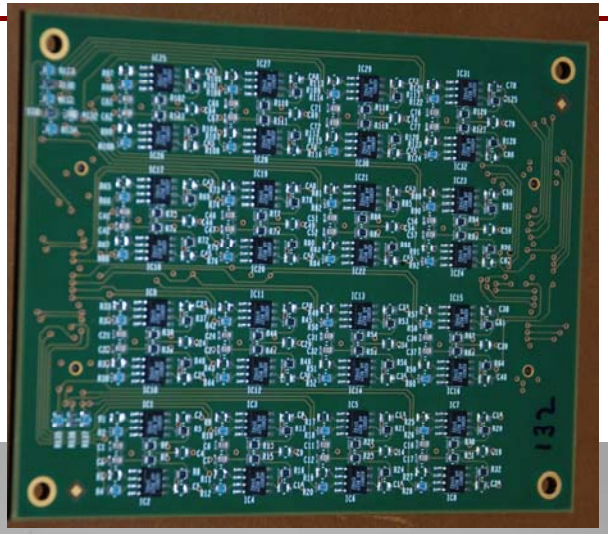
- The TELL1 and control system in LHCb
  - Fully featured
  - Rather complicated
- Modified for R&D purposes
  - Generate the control signals via the TELL1
  - DAQ & control sufficient for 4 R&D modules (4 Beetles per module)
  - LHCb read-out network and PC replaced with a desktop PC
  - Only needs power and Ethernet connection

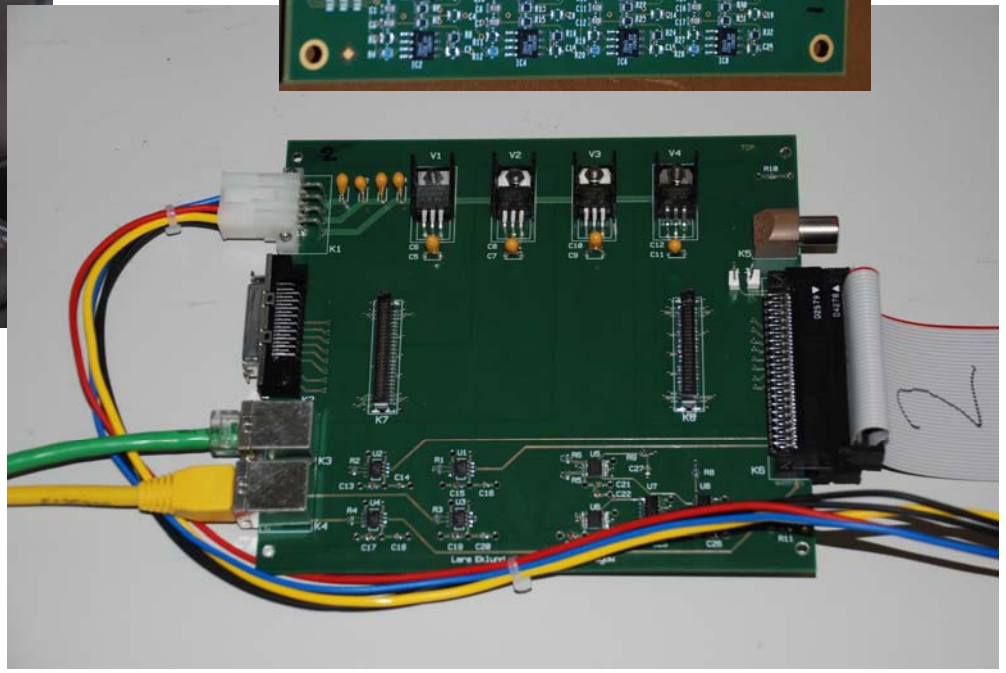
Stand-alone system (2)

- Three PCBs designed
  - Control fan-out:
    - Takes clock, control and configuration signals from TELL1.
    - Signals transmitted on two Cat5 cables.
  - Driver board:
    - Voltage regulators for Beetles and on-board electronics
    - Signal repeaters for clock, control and configuration signals
    - Signal repeaters for data links.
  - Patch card
    - Interface from Driver board to the hybrid pig-tail connector
    - Driver board connector is generic (KEL80), could easily be adapted to other hybrid designs by changing the patch card.

Stand-alone system (3)







Software issues

- Developed for LHCb and is available
- Control software
  - c-code libraries and executables on the Credit Card PC
  - PVSS framework components fully featured and with GUI
- Event builder
  - Linux application on receiving PC
  - Easy to write your own…
- Analysis framework
  - LHCb software (fully featured but complicated)
  - Easily exported to stand-alone analysis framework

Test beam experience

- Successfully used during the ATLAS 3D test beam
  - Strange feature in I^2C configuration under investigation…
- Synchronised read-out with the Bonn telescope
- TELL1 copes with ***very*** high trigger rate
  - Limited by receiving PCs capacity
  - 5 consecutive samples for each telescope trigger
- Data streams merged off-line
  - For results see Gregor Pahns talk tomorrow
- Will now be used for source tests in the lab

Summary and outlook

- A system to test new strip devices in a realistic read-out scheme was built.
- It features 40 MHz analogue readout, works equally well for n and p side read-out.
- Control and DAQ software in place
- Successfully used in the ATLAS 3D test beam
- Ready to be used for source tests in the lab
- Could, if the manpower would be made available, be extended to a 40 MHz telescope which copes with very high event rates.