Open Hardware Development

for CERN's Accelerator Control Systems

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CERN PH-ESE Seminar

Outline

Outline

CERN Beams Controls group - BE/CO

Responsible for

- Controls infrastructure for all CERN accelerators, transfer lines and experimental areas
- General services such as machine and beam synchronous timing and signal observation
- Specification, design, procurement, integration, installation, commissioning and operation

Supports

- beam instrumentation, cryogenics, power converters, etc.

Software

- Linux device drivers, C/C++ libraries, test programs

Beams Controls standard kit

Hardware kit

- analog and digital I/O
- level converters, repeaters
- serial links, timing modules

Currently, February 2013

- about 120 module types
- most are custom designed: only 1 in 4 is commercial
- 1 in 4 is obsolete

Outline

Bus standards for new designs

Two bus standards

- VME64x
  - 6U, large front-panel space, may use rear transition module
- PICMG 1.3
  - Industrial type PC with the processor on a plug-in board
  - Internal buses PCI Express and PCI

Need for a mezzanine approach

- Functions (e.g. ADC, TDC) are needed for both buses.
- Would need twice as many designs, more if additional standards are needed (PXIe, xTCA).

Advantages of the carrier/mezzanine approach

Re-use

- One mezzanine can be used in VME and PCIe carriers.
- People know standards, more likely to re-use or design for it.

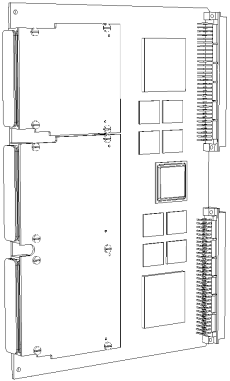
Reactivity

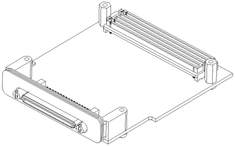
- Carrier: place and route a complex FPGA/Memory PCB once.
- Mezzanine: small and easier to route cards, easy assembly.

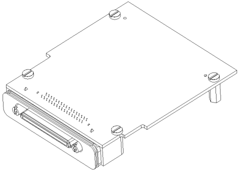
Rational split of work

'Controls' can design the carrier, 'Instrumentation' an ADC mezzanine, 'Beam Transfer' a TDC, etc.

FPGA Mezzanine Card (FMC) standard – Vita 57.1

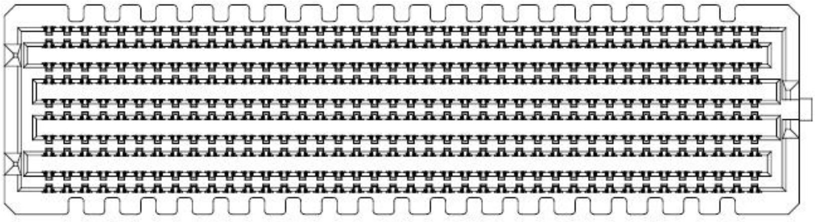






Courtesy of VITA: http://www.vita.com/fmc.html

Connectors

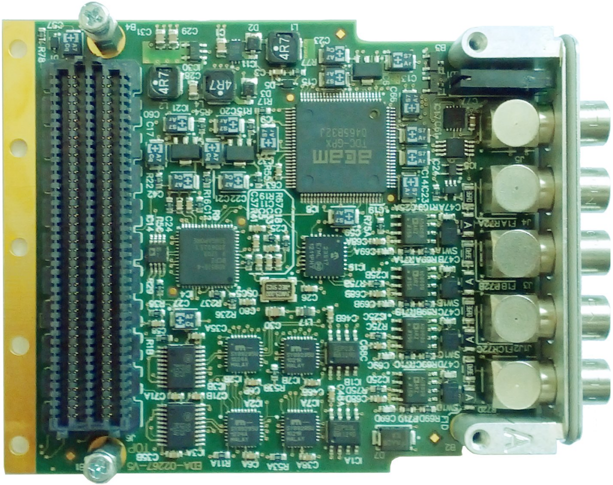


- Low Pin Count (LPC) and High Pin Count (HPC) variants with 160 and 400 contacts respectively.
- Ball Grid Array (BGA) characterized for high bandwidth applications.
- Difficult to solder!

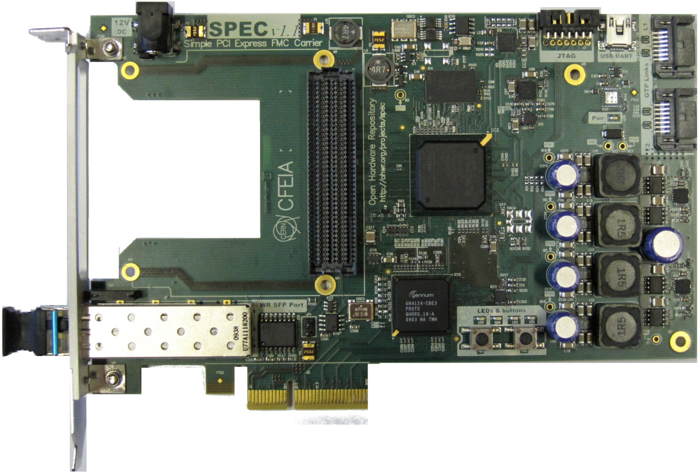
Agnosticism of FMC

- The function of pins is not defined (no bus protocol).
- Pin function, sense – input or output – and electrical standard are defined at FPGA configuration time.
- Carrier reads FMC identity through an I2C serial bus and configures the FPGA accordingly.
- Unfortunately this flexibility makes that interoperability is not guaranteed (Vadj, HPC/LPC, clock signals, levels, board-to-board height).
- We use: Vadj=2.5V, LPC (160 pin), M2C clock only (as LPC), LVDS and LVTTL signal levels, 10mm height.

Example of an FMC mezzanine: 4-channel Fine Delay



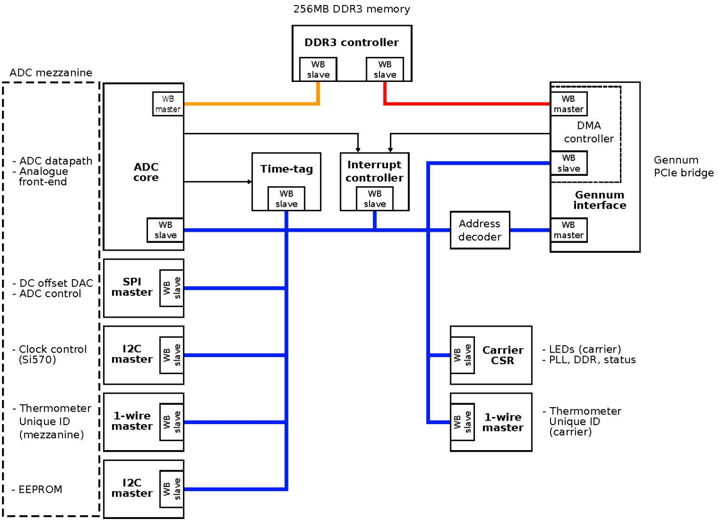
Example of a PCI Express FMC carrier (SPEC)



Inside the FPGA: Wishbone

- System becomes pretty complex: System-on-a-chip
- Build up from re-usable IP blocks
- Connect blocks with Wishbone bus
  - open standard
  - simple address/data bus
  - extended with pipelined mode
  - many cores already available
- We developed a design infrastructure
  - scripts to interconnect Wishbone IP blocks
  - IP blocks with descriptors to aid driver development
  - tools to compile designs with distributed sources
  - library of Wishbone IP blocks

Wishbone-based System-on-Chip architecture (ADC)



Outline

Why we use Open Hardware 1/2

Get a design just the way we want it

We specify fully the design.

Peer review

Get your design reviewed by experts all around the world.

Design re-use

When it's Open, people are more likely to re-use it.

Healthier relationship with companies

No vendor-locked situations. Companies selected solely on the basis of technical excellence, good support and price.

Why we use Open Hardware 2/2

Dissemination of knowledge

- One of CERN's key missions!

Spend money where you or your funding agencies want

- Makes life easier for public institutions.
- Opens the door to smaller companies with good local support.

Dispelling the commercial vs open myth

	Commercial	Non-commercial
Open	**Winning combination. Best of both worlds.**	Whole support burden falls on developers. Not scalable.
Proprietary	Vendor lock-in.	Dedicated non-reusable projects.

Open Hardware Repository – ohwr.org

A web-based collaborative tool for electronics designers

- Wiki, News
- File repository
- Issues management
- Mailing list

Fully open access

- All information readable by everyone, without registration

Server made itself of open software

- ChiliProject (a fork of Redmine)
- SVN/GIT for version management, integrated in OHR

Example of an OHR project

HOME PROJECTS LICENSES COMPANIES SIGN IN REGISTER

FMC PROJECTS » SIMPLE PCIE FMC CARRIER (SPEC)

OVERVIEW | WIKI | ACTIVITY | MAILING LIST | ROADMAP | ISSUES | NEWS | DOCUMENTS | FILES | REPOSITORY

OVERVIEW

A simple 4-lane PCIe carrier for a low pin count FPGA Mezzanine Card (VITA 57). It has memory and clocking resources and supports the White Rabbit timing and control network. Commercially available.
More info at the Wiki page

- Subprojects: **Software support for the SPEC board**
- Status: Release

Latest news

License

CERN OHL v1.1

OHR Status
February 2013

Projects

- About 52 hardware designs (of which 40 FMC projects)
- About 39 re-usable IP blocks
- General tools (9 projects)
  - Production test environment (Python based)
  - ADC performance test, WB slave generator, crossbar, ...

Partners

- Institutes: CERN, Soleil, GSI, Brazilian Light Source
- Universities: Bristol, Warsaw, Zurich, Pavia, Rockefeller, Cape Town, Heidelberg
- 16 Companies (hw design, sw and drivers, production)

CERN FMC projects in OHR – some examples

FMC Carriers

- VME64x (BE/BI & BE/CO), VXS (BE/RF)
- PCIe (BE/CO), PXIe (EN/ICE & BE/CO), AMC (PH/ESE)

FMC Mezzanines

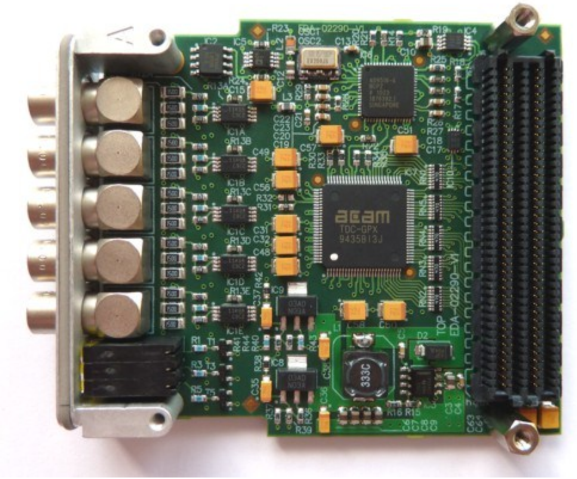
- ADC's, sampling speeds: 100 kSPS, 100 MSPS
- TDC and Fine delay: 1 ns resolution
- Digital I/O: 5 channels, 16 channels

Stimulates collaboration between CERN groups

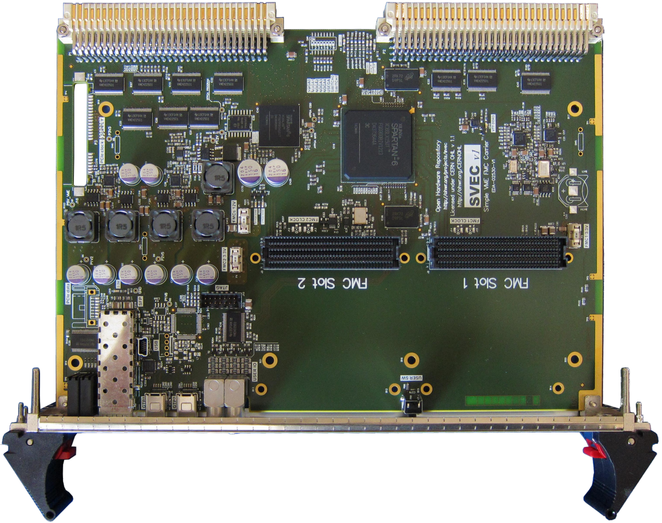
- VME64x: BE/BI & BE/CO
- TDC: TE/ABT, TE/CRG & BE/CO

Example of an FMC mezzanine: 5-channel 1ns TDC

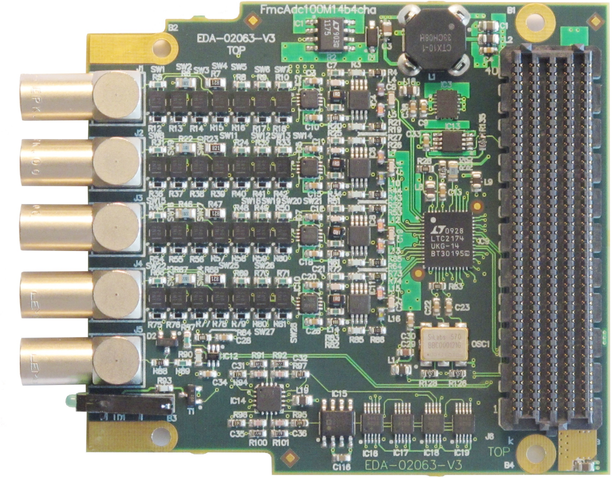
joint development by TE/ABT, TE/CRG & BE/CO



SVEC - Simple VME FMC Carrier



FMC mezzanine: 100 MSPS 14-bit 4-channel ADC



CERN non-FMC projects in OHR – some examples

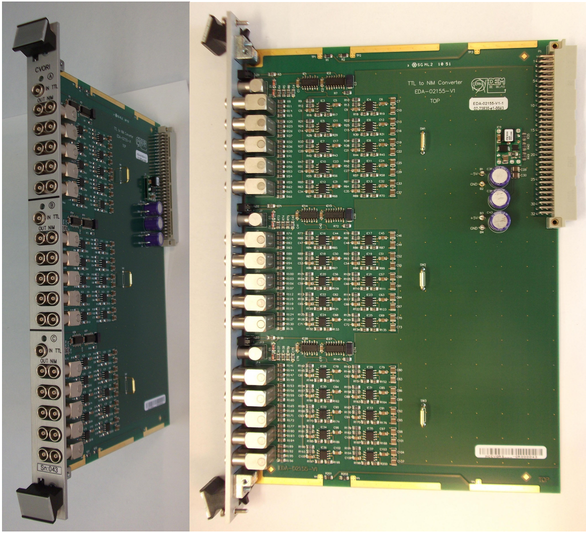
Hardware

- TTL to NIM/Blocking/RS485 level converters (VME)
- White Rabbit timing network switch
- Small footprint ARM-based computer

IP modules, Software and Tools

- Wishbone cores: DDR3 controller, VME64 core, serialiser
- RISC Processor core
- Time-to-Digital Converter core
- NanoFIP WorldFIP interface
- Production test environment for PCIe & VME (Python)

TTL to NIM converter



CERN Open Hardware License – ohwr.org/cernohl

Provides a solid legal basis

- Developed by Knowledge and Technology Transfer Group at CERN
- Open Software licences not usable (GNU, GPL, . . .)
- Defines conditions of using and modifying licenced material

Practical: makes it easier to work with others

- Upfront clear that anything you give will be available to everyone
- Makes it clear that anyone can use it for free

CERN Open Hardware License – ohwr.org/cernohl

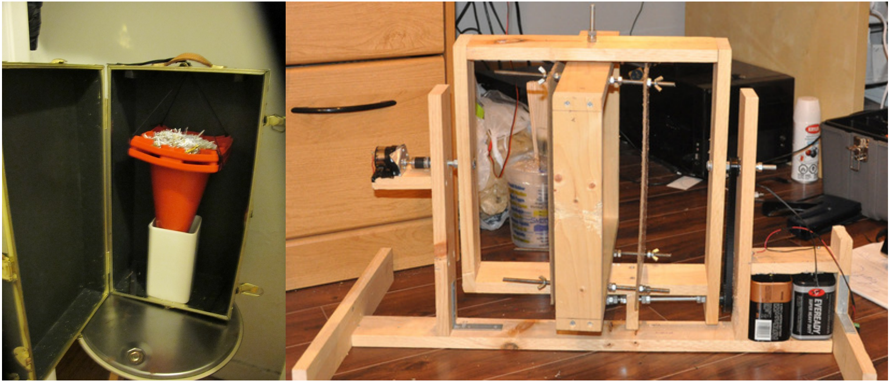
Same principles as Open Software

- Anyone can see the source (design documentation)
- Anyone is free to study, modify and share
- Any modification and distribution under same licence
- Persistence makes everyone profit from improvements

Hardware production

- When produce: licensee is invited to inform the licensor

Example of mechanics licenced with the CERN OHL



Worm farm - Rotocaster

Balloon mapping, Rockets, Small wind turbines, Open Beer ...

http://www.ohwr.org/projects/cernohl/wiki/CernOhlProjects

Outline

Case study – SPEC – Simple PCI Express Carrier

We started with a complex design

- Our first FMC carrier design
- Wanted to have lots of timing things on it
- Wanted it to be very flexible: one design does it all

And got results

- We built a few prototypes
- Actually a bit overdesigned, too complex and expensive

Case study – SPEC

PCIe FMC Carrier (PFC)
12-layer PCB

Case study – SPEC

Too complex, so we wanted to have a simpler board

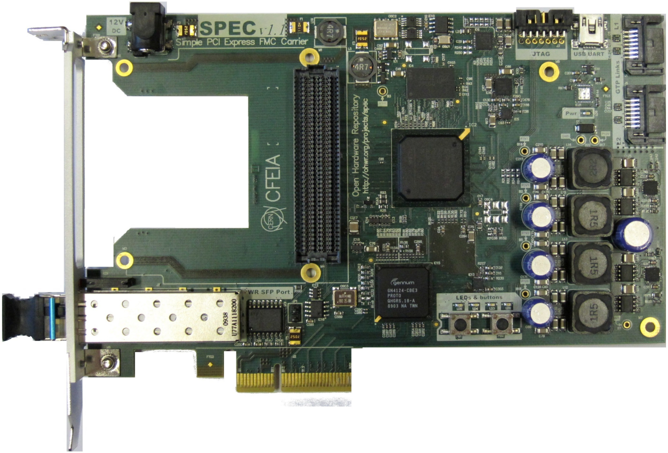
- Simple PCI Express Carrier (SPEC)
- Basically remove components from old design
- Optimise with new knowledge and re-layout

Industry got in

- We didn't have time to do the work
- Hired a small **company** (<15 persons)
- Review, review, review (specifications, schematics, pcb)
- CERN's design office generated final production files
- Used ohwr.org for all documentation

Case study – SPEC: Simple PCI Express FMC carrier

Made in Spain, The Netherlands & Poland



6-layer PCB instead of 12 on the PFC

Case study – SPEC

Make it a testable product

- Developed an FMC connector test card
- Developed a re-usable test environment (using Python)
- Developed go/no-go test suite

Redesign: V1, V1.1, V2, (V3,) V4

- 72 Issues registered and tracked in ohwr!

First series of 70 boards (production, guarantee)

- Solid specification, IPC norms for PCB fab and assembly
- Price Enquiry to 7 **companies** *having already PCIe products*. First delivery in March 2012. Now 3 produce!

Case study – SPEC

Users, incomplete list

- B-train system (CERN TE/MSC)
- CLIC Interlock System study (CERN TE-MPE)
- ATLAS Pixel IBL readout concept prototyping
- CNGS
- GEM detector readout (Creotech, PL)
- FAIR accelerator timing network (GSI)
- LHAASO telescope (Tsinghua University, China)
- Industry

http://www.ohwr.org/projects/spec/wiki/Users

Case study – 100 MSPS 14-bit 4-channel ADC

Design

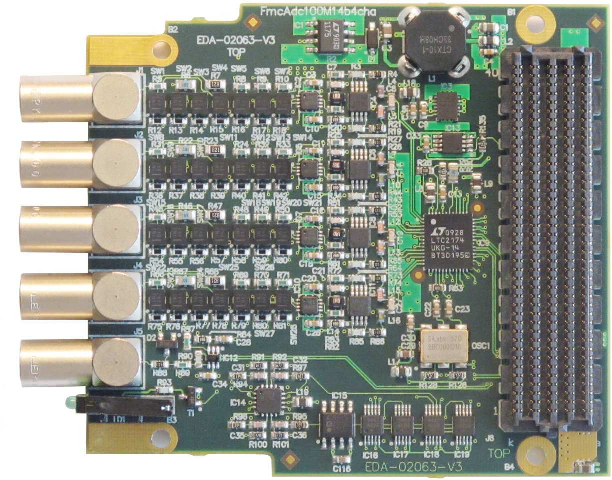
- Design by CERN student
- A small specialist **company** designed the front-end
- Review, review, review
- Design process well documented (mails, documents)
- 46 Issues documented
- 4 prototype versions, produce V5

CERN Price Enquiry for 40 boards (production, guarantee)

- Price Enquiry to five companies *that produce ADC boards*
- Useful design feedback (schematics and PCB layout) from **company**. Delivered in April 2012.

Case study – 100 MSPS 14-bit 4-channel ADC

Made in The Netherlands



Case study – 100 MSPS 14-bit 4-channel ADC

Potential users who contacted us

- BPM Linac4 (CERN BE/BI)
- Frame grabber for BSRT emittance meter (CERN BE/BI)
- PSB pick-ups (CERN BE/BI)
- Septum. Booster Trajectory Measurement (CERN TE/ABT)
- OASIS general purpose (CERN BE/CO)
- Italian Hadron Therapy Centre, BPM system (CNAO)
- Agata experiment (INFN, PH/UCM)
- Culham Centre for Fusion Energy (CCFE)
- Advanced Photon Source (Argonne National Laboratory)
- Radio Telescope (Oregan State University)

Experience with Industry

Product Design

- Needs additional effort to make CERN designs a Product.
- Particular effort to reduce the Bill of Material.
- Precise production documentation. DEM's output perfect.
- Automated test bench (serious effort).

Industry and the OH concept

- Open Hardware is new and not always understood.
- Need to explain companies the opportunities and risks.
- Companies think they compete with assembly companies. We ask only companies that can also give support (guarantee, repair, improve).
- Needs time from us and guts from companies.

Experience with Industry
February 2013

Companies used (usually paid for)

- 15 European companies
- 1 US company (no CERN project)

Types of work

- Hardware: development, production
- Software: VHDL firmware, drivers
- Usually small projects (<2 months work), speeds up projects, gets in specialist knowledge
- Small companies can play a large role
- Production: follows CERN purchasing rules (competition)

Experience with Industry

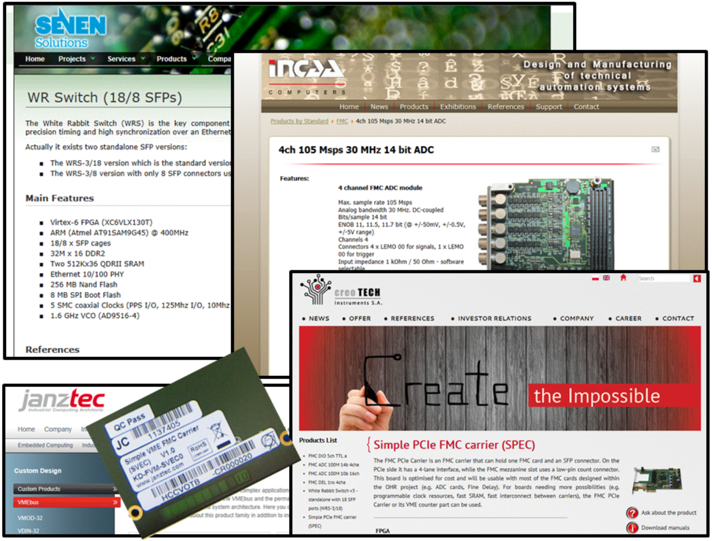
Examples of re-use of work

- Two companies modified SPEC carrier design.
  - larger FPGA (for software radio), PXIe bus version
- A company modified ADC100M design.
  - other input filter, high-voltage front-end
- A company re-uses White Rabbit spec for own product.
- A company re-used nanoFIP code for renovating trains.

Generates interaction

- Companies work together – building an ecosystem:
  - One sells a carrier, others sell mezzanines
  - One sells a WR switch, others sell WR nodes
- Once company makes its own designs available on OHR.
- Could negotiate component pricing for all partners.

Open products are real products™



Why does it seem to work?

Design

- Are fully Open, everything visible, incl. issues we had.
- Have a licence with a big name behind: CERN OHL.
- Design using standards. Have a killer app: White Rabbit.
- Have generic functionality (FMC carriers, ADC, TDC, ...)
- Have high quality designs and production documentation.
  - Many reviews; be open for feedback
  - DEM support for documentation
- Have web pages that are active and complete.
  - Manuals, FAQ, Status, Users
- Have Linux drivers available.

Why does it seem to work?

Interaction with industry

- Make easy to produce: have a production test system.
- Have a Technical Specification referring to IPC and JSTD.
- Place a single order to get things going.
- Verify product compliance to quality norms (DEM support).
- Stimulate to make it a catalog product of the company.
- Help these partners when possible, also in hard times.
- Help potential clients outside CERN, then send to industry.
- Help industry to take responsibility in support.
  - keeps our efforts scalable
- Have in-house knowledge of all steps.

What went wrong?

We could recover from it anyway.

Design

- Designs by industry not flawless. We reviewed.
- Our designs not flawless. Industry reviewed.

Test system

- Test system was broken during shipment.
- Some tests fail (voltage margins set wrongly, initialisation); other tests don't give enough information.

Production

- Bad PCB production (unreadable silkscreen, bad plating).
- Bad assembly (FMC connector. Bad soldering & cleaning).
- Delivery of wrong version. Late deliveries.

Future work

OHR site

- Quality control important to keep site interesting.
  - Not all projects are active or store all information.

Consolidate our designs

- Consolidate firmware and Linux drivers. Make Releases.
- Consolidate documentation (manuals, FAQs, ...).

Improve re-usability with free electronics design tools

- Tools are expensive and do not interoperate.
- Existing free tools are not usable to make complex designs.
- Therefore we stimulate the development of free tools:
  - VHDL Simulator (extension of Icarus Verilog simulator)
  - Schematics & PCB editor (catalysing KiCAD development)

Outline

Why we use Open Hardware

Does it hold its promises?

Get a design just the way we want it – Yes

With own designers and with outside help (industry, institutes).

Peer review – Yes

From different groups. Also by industry.

Design re-use – Yes

- SPEC, SVEC and ADC100M have users and lots of interest.
- SPEC design is being copied and re-used in other designs.

Healthier relationship with companies – Yes

- Are much more free to use small companies.
- Not tied to any single company.

Conclusions

- The electronics that we support cannot be black boxes.
- Open Hardware has many advantages.
  - Anyone can help in developments and make improvements.
  - Allows to work differently with industry (design work, smaller companies).
  - Not tied to a single company for production and support.
- CERN Open Hardware Licence provides a legal basis.
- Using standards (VME64x, PCIe, FMC, Wishbone) attracts users and improves re-usability.
- OHR site is practical for engineers and is stimulating.
- OHR site contains many re-usable IP modules.
- Seven of CERN's designs are already commercialized.
- Four years of experience show it works!

Open products are real products™