Low Mass

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Outline

- Aluminum circuits
  - Material budget /General possibilities
  - Micro-via
  - Finishing possibilities
  - Different examples
- Wire bonding alternatives
  - Wire bonding
  - Stud bump
  - Embedded active devices
- Low mass cooling structures
  - Polymer Micro channel

Material budget

Material	Radiation length [cm]	Density [gr/cc]	Resistivity [uohms*cm]
Gold	0.3	19.3	2.4
Copper	1.4	9.0	1.7
Aluminum	8.9	2.7	2.7
Glass epoxy	19.4		
Polyimide	29.0		
Beryllium	35.3	1.9	3.3

Copper is close to 6.5 times less transparent than aluminum
And aluminum has only 1.6 times the resistivity of copper
Polyimide is 1.5 times better than glass epoxy.

Possibilities

- Aluminum
  - Laminated:
    - Foils of 15 , 30 or 50 um (crystalline)
  - Vacuum deposited:
    - From 5 to 30um (Amorphous)
  - Line and space:
    - 6 time the thickness (3 times for copper)
- Dielectrics
  - Polyimide :
    - 12um , 25um, 50um, 75um
    - Liquid polyimide from 1 to 10um
  - Photoimageable coverlay (modified epoxy):
    - 25um, 50um , 64um
  - Epoxy glue:
    - 5um (liquid), 12um , 25um
- Hole or vias
  - Minimum 0.05mm
- Sizes
  - Up to 2m x 50cm for single sided flex
  - Up to 1m x 10cm for double sided flex with plated holes
  - Up to 60cm x 10 cm for multilayer structures

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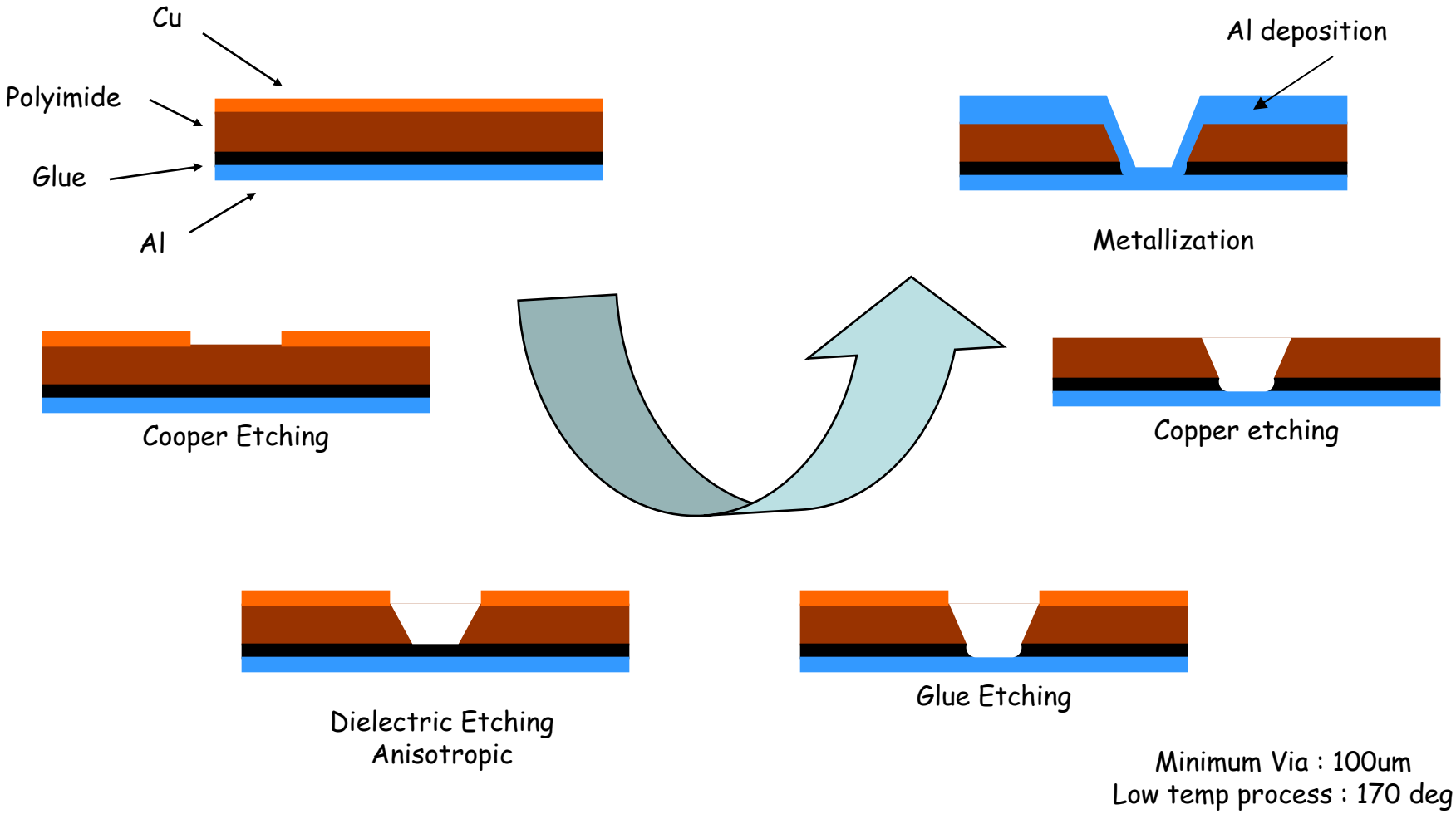
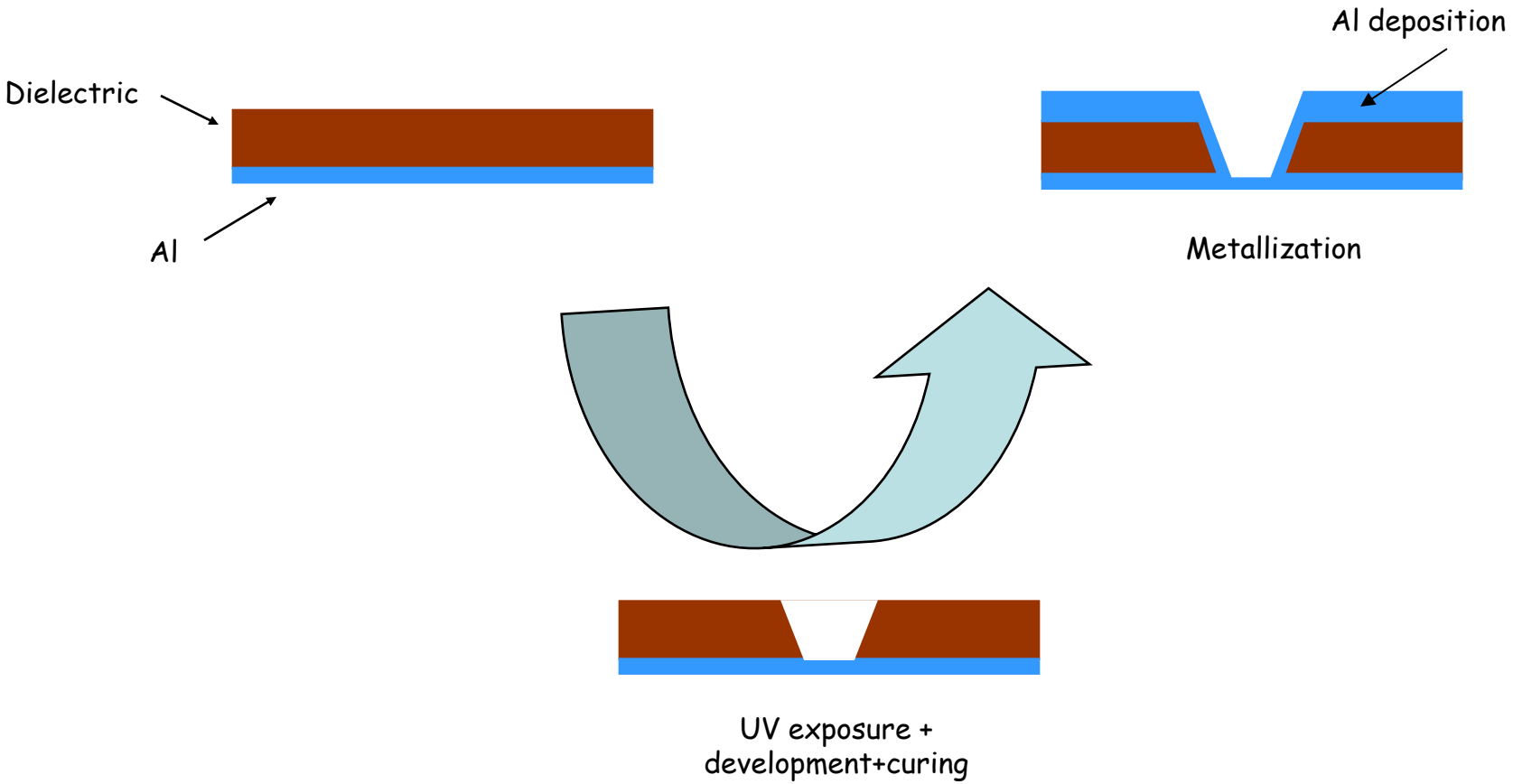
Micro-via , Process with Laminated PI



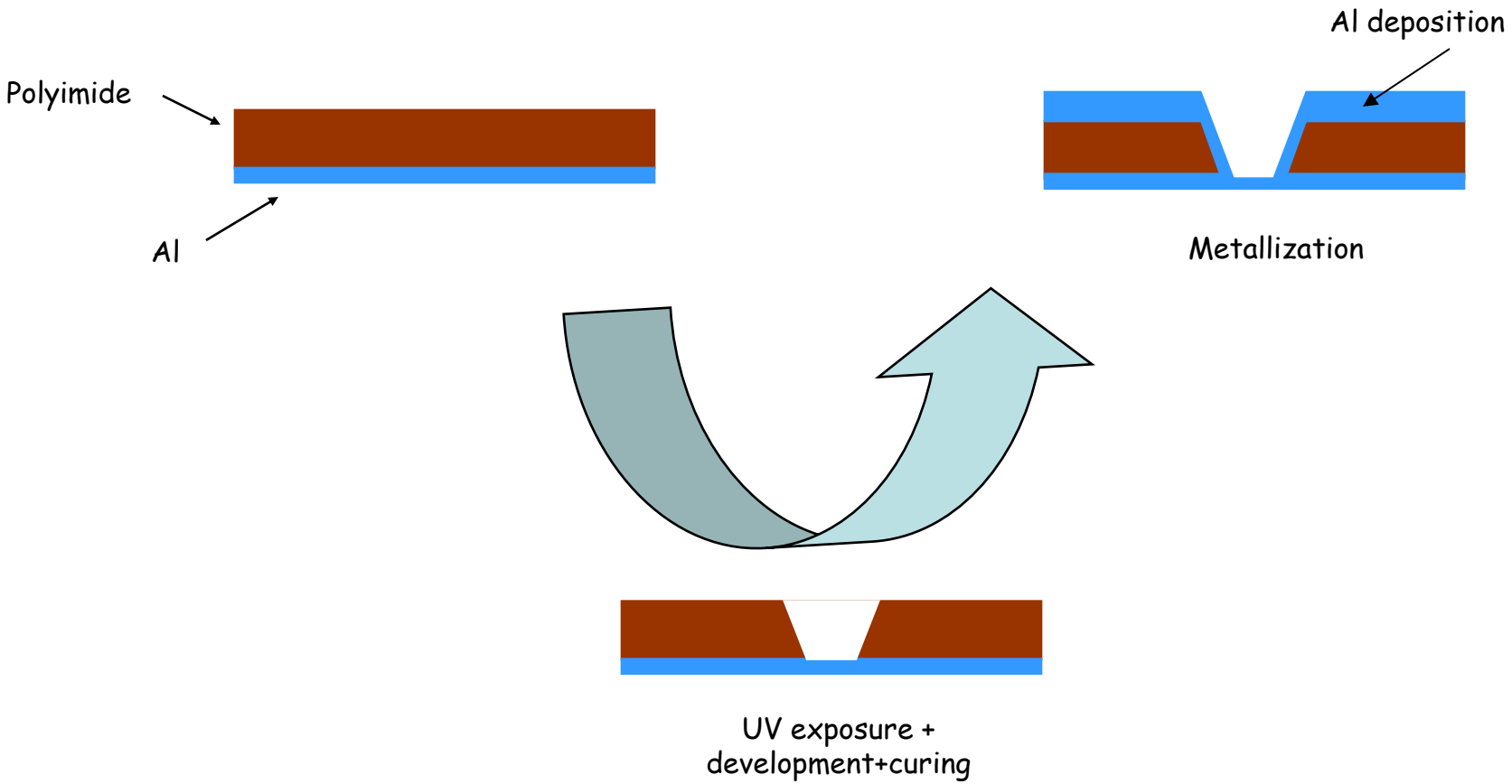
Minimum Via : 100um
Low temp process : 170 deg

Process with Photoimageable coverlay



Minimum Via : 50um
Low temp process: 170deg

Process with Photoimageable Polyimide



Minimum Via : 30um
High temp process : 300 deg

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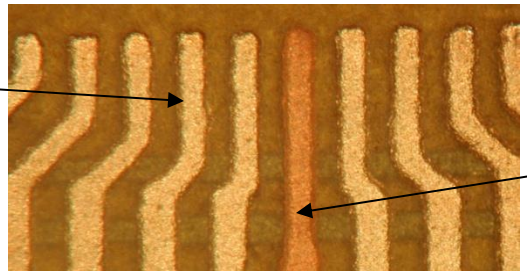
Finishing possibilities

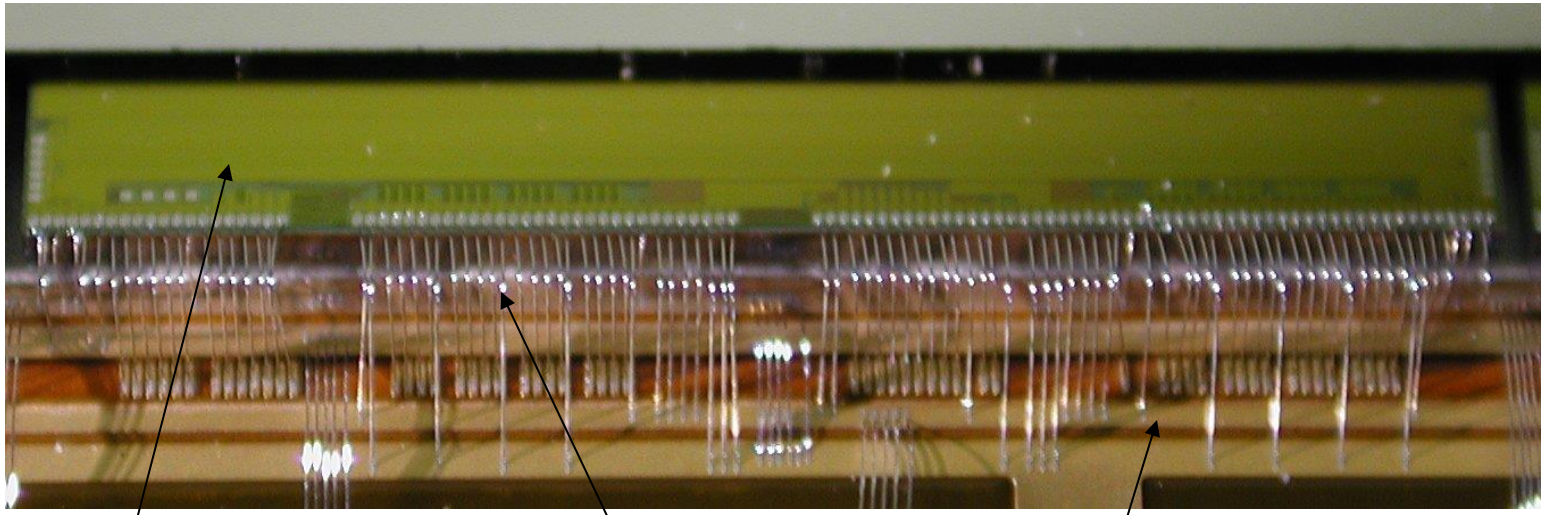
- For wedge aluminum bonding
  - No treatment in case of Crystalline Aluminum
  - Chemical NI/Au Plating on Amorphous deposited Aluminum
- For Au Bonding
  - No treatment in case of Crystalline Aluminum
  - Chemical NI/Thick Au Plating on Amorphous deposited Aluminum
- For soldering
  - Chemical NI/Au Plating

Bonding Close up view example

10umAl + 0.1umZinc + 10umNi + 0.1umAu
With sand blast pre-treatment



Plating defect



Ladder

Bonding

AL bus

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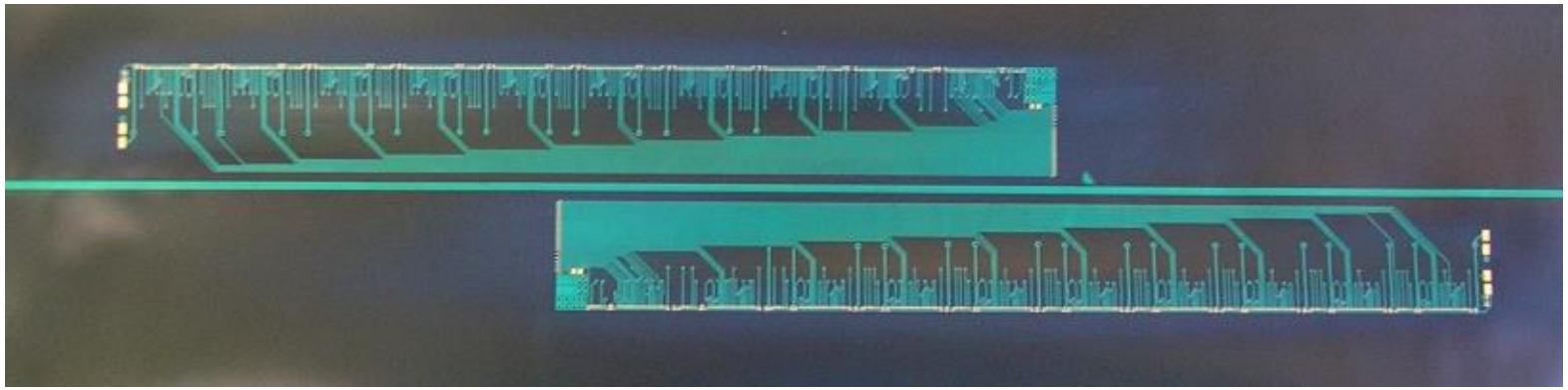
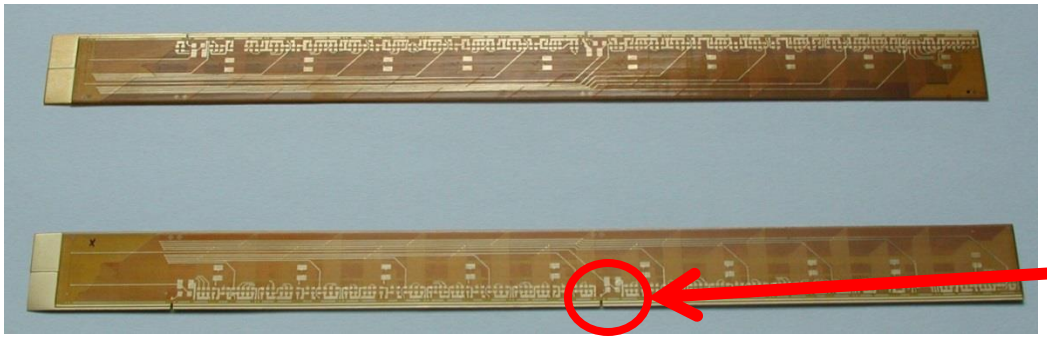
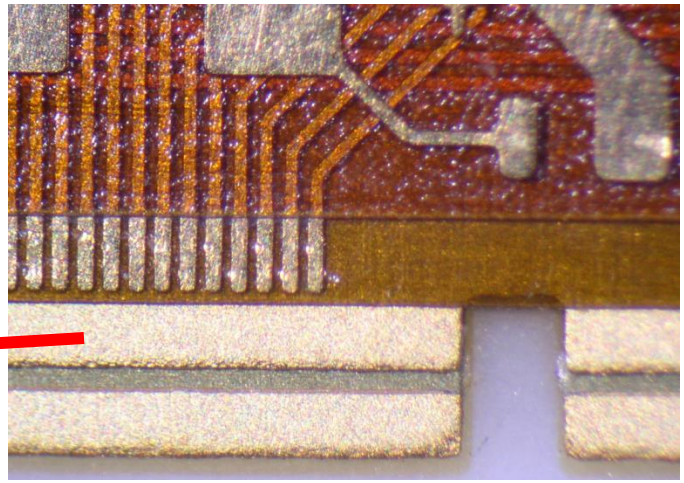
Al double Sided flex with plated through Holes



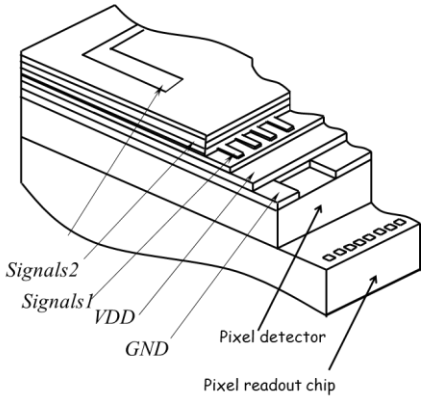
Via : 300um
Double sided
2x 30um Vacuum deposited aluminum
200um line and space
25um Kapton support
Size 300mm x 20mm
NI/AU finishing

5 layers ALICE Pixel Bus





Via : 100um
5 Aluminum layers
3x10um Vacuum deposited aluminum
2x50um laminated aluminum layer
100um line and 50 space
12um Kapton layers
Size 160mm x 16mm
Staircase shape on one side
170 buses produced
NI/AU finishing



8 layer ATLAS IBL Al/Cu mixed multilayer

Via min : 300um
5 Copper layers
2x50um laminated aluminum layer
70um line and 50um space
25um Kapton layers
Size 400mm x 20mm
Semi flex rigid structure
Rigidizers near connectors
20 buses produced
Milli-ohms level resistivity check
200 to 300 Mrad compatible
NI/AU finishing

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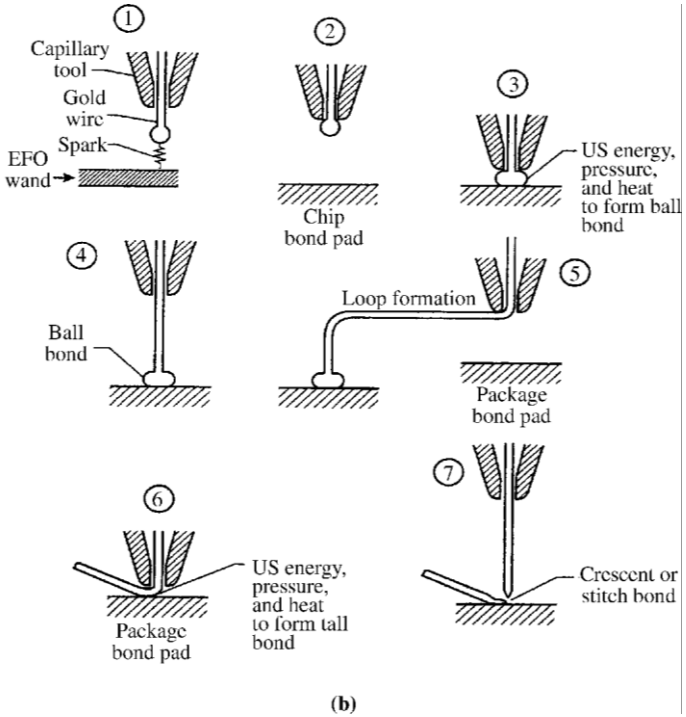
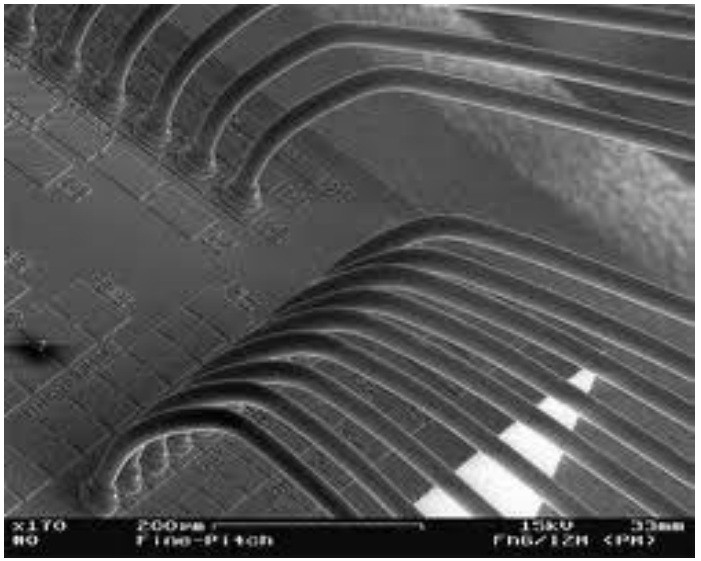
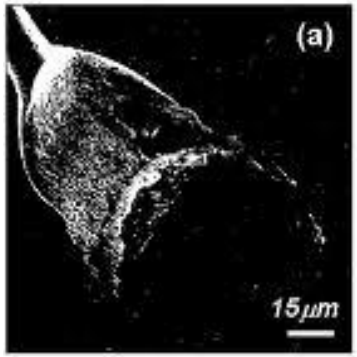
Gold Ball bonding

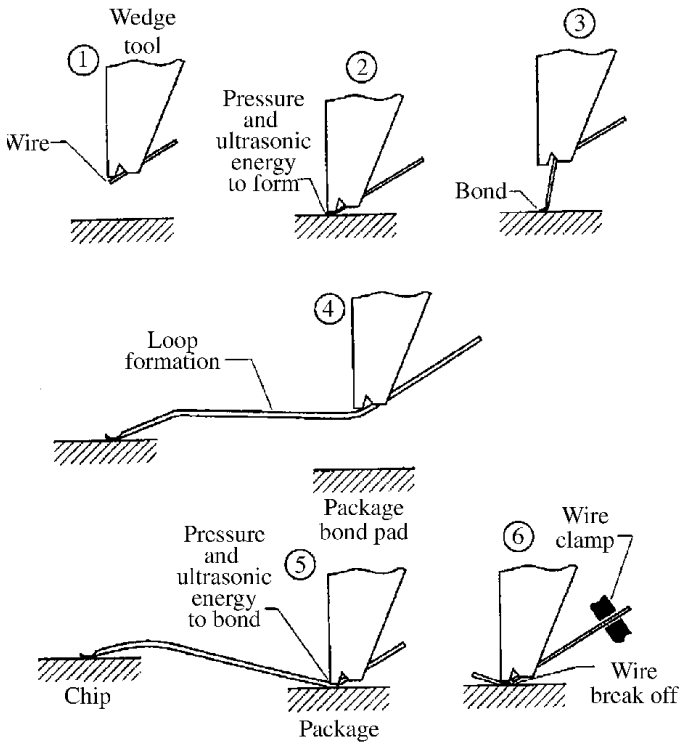


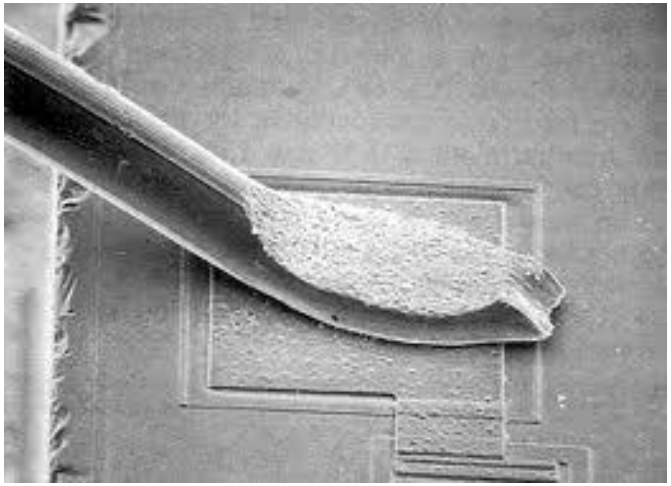




The lowest cost
Some limitation in fine pitch
Repair possible
But → Periferical connection→ dead zones
Needs mechanical and humidity protection (Al/Au) glob top

Wedge Aluminum or Gold





Medium cost
Fine pitch
Repair possible
But → Periferical connection→ dead zones
Needs mechanical and humidity protection (AL/Au) glob top

Wire bonding alternative

- Stud bonding
  - Low cost
  - Need a simple chip post processing
  - Limited minimum pitch (0.2mm to 0.3mm mini)
  - Can be sensitive to chip bow
- Micro-BGA – Chip scale package (CSP)
  - Heavy metal connection
  - Need Chip post processing
  - Really sensitive to chip bow
  - Limited minimum pitch (0.2mm to 0.3mm)
- Flip Chip
  - Ultra Low minimum pitch (50um)
  - High cost
  - Need Chip post processing
  - Sensitive to chip bow
- Embedded device
  - Low cost
  - Low minimum pitch (0.1mm)
  - Do not need chip post processing
  - Not sensitive to chip bow

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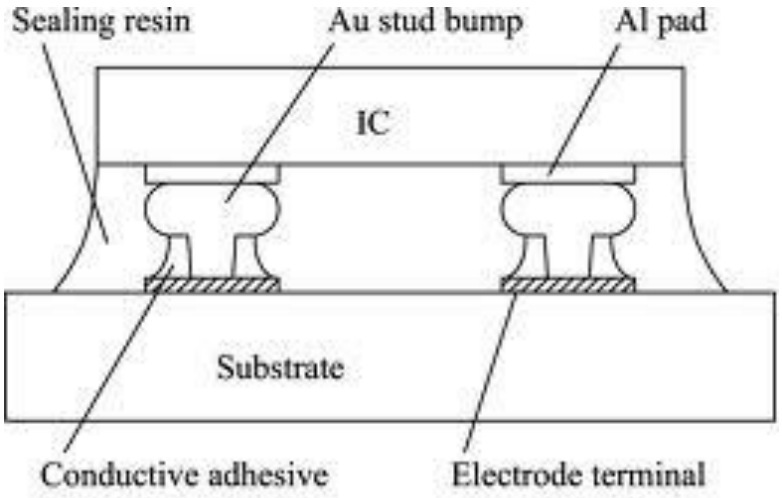
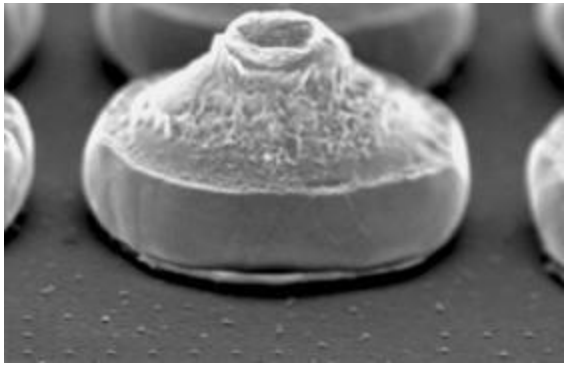
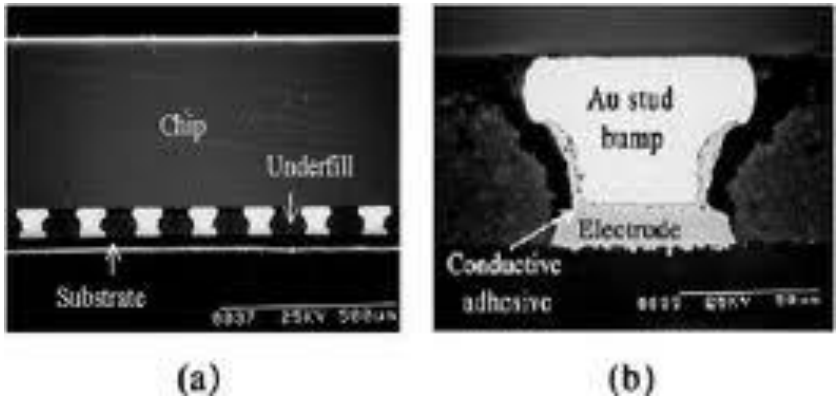
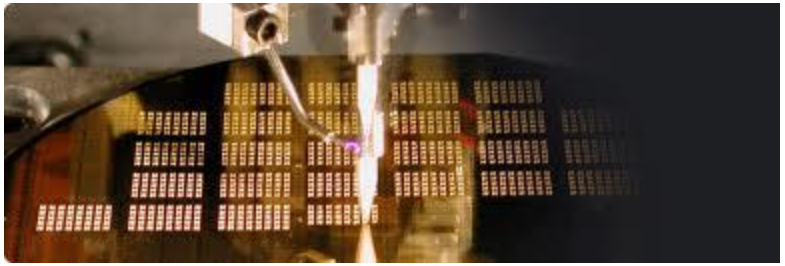
Isotropic conductive glue Stud bonding

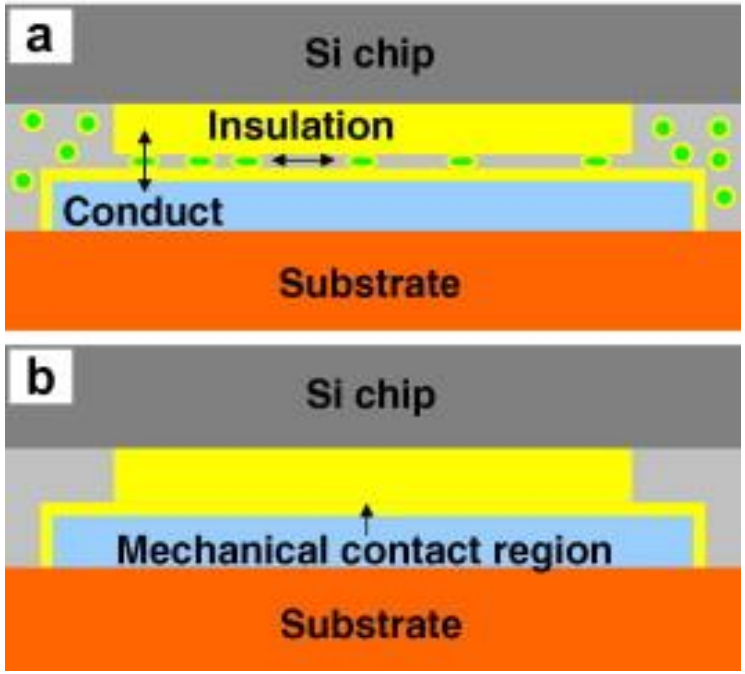


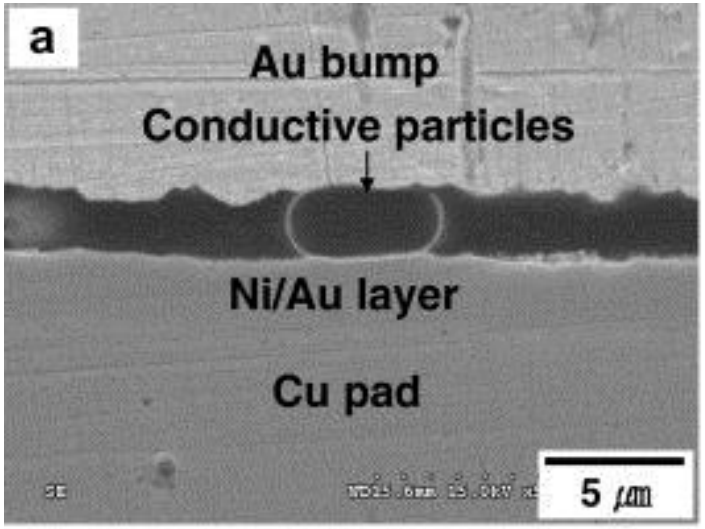






Z axis conductive glue contact or no conductive glue contact





Long term study

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16th European Workshop on "Materials for Advanced Meyallization 2007"
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Reliability of adhesive interconnections for application in display module

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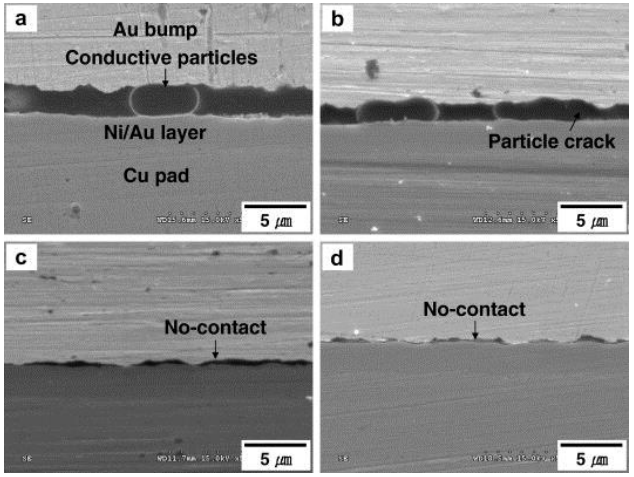

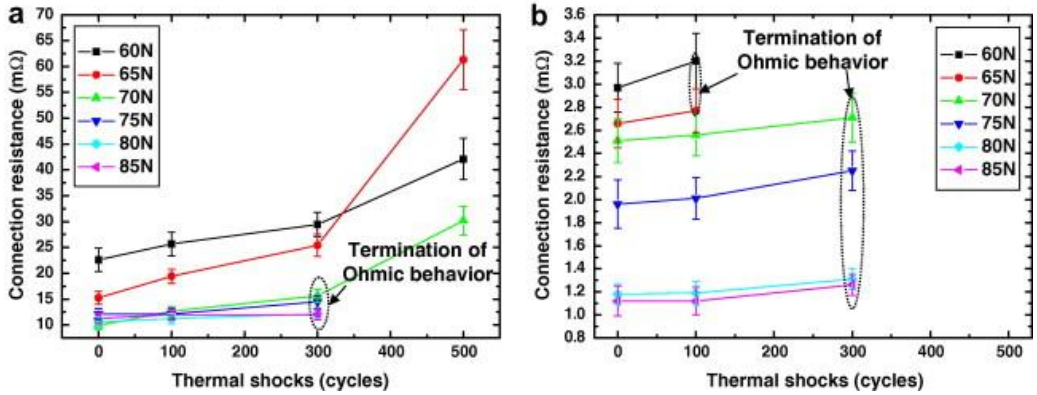

cycles : –40 °C to 125 °C (15 min cycle time, air to air, 6 min dwelling time)

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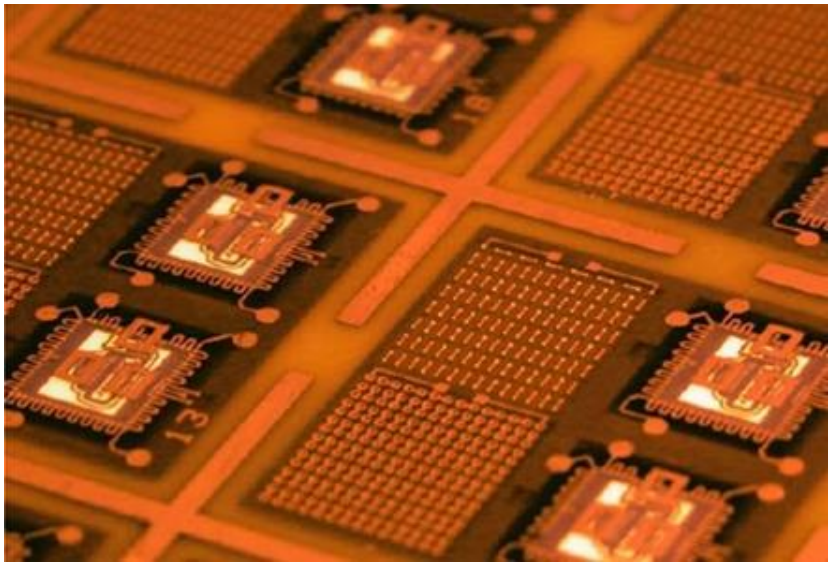
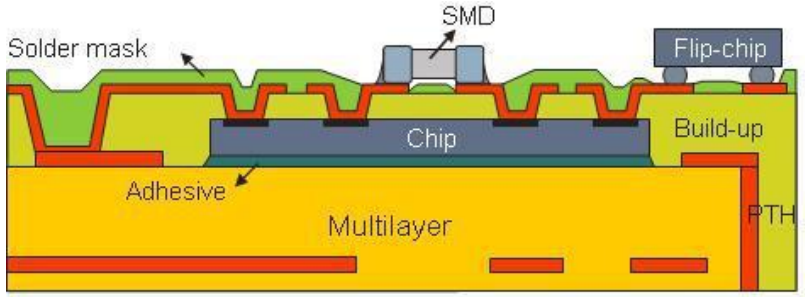
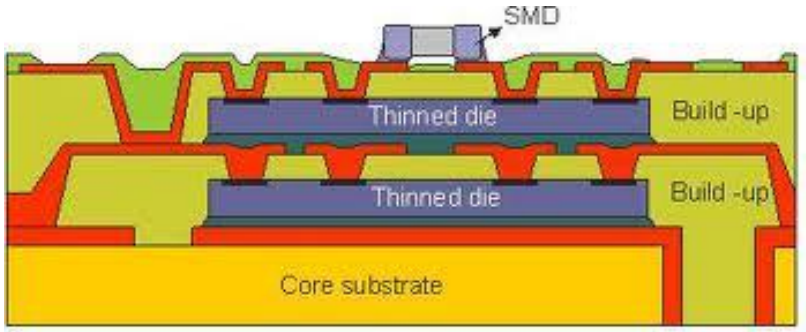
Embedded Chip situation in industry







Laser micro-vias
Thick copper pads on chip (15um)
100um vias
Position of pads : anywhere on the chip
100%compatible with PCB line
RCC glues
Thick or thin chip

Embedded Chip at CERN

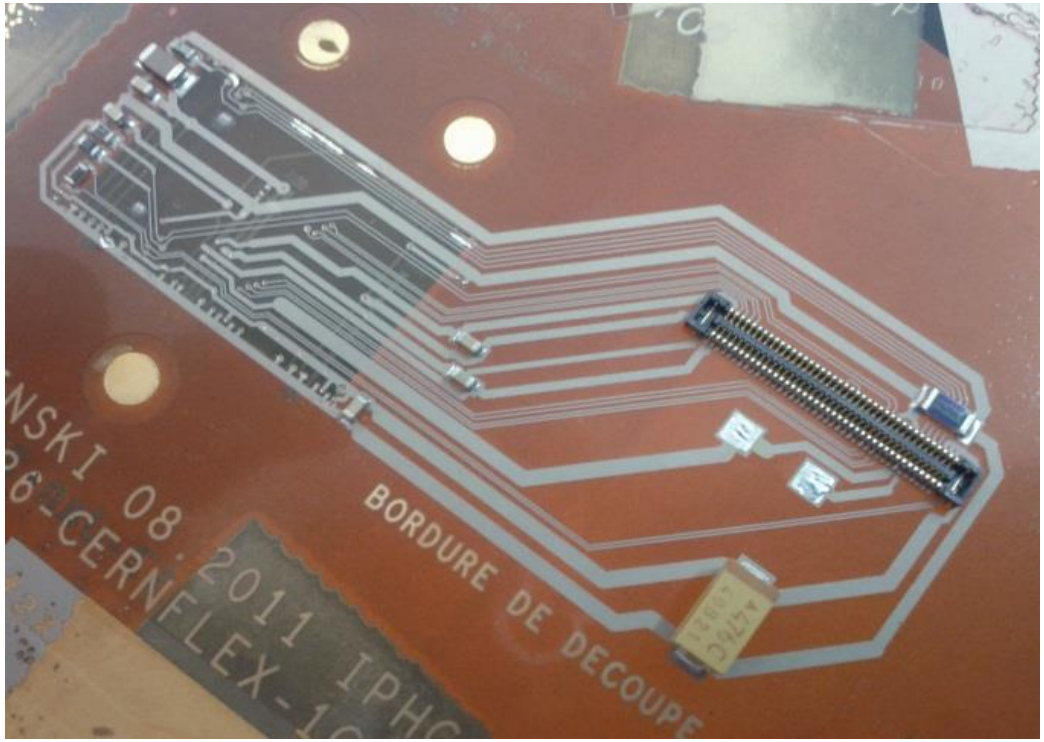
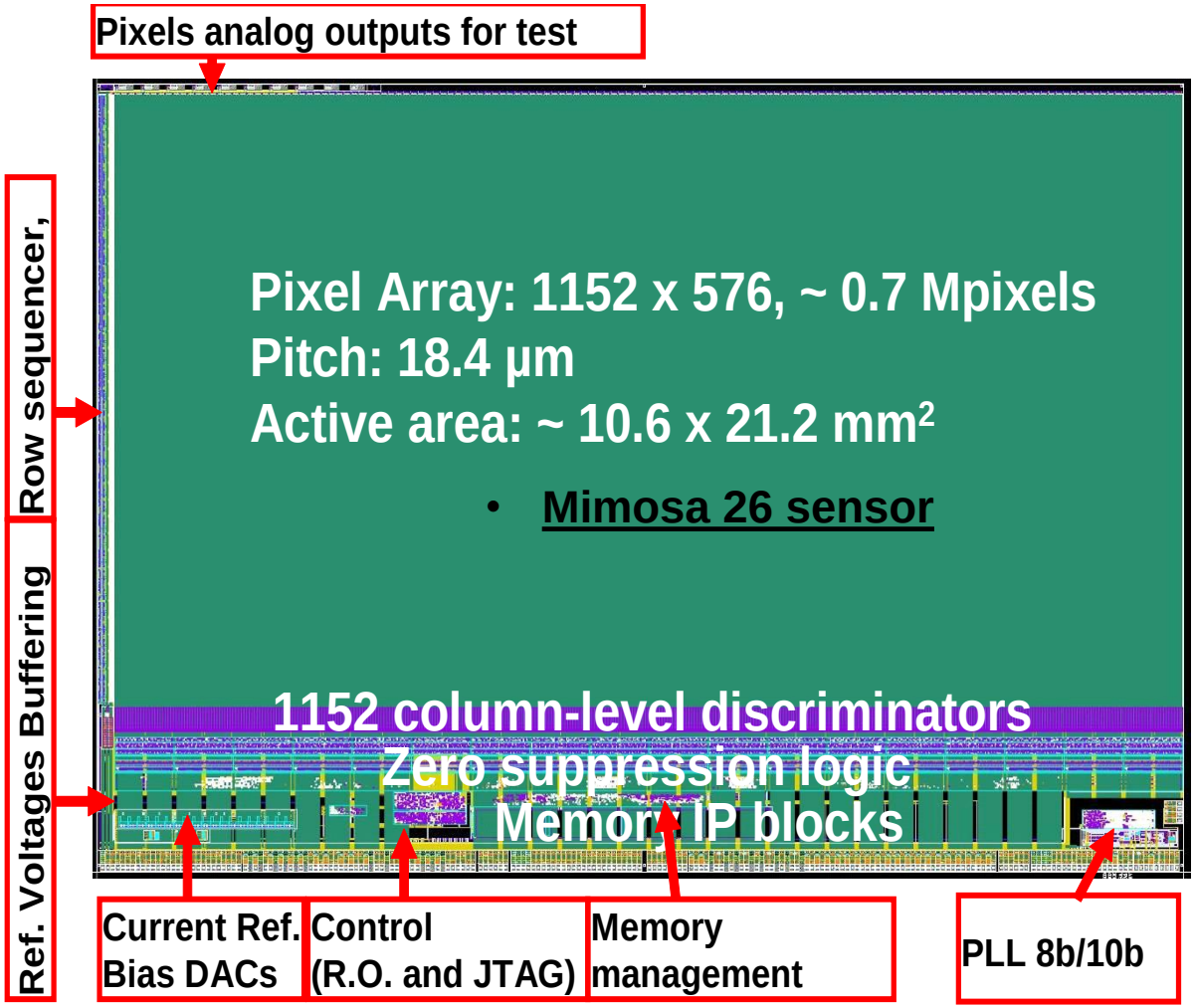


Photo imaged micro-vias
Std aluminum pads on chip (no post process)
Insensitive to bowing
50um micro-vias
Position of pad on the chip : anywhere
1 to 4 routing layers possible
No copper
Thinned chip only (50 to 100um)

Embedded Chip at CERN

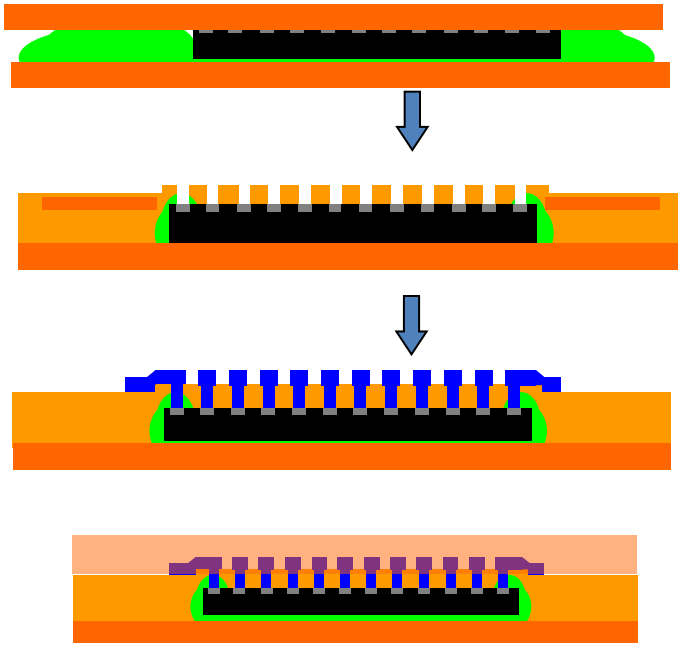


Bonding pads:
Shape : square 80um
Pitch : 100um
Position : periferical
Pad metal: Al

Chip thickness: 50um

Chip not flat

Embedding principle



• Gluing between two kapton foils

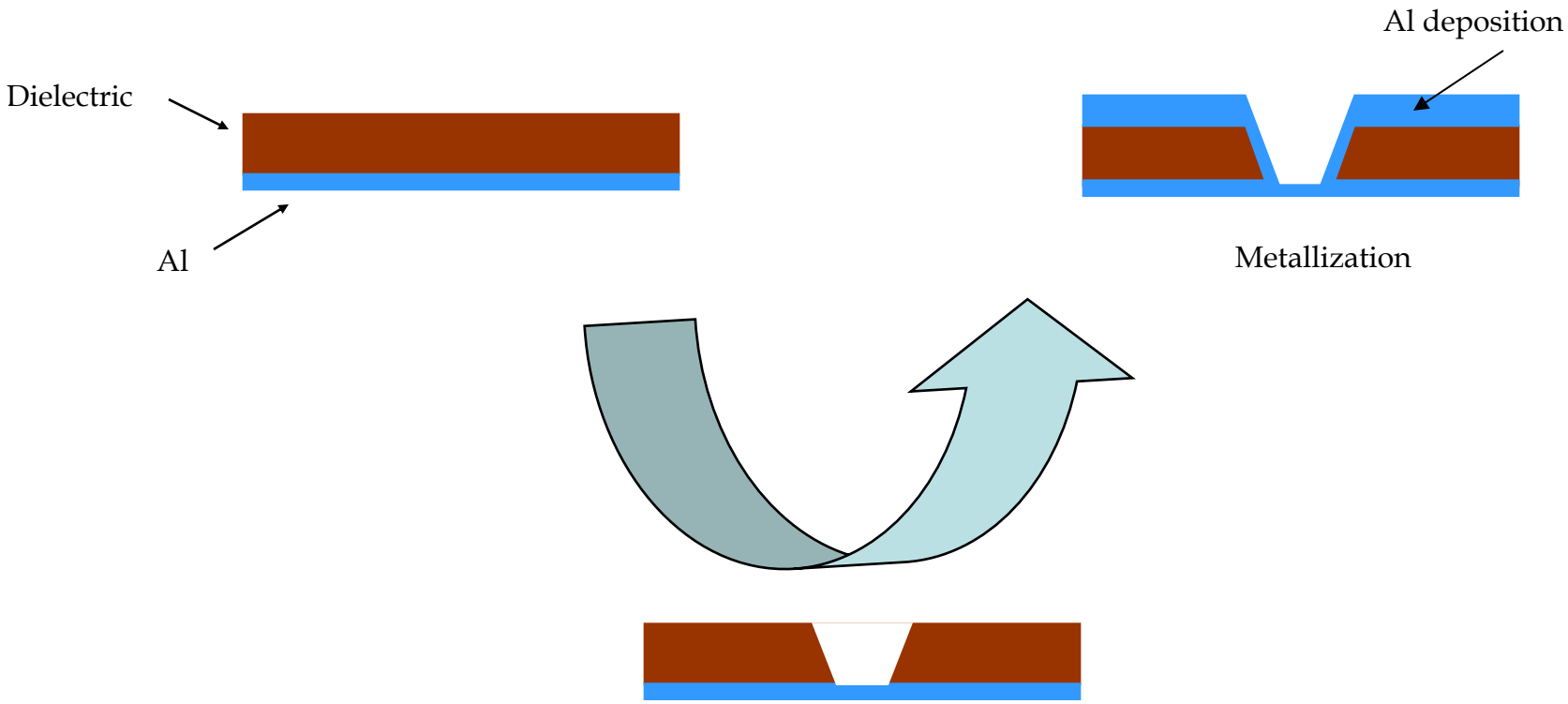
•_Opening vias using lithography

•_Metallization: Al (5-10 μm)

• Lithography to pattern metal

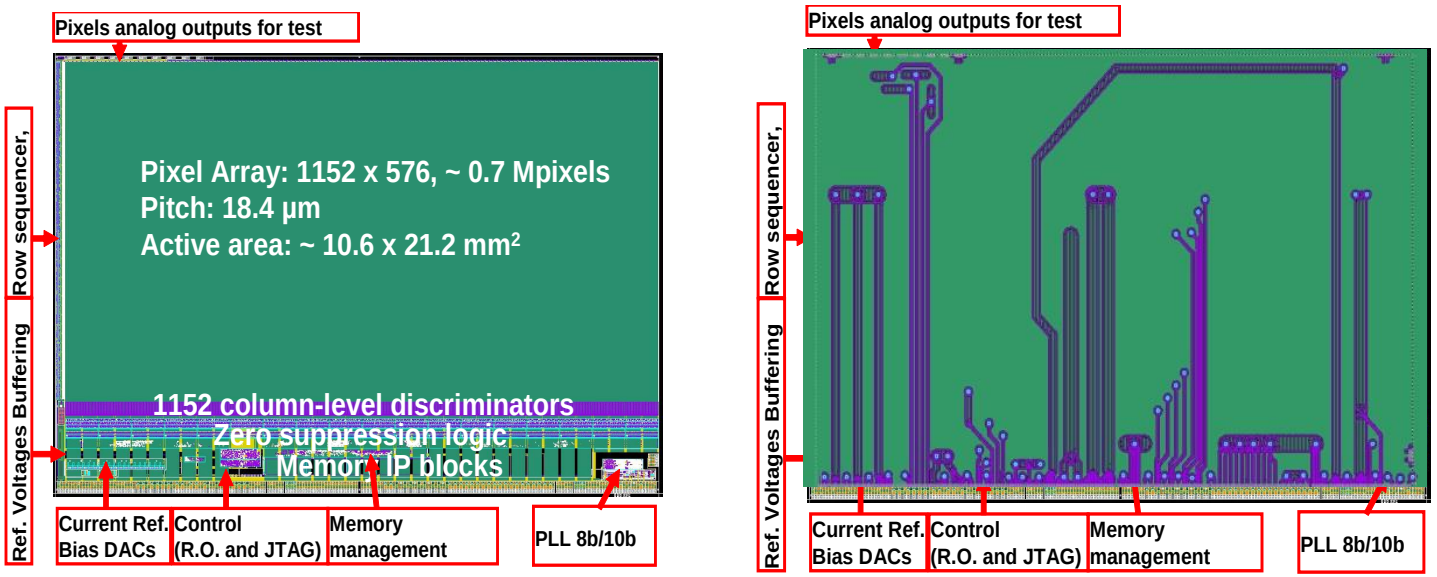
• Gluing of another kapton foil for deposition of second metal layer

Process with Photoimageable coverlay



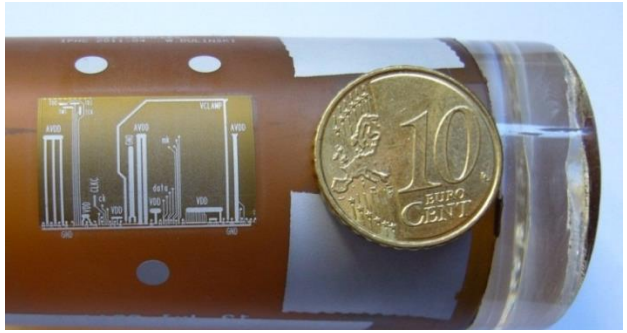
Minimum Via : 50um

Real example : First AL redistribution layer

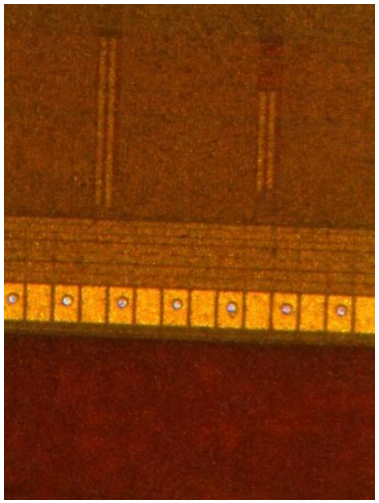


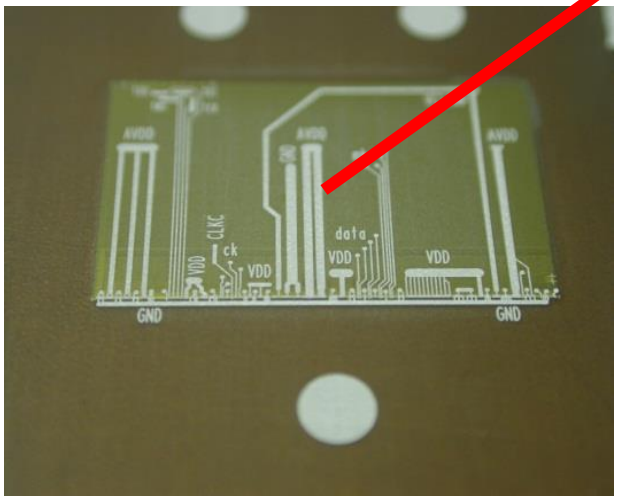
Redistribution layer
Make the connection between silicon world and PCB world
From 50um vias to 200um vias
10um vacuum deposited aluminium

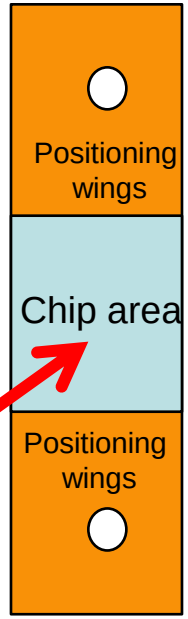
First redistribution layer



Solid state flexible sensor wrapped over cylindrical shape (R=20 mm)



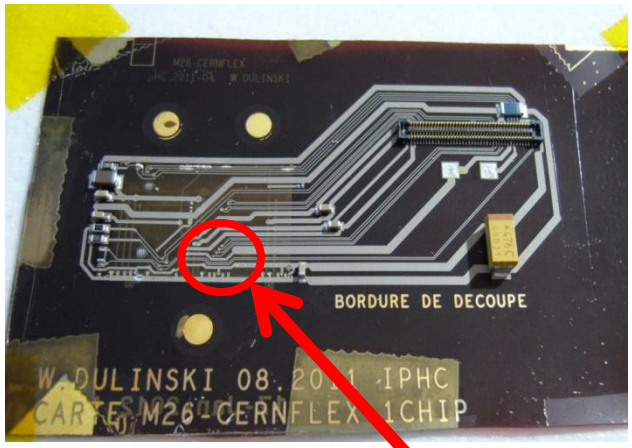


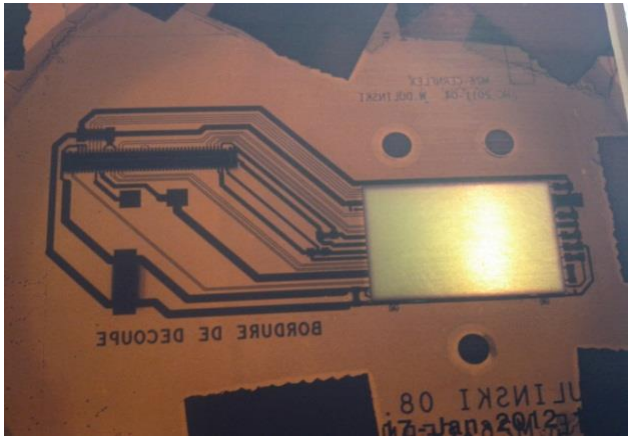


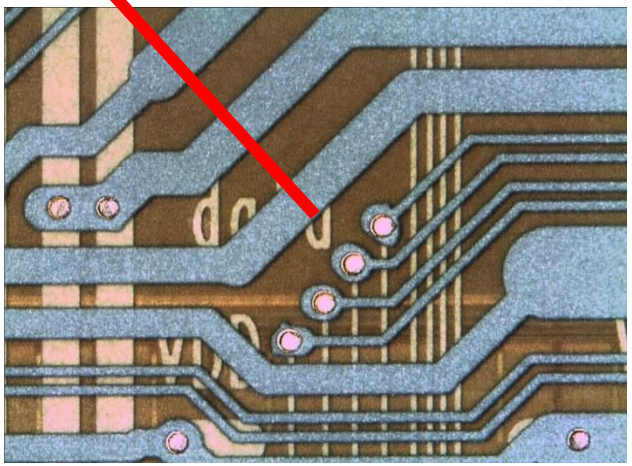
Laser flex cutting keeping positioning wings.

50um accuracy

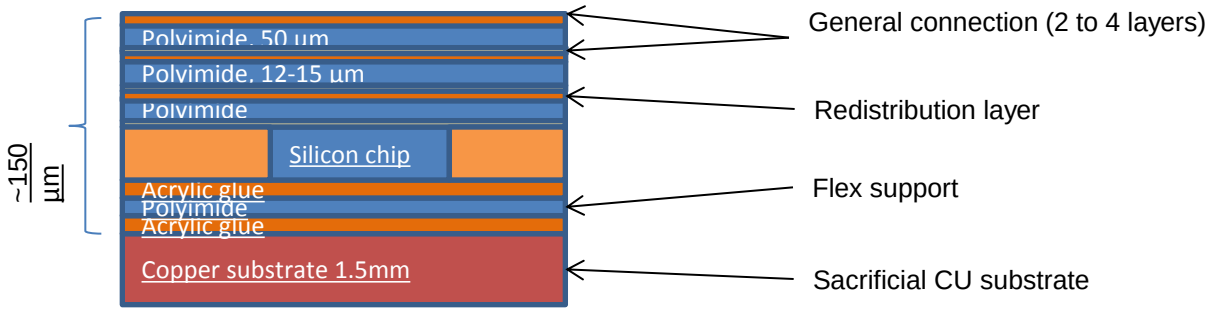
Second layer just for preliminary check

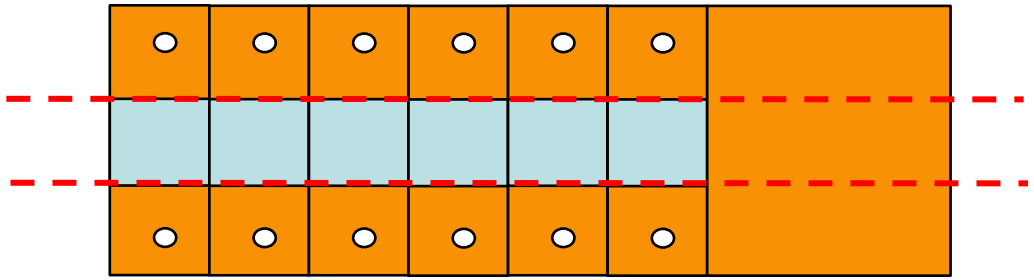






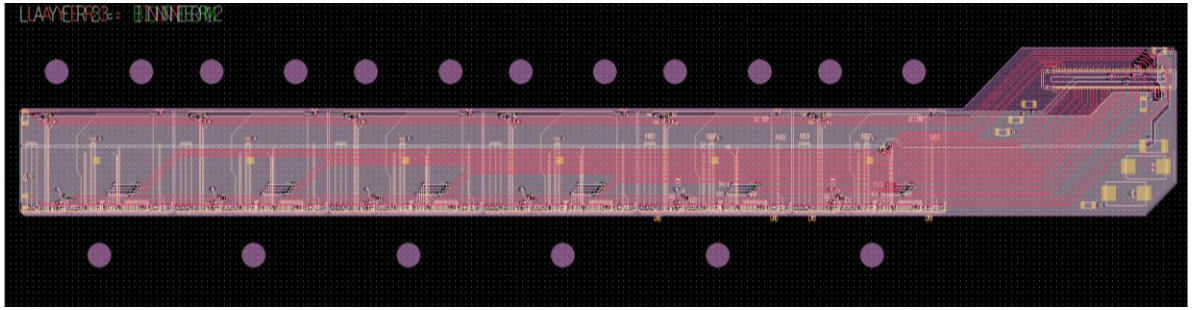
Multi chip embedding principle



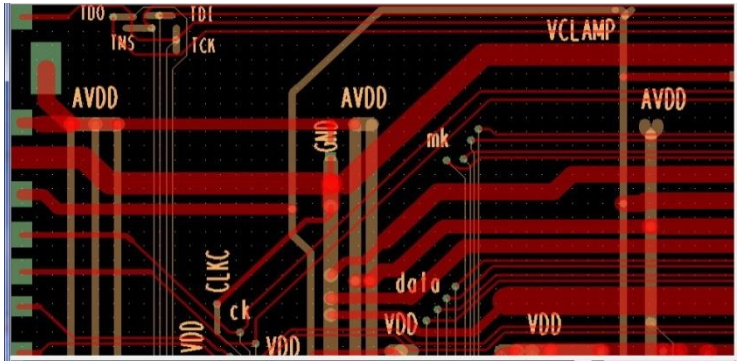


Redistribution layer is made on single chips

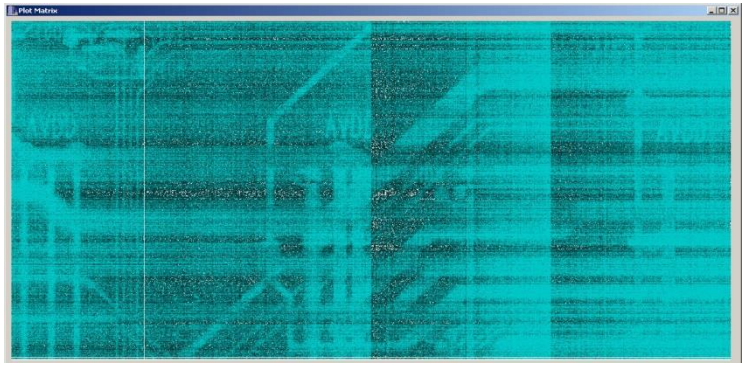
General connection are made on the full bus



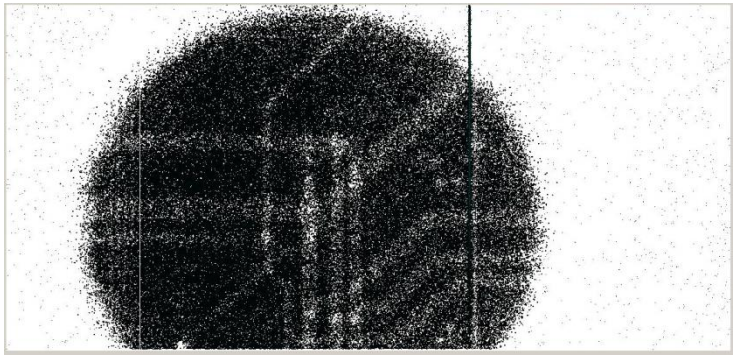
Results



Lithography details of interconnecting metal (two layers of ~10 µm thick Al) deposited on top of the pixel sensor



"Shadow" of metal measured by pixel sensor in visible light



Auto-radiography of metal measured by pixel sensor using 5.9 keV Xrays (^{55}Fe)

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NEW cooling structure details

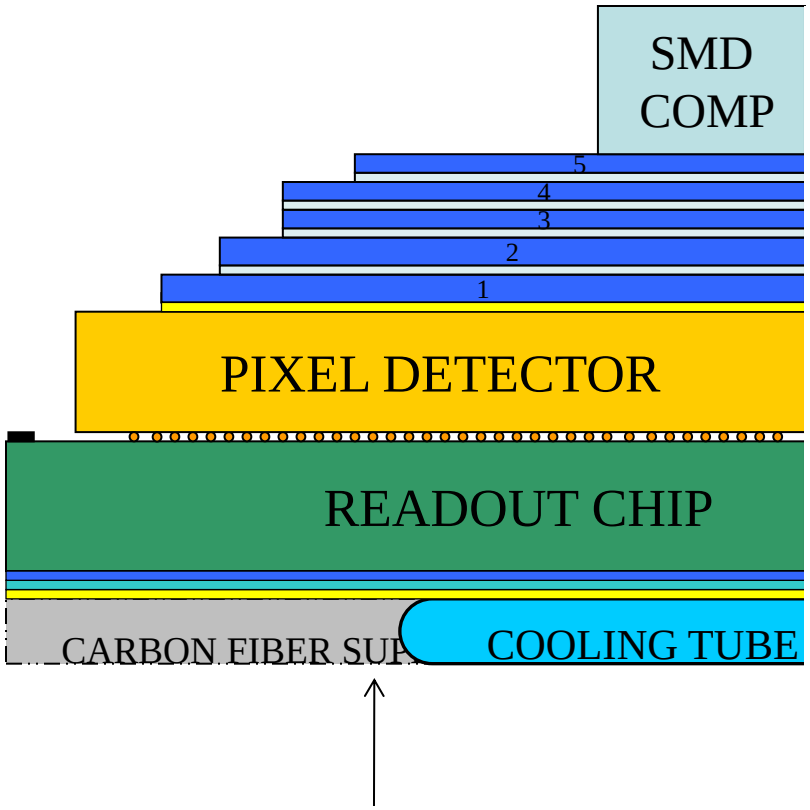
Photoimageable coverlay on Kapton

Coverlay paterning

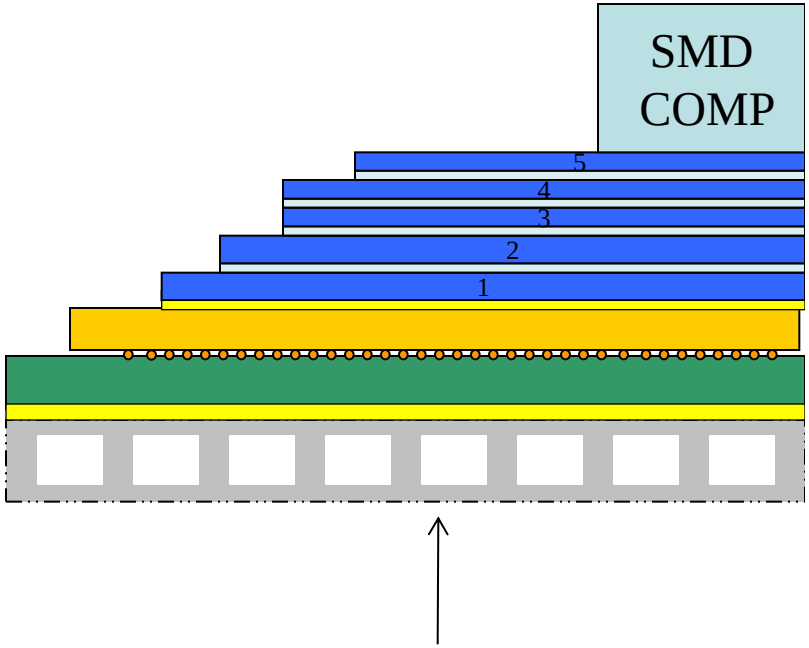
Kapton covering

Channels width from 0.1mm to 1mm
0.1mm to 0.5mm thick
Shape define by layout
Size up to 60cm x 50cm
Low cost

NEW possible cooling structure

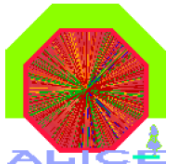


Existing structure



With new cooling structure

EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
European Laboratory for Particle Physics



Internal Note/
ALICE reference number
ALICE-INT-

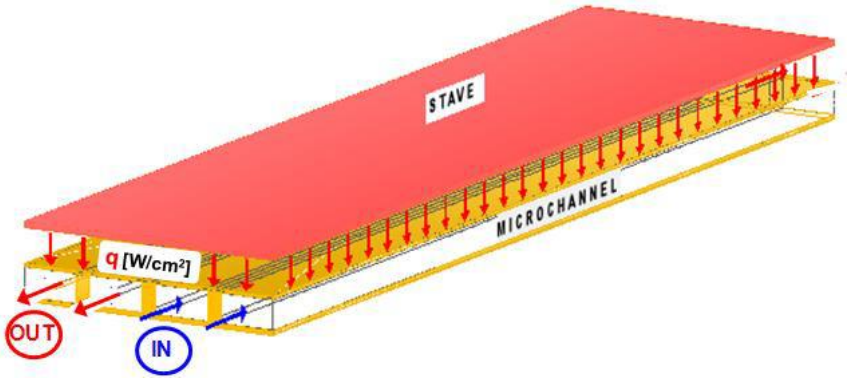
Date of last change

Development of polyimide microchannels for cooling the silicon detector modules of the ITS upgrade

Abstract

The aim of this document is to present the development of the polyimide micro scale system which is one of the three solutions under evaluation for cooling down the silicon detector of the ALICE-ITS upgrade. This system is based on the microchannels heat sink philosophy with channels imbedded in polyimide substrate. In single phase flow with water and perfluoroexane, it has been showing to be capable of maintaining the temperature sensors between 15°C and 30 °C with an heat dissipation ranging from 0.3 to 0.5 W/cm^2. Moreover thanks to its low mass it is able to guarantee a material budget of about 0.1% X_0.

In this study, the hydraulic and heat transfer performances have been investigated at different geometries both analytically and numerically. The mechanical behavior induced by the internal pressure coolant was also studied by finite element method. The first prototypes were fabricated and the preliminary mechanical and thermo fluid dynamic tests were carried out with successful.



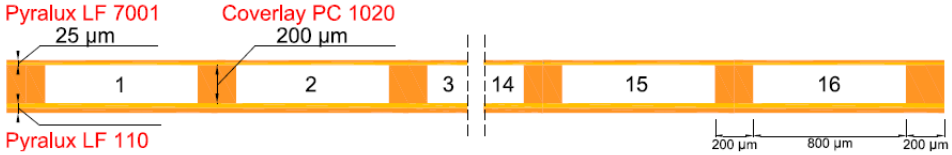


Figure 5: Schematic of the polyimide MCHS cross section.

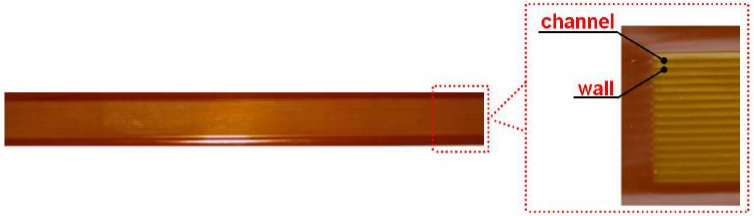
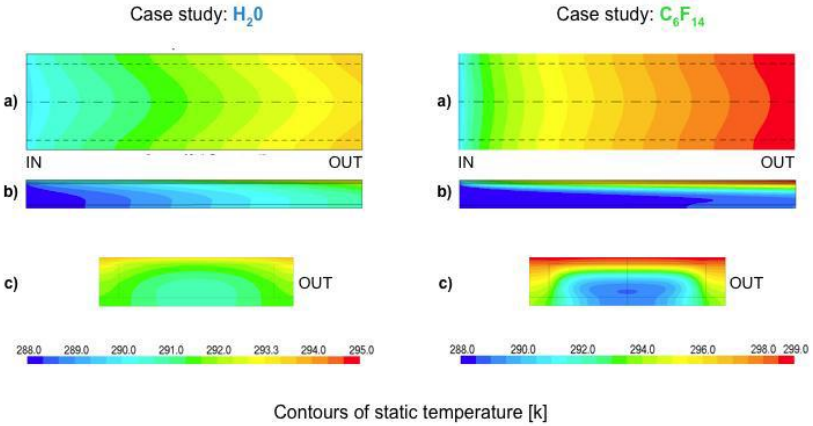


Figure 6: Picture of a polyimide MCHS prototype: 16 channels 800 x 200µm with 15 channel wall 200µm tick .

Fig. 15: a) Coolant temperature at inlet and outlet of MCHS for different levels of heating power. b) Sensor temperature vs. position on the heater upper surface for different levels of heating power.



Coolant	Power [W/cm²]	$T_{COOLANT}$ OUT [°C]	Heated surface T_{MIN} [°C]	Heated surface T_{MAX} [°C]	Flow rate [l/h] 1 channel	Flow rate [l/h] 16 channel	ΔP [bar]
H_2O	0.5	18.1	16.7	20.6	0.28	4.6	0.35
	0.4	17.5	16.2	19.4	0.28	4.6	0.35
	0.3	16.9	15.9	18.2	0.28	4.6	0.35
	0.3	18.2	15.9	19.7	0.2	2.8	0.2
C_6F_{14}	0.5	18.2	17.2	26	0.7	11.2	0.6
	0.3	17.0	16.0	21.6	0.7	11.2	0.6

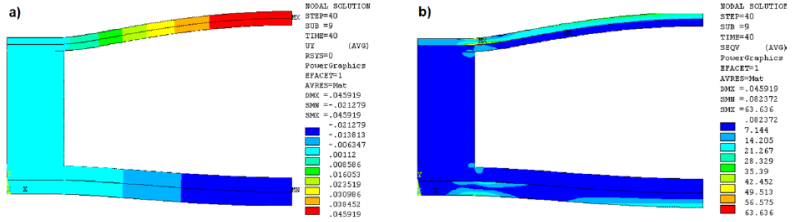


Figure 10: FEA results @ 2bar relative coolant pressure: a) vertical deformation [mm], b) Von Mises Stress distribution [Mpascal].

Future

- Dedicate some equipment's for AL processes to reduce production time and costs.
- Build a 2 chip Embedded structure and then probably 6 chip.
- Continue characterization of Cooling device for Alice project.