CERN PH-ESE Electronics Seminar

Time to Digital Converters and results from a new 5ps TDC prototype ASIC

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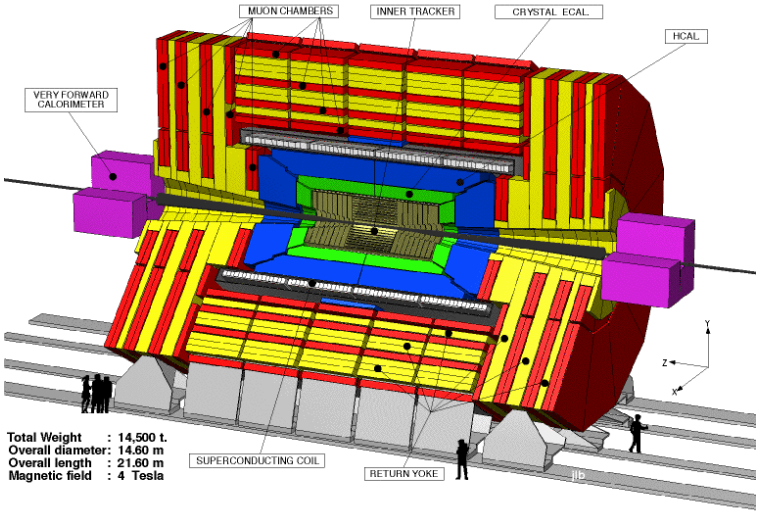
Outline

- **Time measurements in HEP**
- **Time-to-Digital Converter Concepts**
- **Challenges in Fine-Time Resolution TDC Design**
- **Demonstrator Architecture**
- **Measurement Results**
- **Conclusion**

Time-to-Digital Converters in HEP

Large systems with many channels (100k or more)

- Electronics distributed over larger area
- Time resolution and stability across whole system
  Distribution of common time reference to all the channels
- Detector time resolution sets requirements for TDC



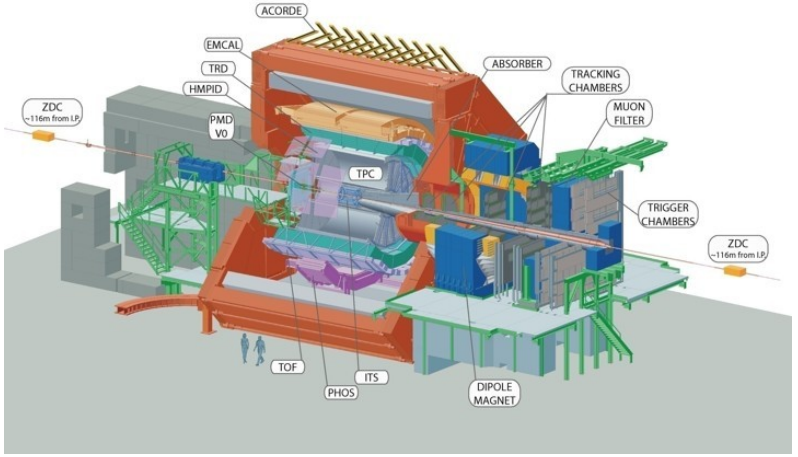
CMS

Drift time in gas based tracking detectors

- Low resolution: ~1ns
- Examples: CMS and ATLAS muon detectors

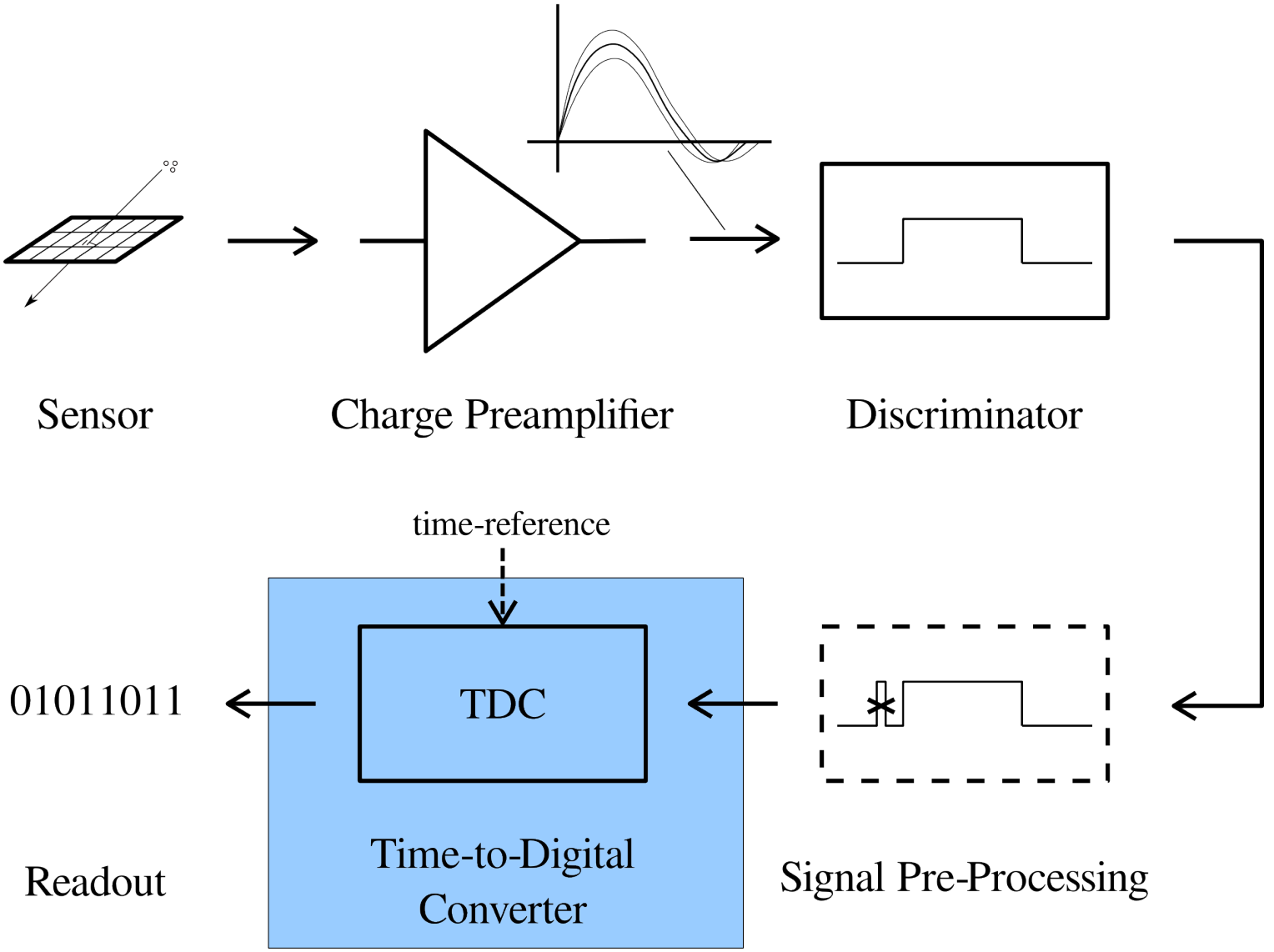
Time of flight detectors

- High resolution: 10ps – 100ps
- Example: ALICE TOF



ALICE

Time Measurement Chain



Special needs for high energy physics

Other Applications

- **Frequency synthesizer (All Digital PLLs)**
- **Laser Ranging and Radar Applications (distance measurement ...)**
- **On-Chip Instrumentation (Jitter ...)**
- **Imaging Systems (Positron Emission Tomography, Time Correlated Single Photon Counting ...)**
- **...**

In HEP often have different needs

- **hundred / thousands of channels**
- **often single shot time precision**
- **distributed large systems (common time reference)**
- **high dynamic range (25 ns)**
- **hit rates (kHz - Mhz)**
- **...**

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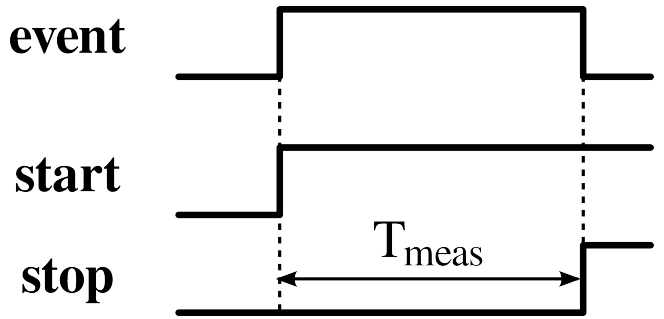
Time Measurements

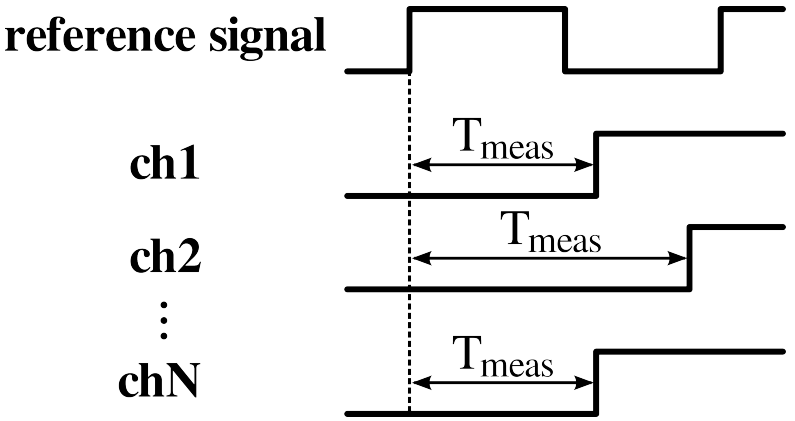
Start - Stop Measurement

- Used for measuring time interval between two local events
- No absolute time measurements possible
- Often used for small local systems and for low power applications

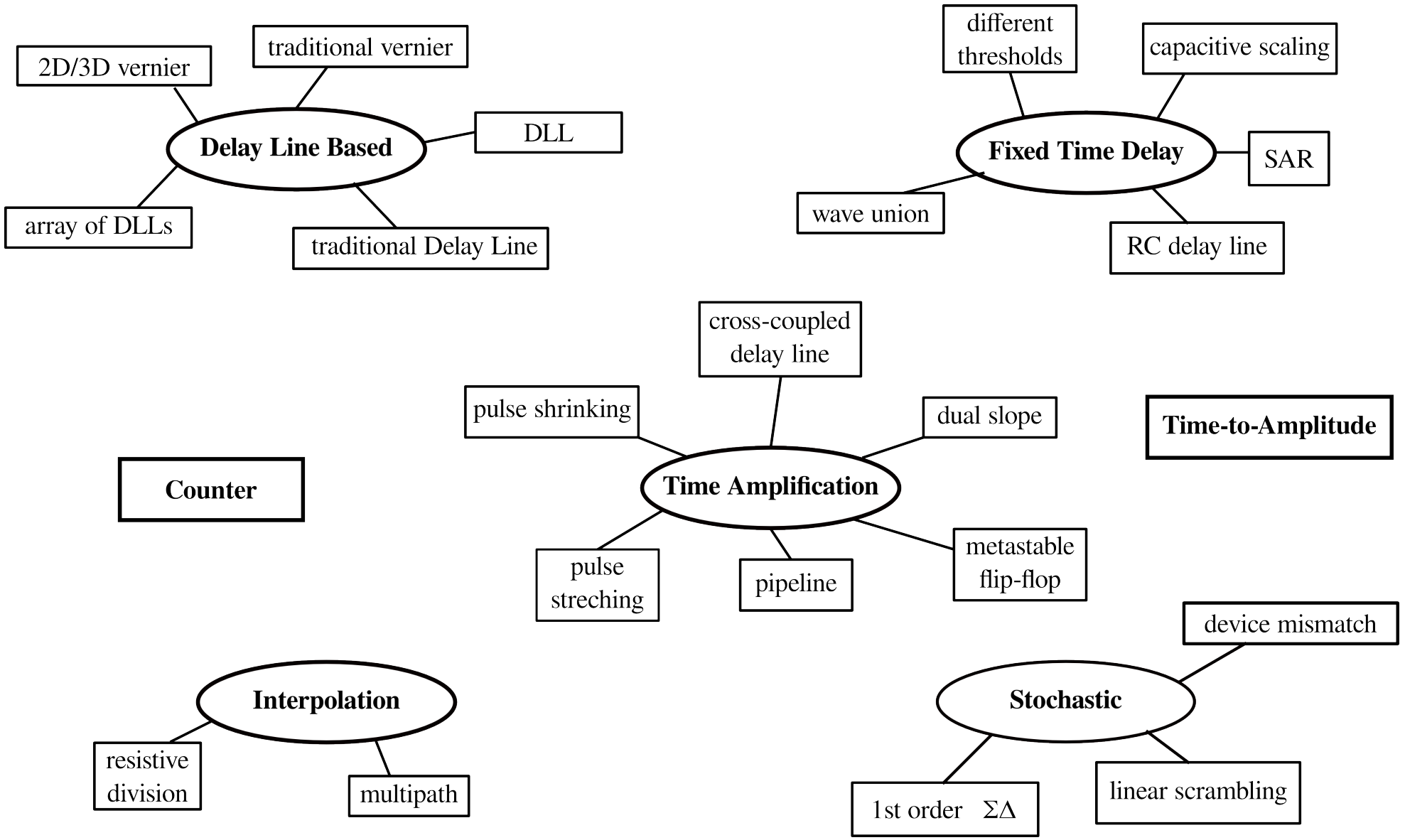


Time Tagging

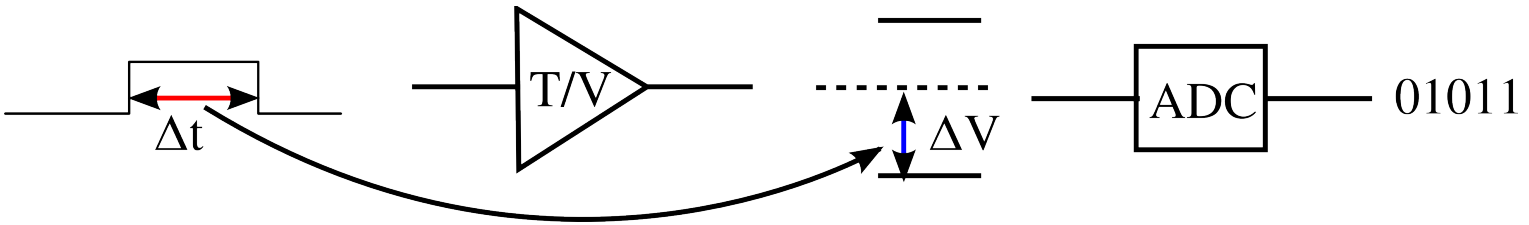
- Used for measuring the time of an event relative to a time reference (e.g. clock)
- Absolute time measurements possible
- For large scale systems with many channels all synchronized to the same reference



TDC Architectures

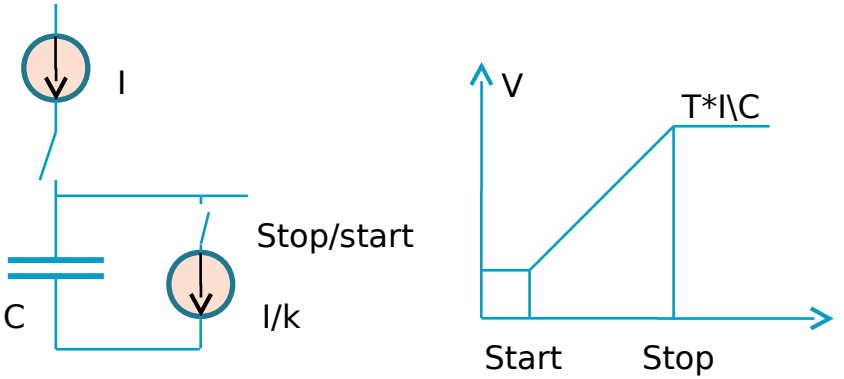


Time to Amplitude

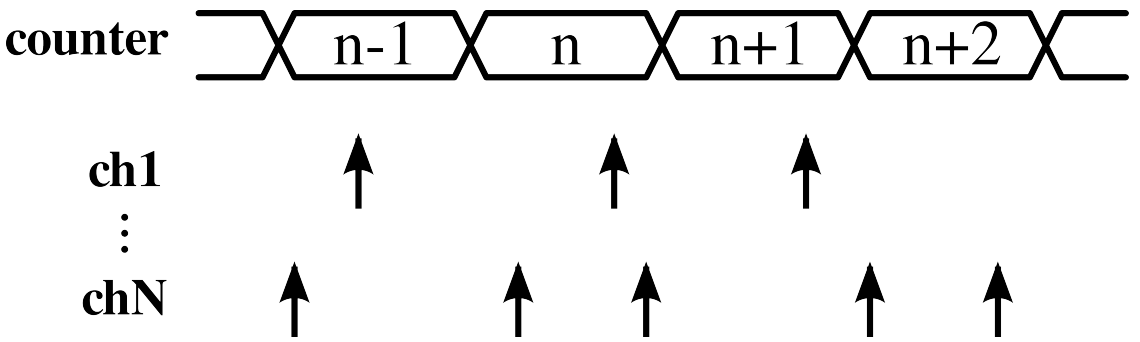


- convert time difference into voltage domain
- resolution defined by T/V-converter and ADC
- move complexity to ADC domain

T/V converter



Counter Principle



- on arrival of hit, store counter state
- hit can arrive at switching point of counter
  -> synchronize hit to counter / use gray counter
- timing precision limited by clock period = LSB

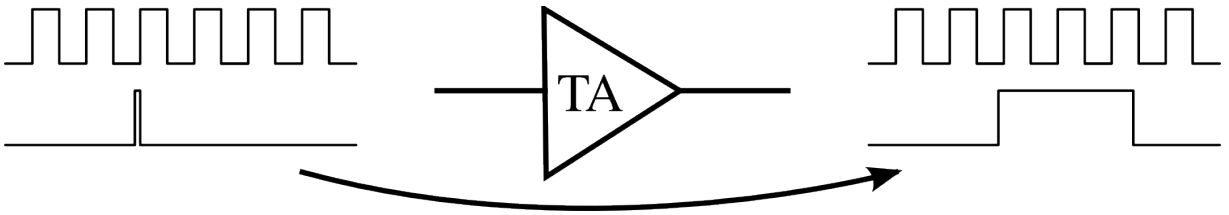
quantization noise

for uniformly distributed hits:

$$\sigma_{TDC} = \frac{LSB}{\sqrt{12}}$$

e.g. 1 GHz counter
-> 1ns LSB
-> ~ 300 ps-rms

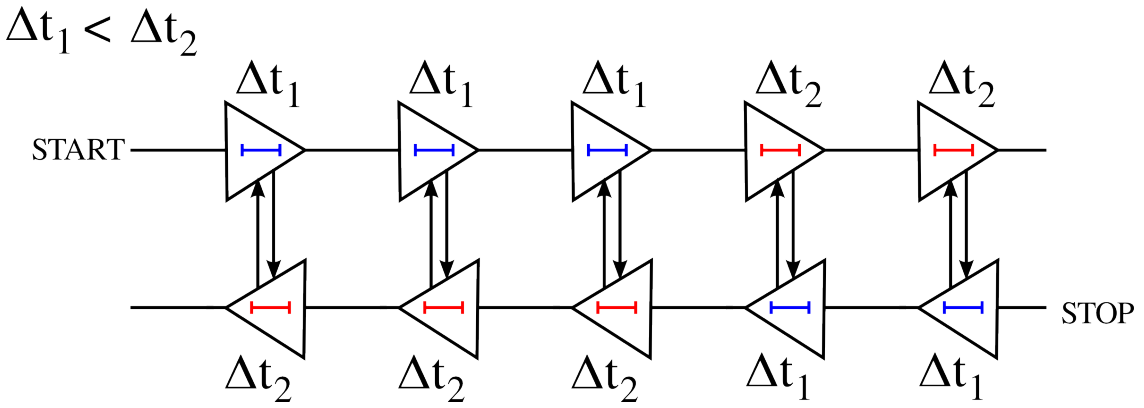
Time Amplification



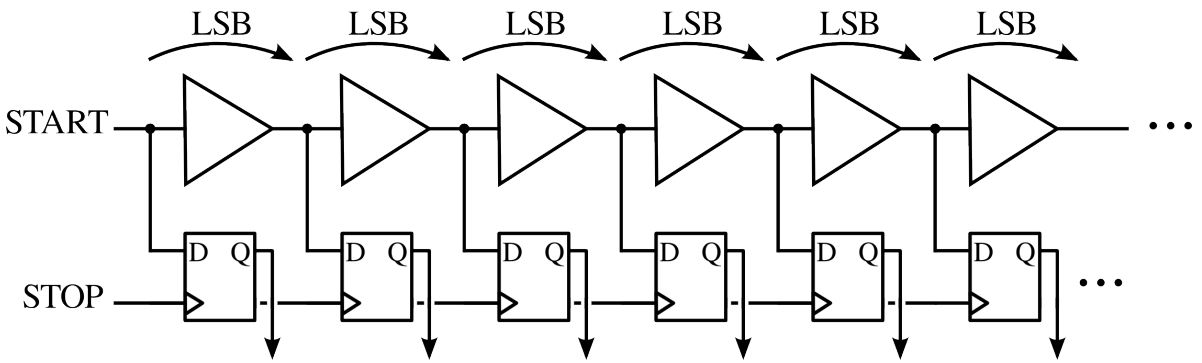
- Amplify time difference
  -> relaxed second stage TDC (e.g. counter)
- Precision of TA defines resolution
- Dead-Time

TA concepts

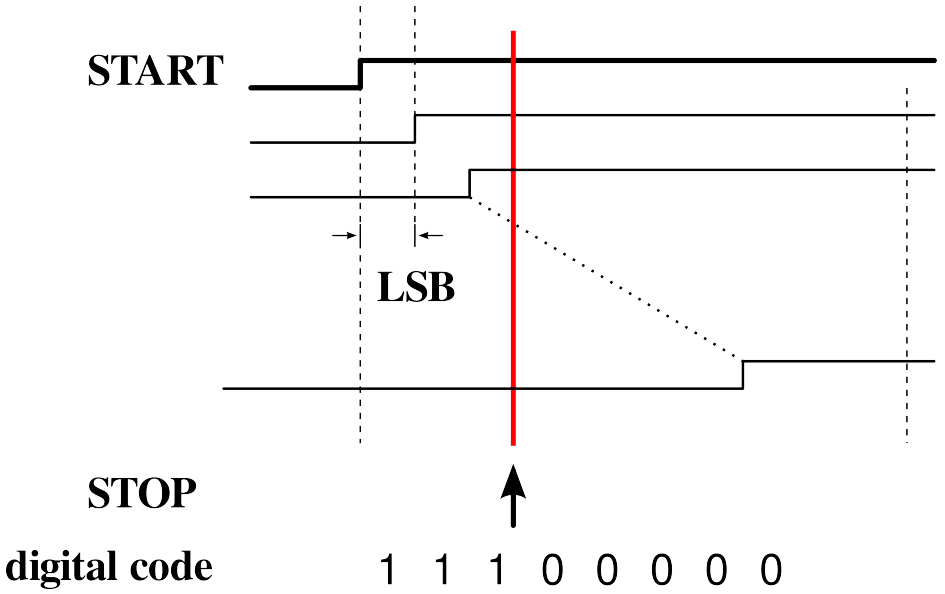
- Dual-slope
- Metastable FF
- Cross-coupled delay line
- Pulse stretching



Delay Line Principle

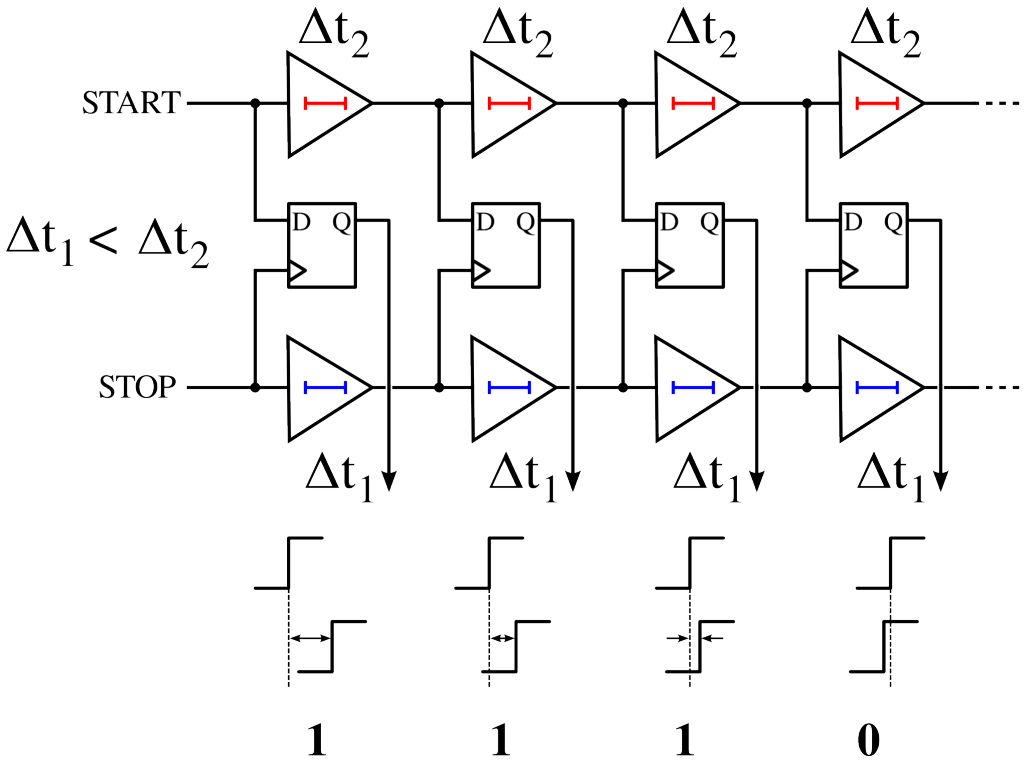


- generate set of delayed signals
- on hit store the state of delay-line
- LSB size limited by the gate-delay of the technology



e.g. 90/130 nm
-> LSB = 15 - 20 ps

Vernier Delay Line

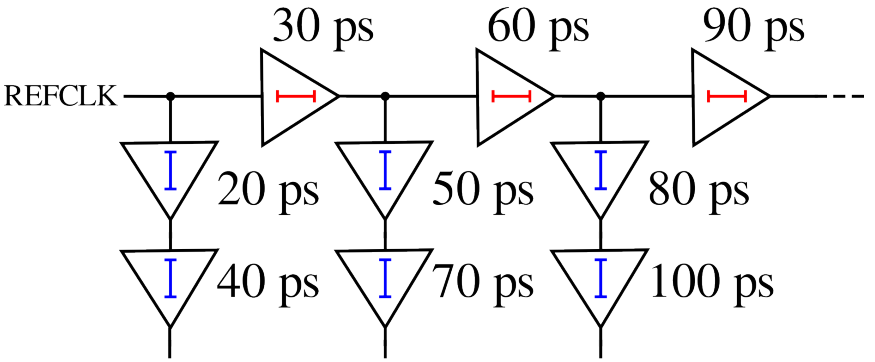


- LSB defined by delay difference
- Reduce relative delay between signals in each stage
- Long propagation delays on both paths

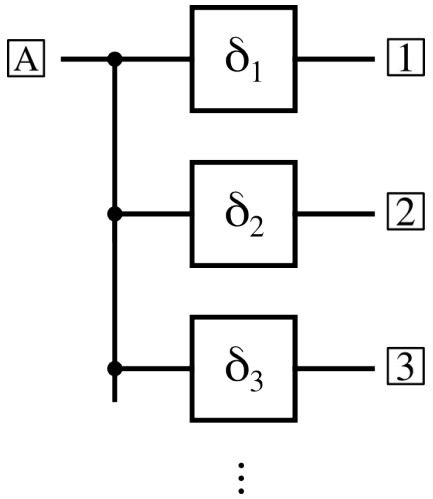
TA concepts

- 2D Vernier Line
- 3D Vernier Line
- Array of DLLs
- ...

Array of DLLs



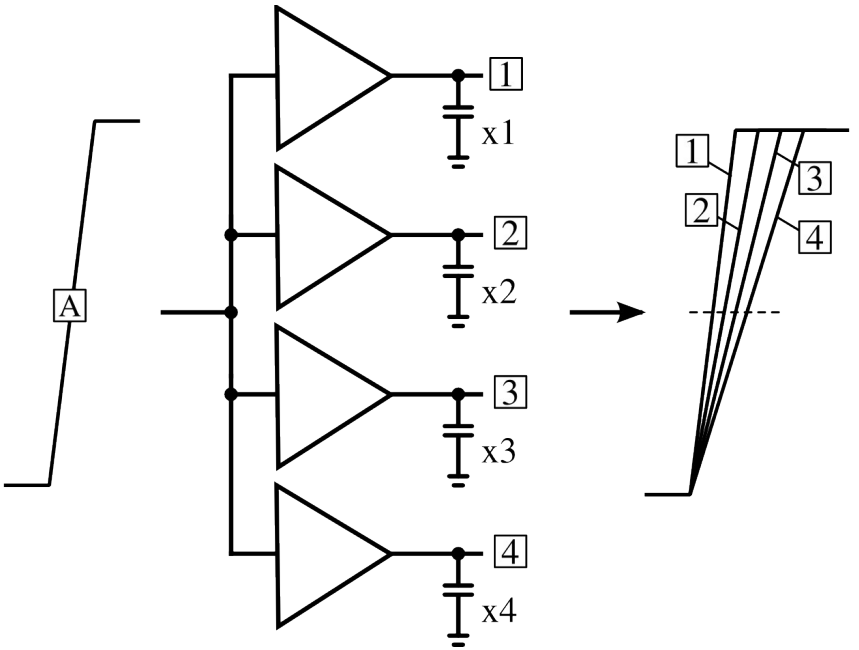
Fixed Time Delay



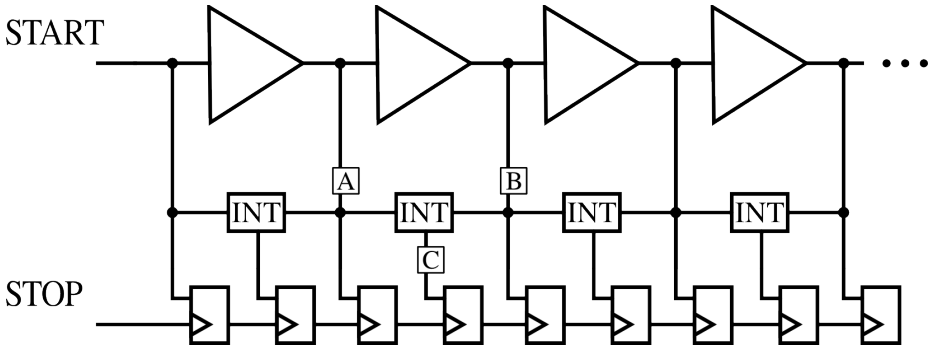
- Change signal propagation delay relative to each other
- constant delay

Fixed time delay concepts

- Capacitive scaling
- Different thresholds
- Wire Delay / RC - delay
- Buffer scaling
- SAR
- ...



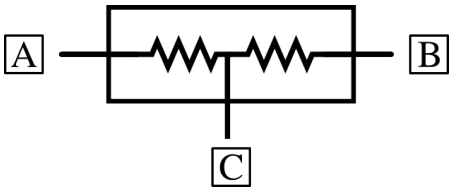
Interpolation

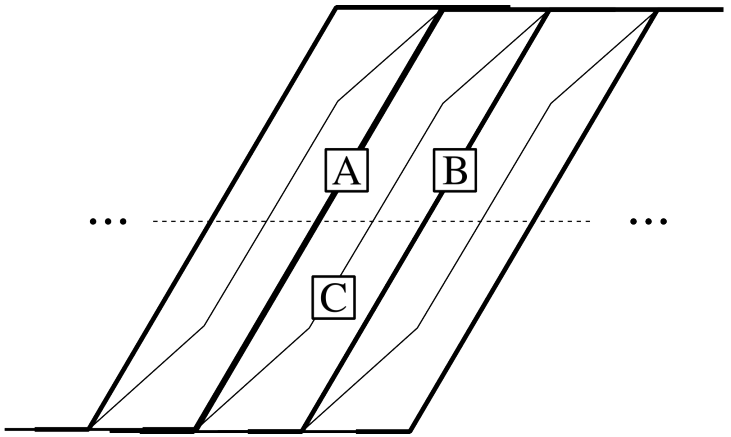


- Intermediate signals generated out of two time delayed signals
- Allows generation of sub gate delay LSB sizes
- Signal edges need to be overlapping

Interpolation concepts

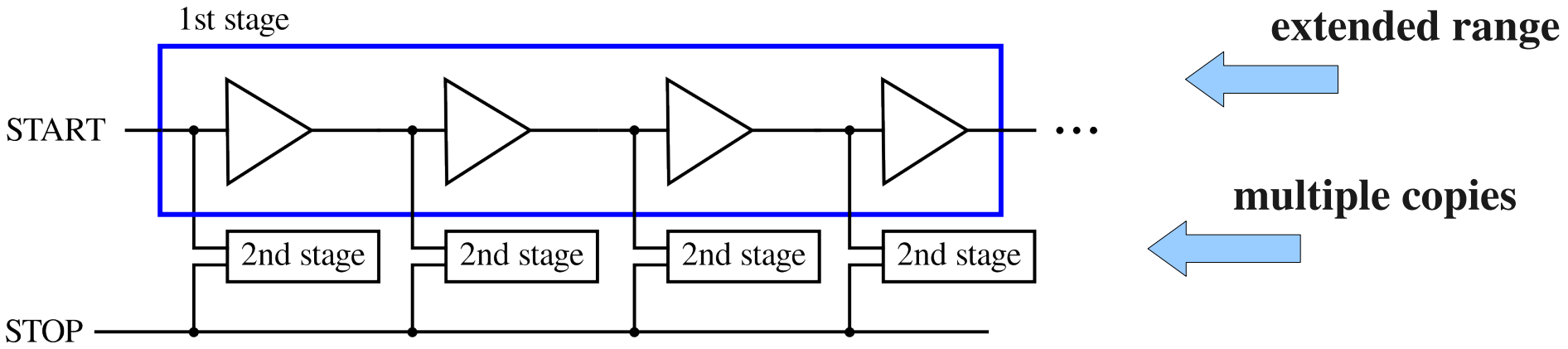
- Resistive Division
- Multipath Buffers
- ...





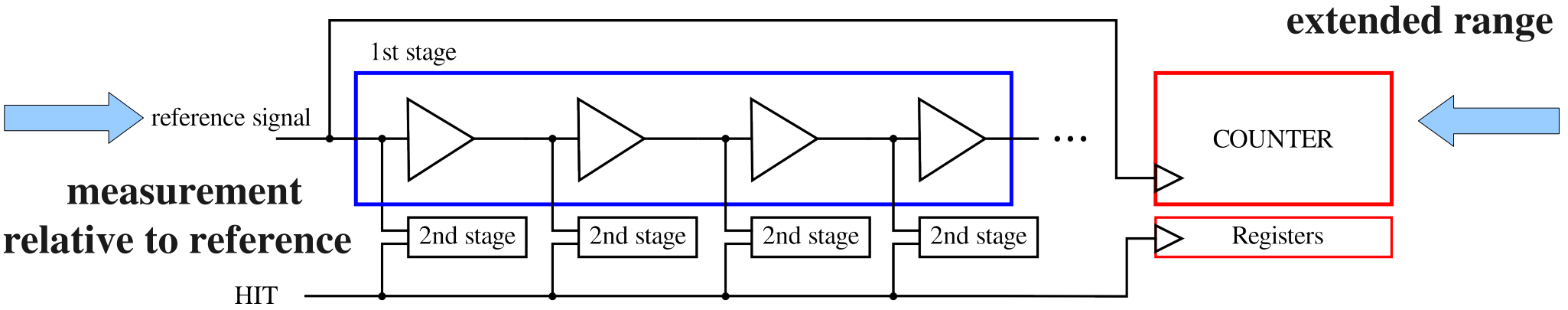
Multistage Approach

trade off: dynamic range vs. resolution
-> multistage approach



- high resolution 2nd stage w/ small dynamic range
- multiple copies to increase dynamic range
- dynamic range of 2nd stage fits dynamic range of one bin of 1st stage
- long delay lines for large dynamic ranges

Counter Extension

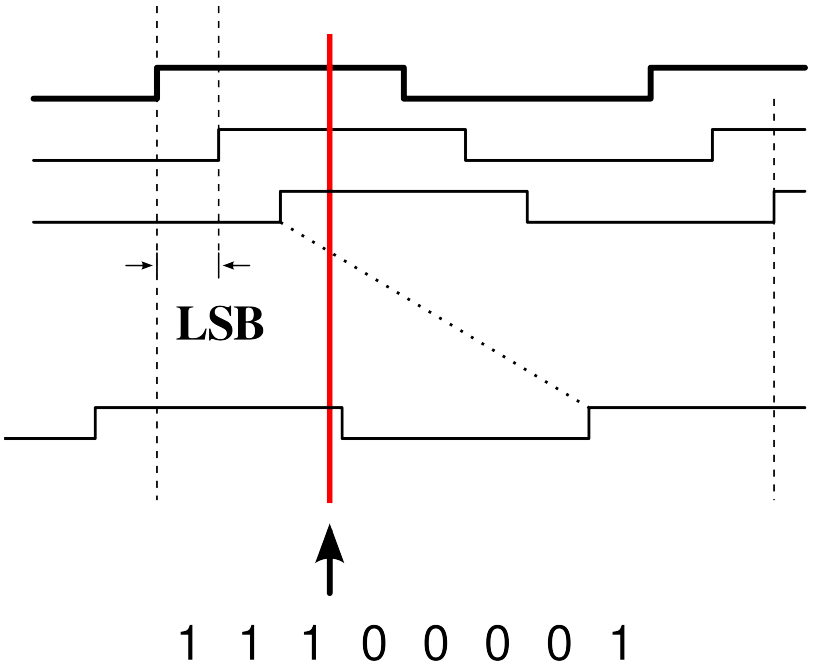


relate measurement to reference signal

- delay needs to fit one reference clock cycle
- analog / digital control

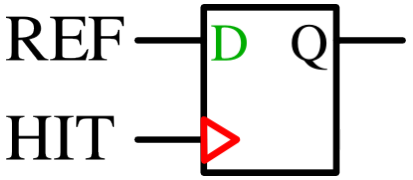
counter metastability

- hit is an asynchronous event
- double counter / gray & additional bit



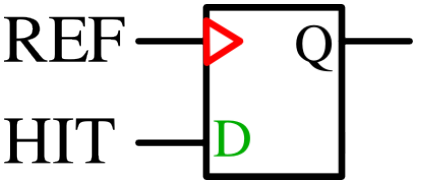
Event vs. Data Driven Architecture

Event Driven



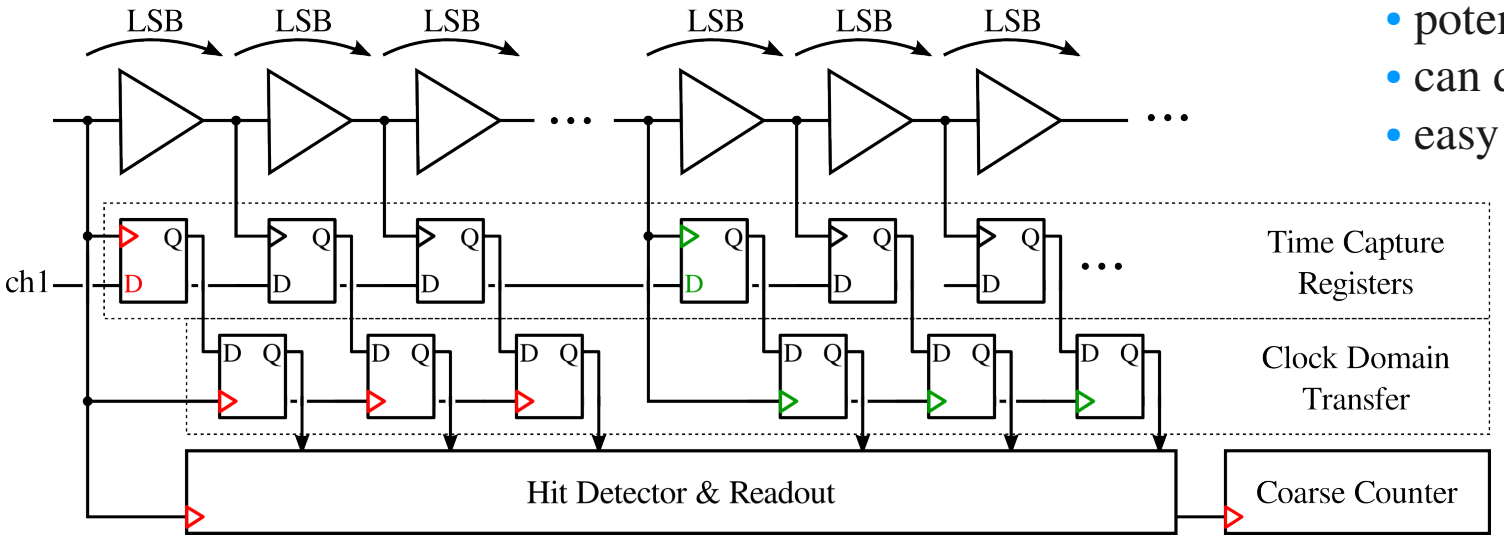
- sample state of reference signal

Data Driven



- sample state of HIT signals

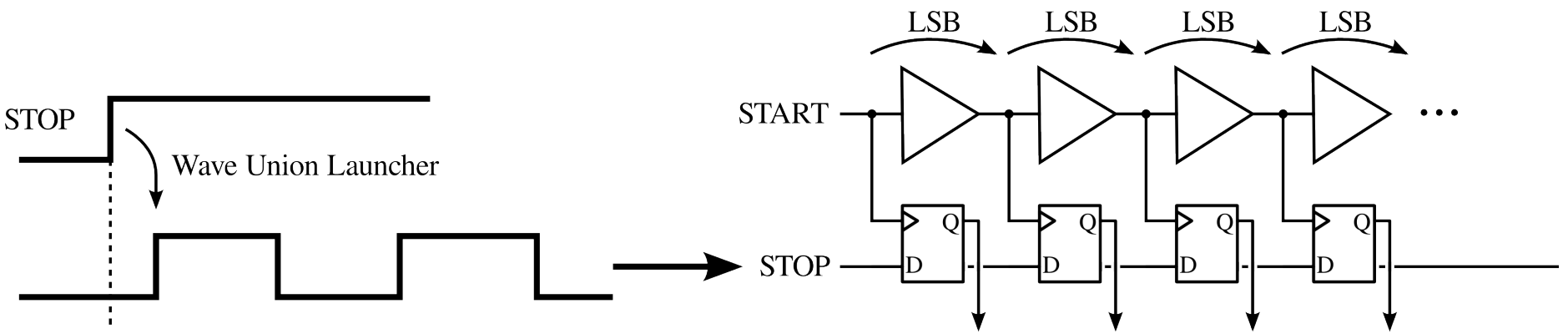
Data Driven Example

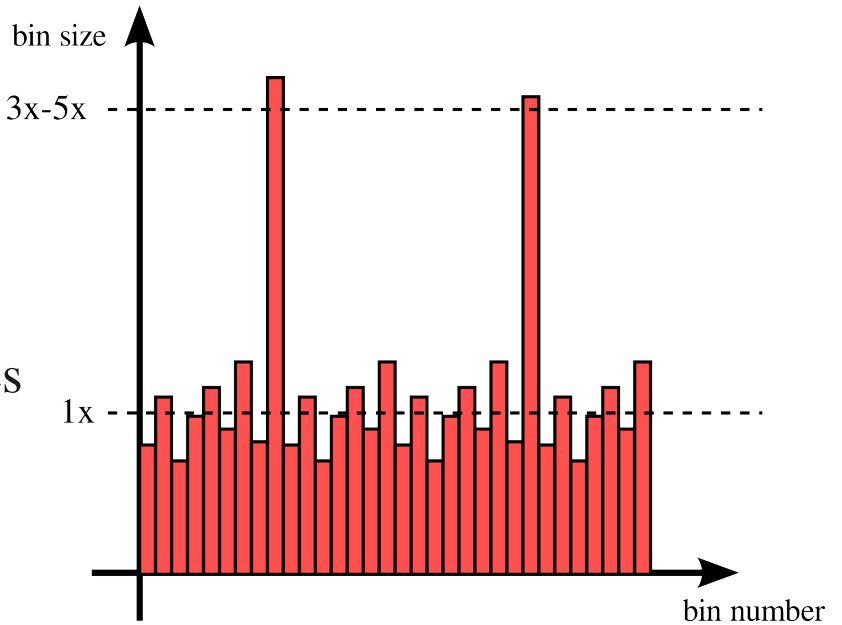


- potentially no dead-time
- can detect multiple transitions
- easy counter synchronization

- constant data flow
- clock domain transfer
- higher power consumption (3x registers)

Wave Union TDC





- multiple measurements on single channel
- need to sample the HIT (data driven structure)
- often used in FPGAs to overcome large bin sizes

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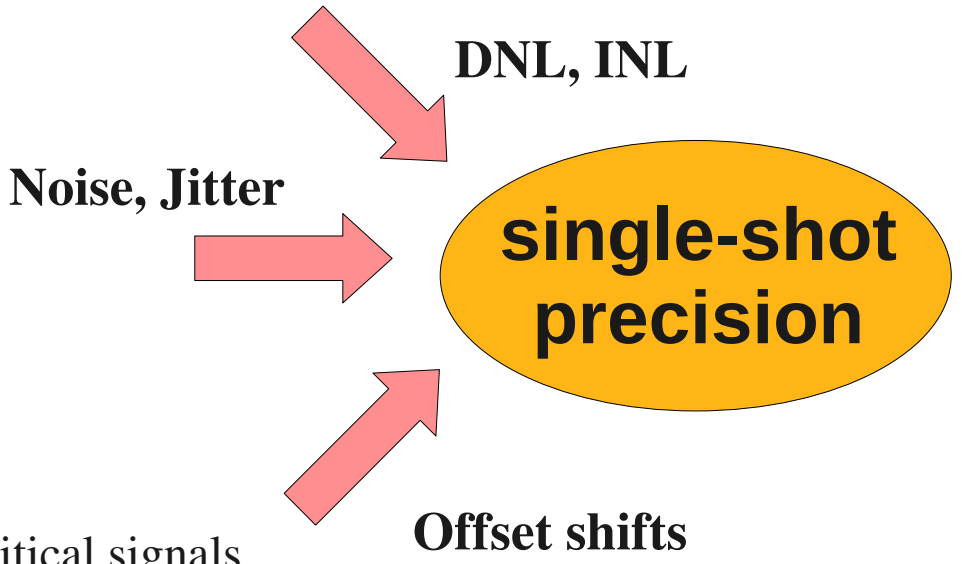
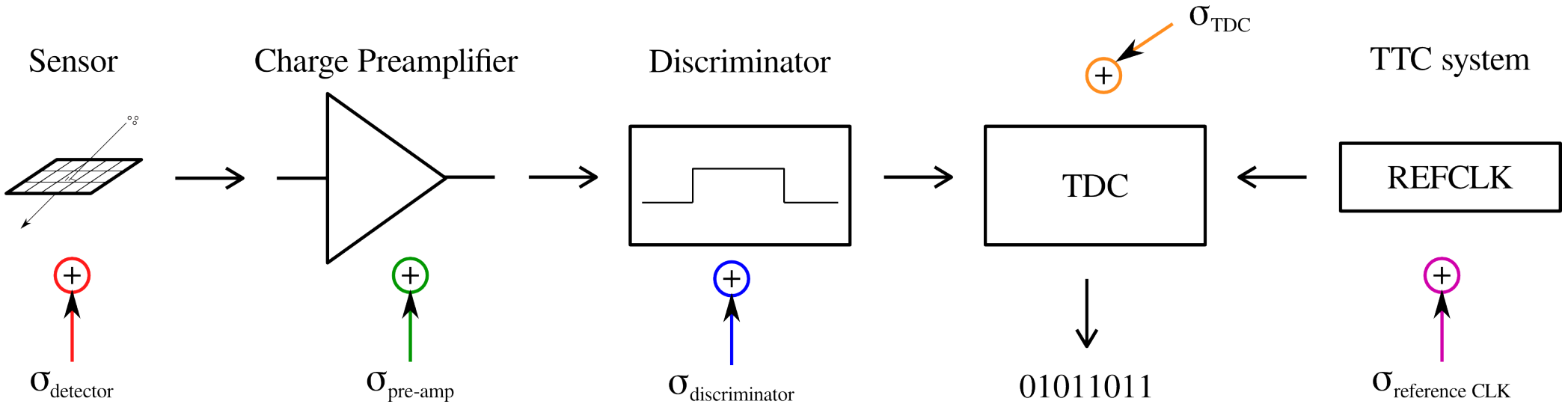
Difficulties in ps range resolution

LSB/sqrt(12) ≠ rms

- In sub-ps resolutions device mismatches can become dominant
  - -> careful simulation & dimensioning during design time
  - -> can have major impact on design
- Power supply noise
  - -> short delays, fast edges
  - -> separate power domains
  - -> substrate isolation
  - -> clean PCB layout
- Distribution of signals get critical
  - -> RC delay of wires
  - -> balanced distribution of timing critical signals
- Process-Voltage-Temperature variations
  - -> LSB auto calibration to compensate for slow VT variations
  - -> global offset calibration still required



System Level

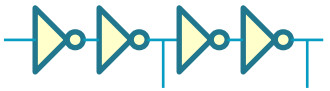


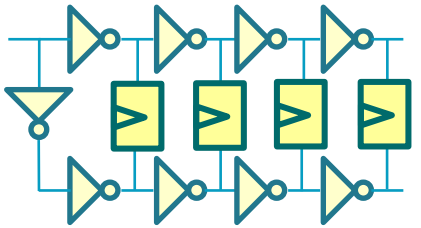
Complete Measurement Chain

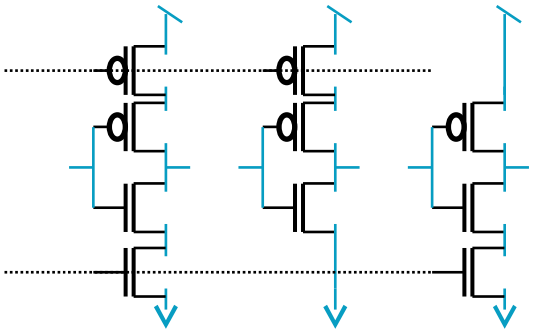
- Detector Noise
- Analog Front End
- Time Walk Correction
- Time Reference Noise
- TDC Noise
- Inter-channel Crosstalk
- PVT variation ...

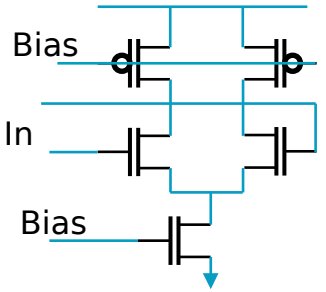
Delay Element

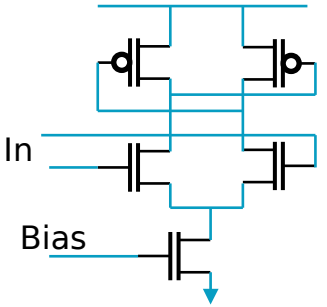
- **Critical building block - often longest delay path / used in many architectures**
  - CMOS inverter
    - double inverter
    - pseudo differential
  - Current starved / Voltage Controlled
    - large propagation delay variations
    - slower cell due to control
    - NMOS / PMOS
  - Fully Differential
    - short propagation delay w/ control
    - more robust against power supply noise (depends on design)
    - cross-coupled load / low power











For fine-time TDC designs:

Fast = Short Propagation Delays = More robust design

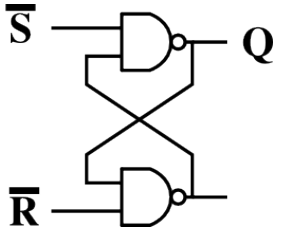
Time Capture Registers

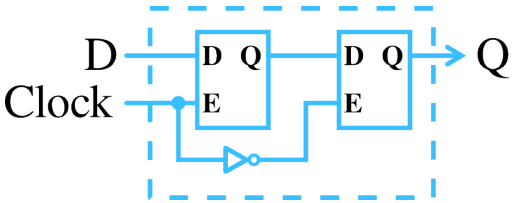
- **Critical building block - makes timing decision**

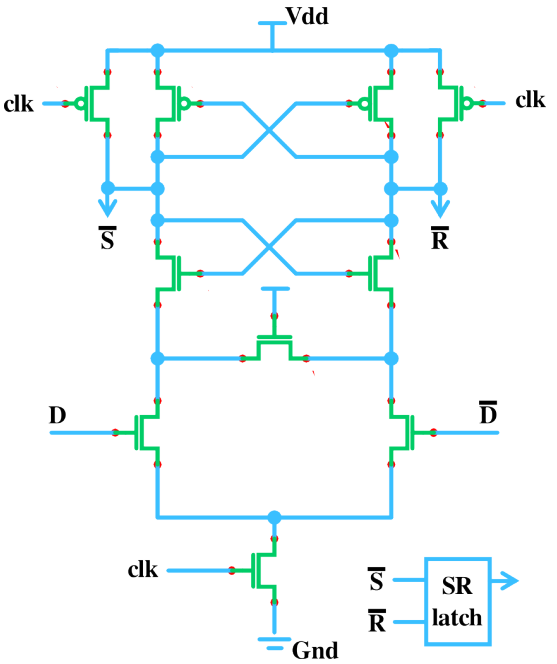
  - Latch
    simple / small area
    timing information can be overwritten

  - Standard D Flip-Flop
    hit independent readout out
    single-ended

  - Fully Differential Flip-Flop
    static current consumption
    fully differential input
    no conversion if differential signaling







sense-amplifier FF

For fine-time TDC designs:

Fine resolution = good matching / high power
OR
Fine resolution = FF calibration

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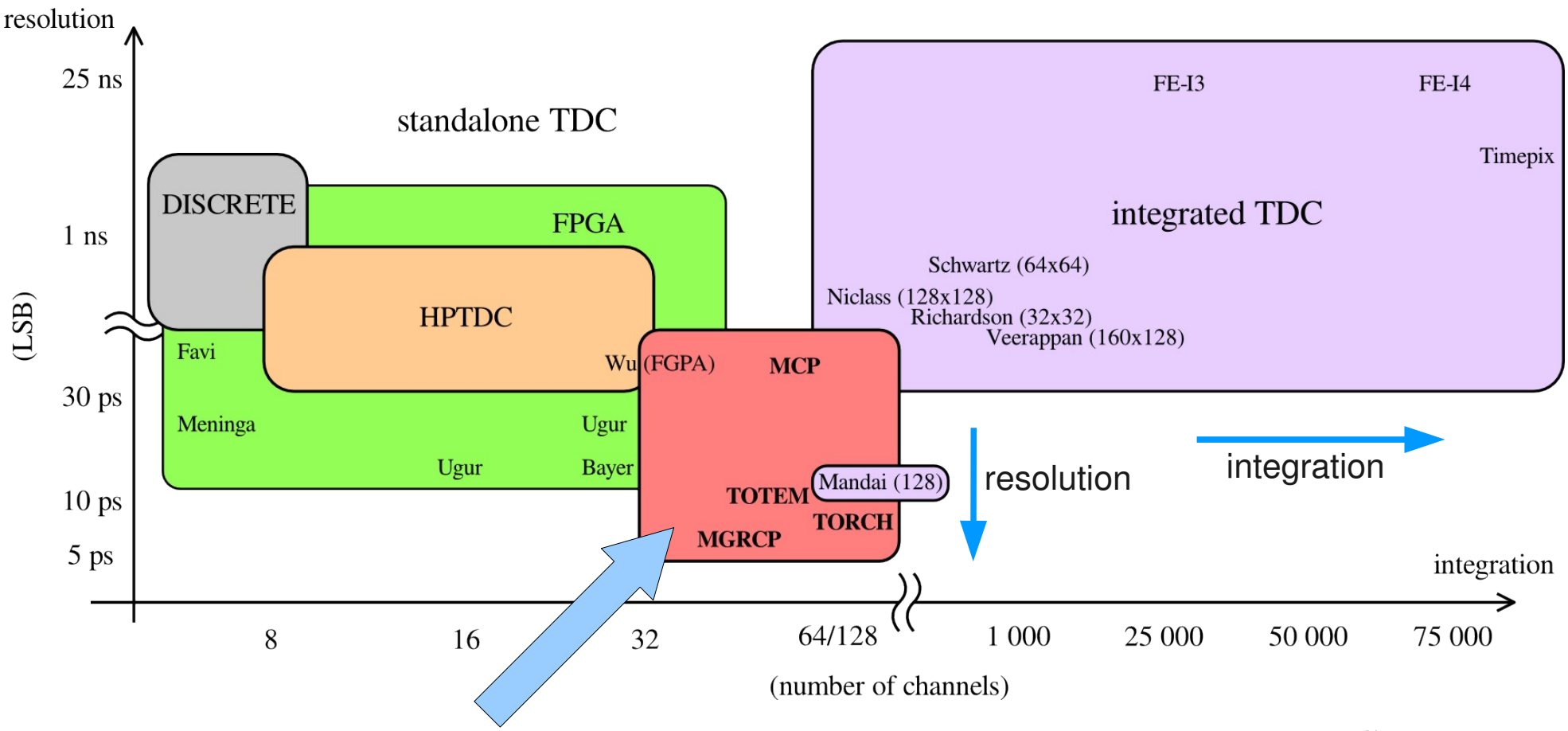
TDC development trends in HEP



LSB ≠ rms

new detectors and sensors require TDC < 10 ps resolution

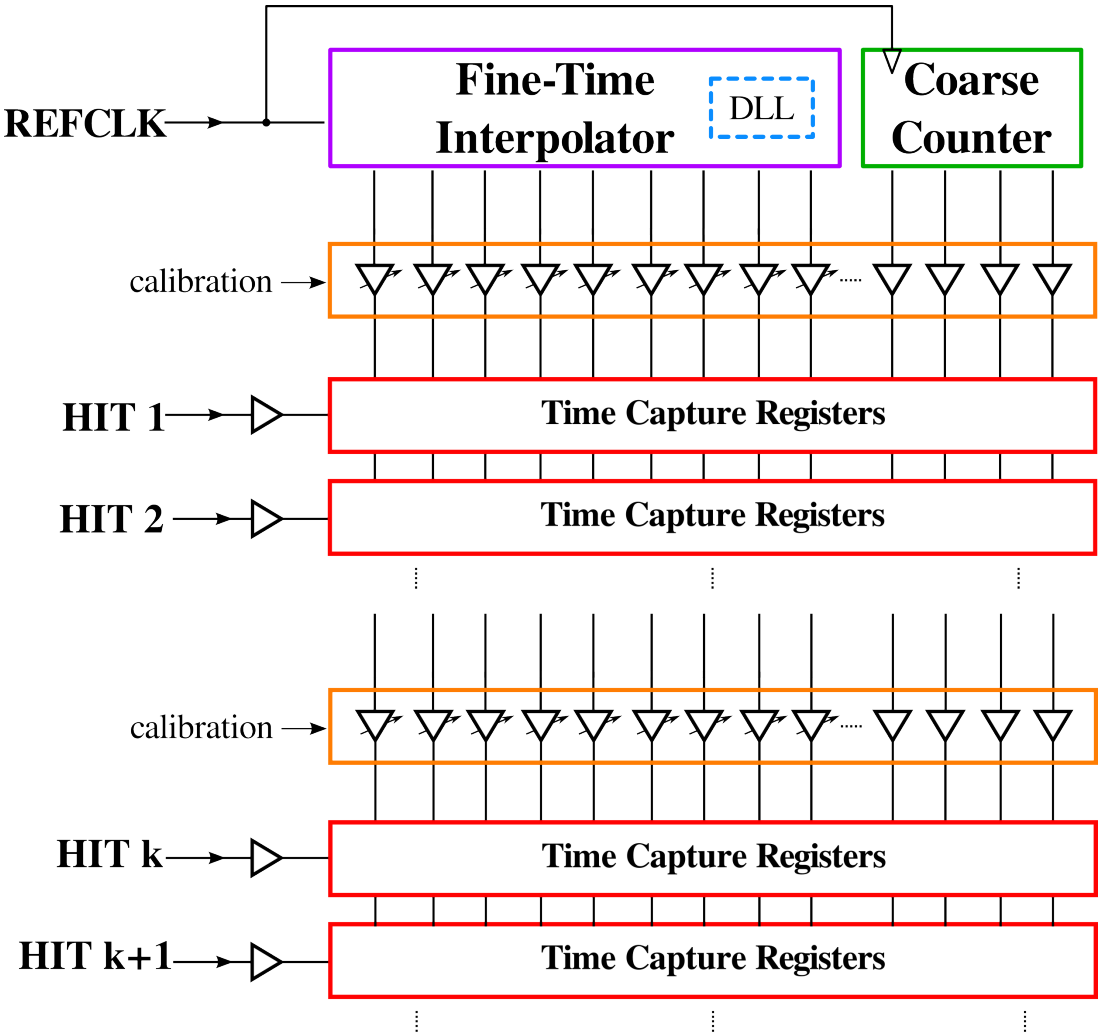
Demonstrator ASIC

Requirements

- achieve sub 10 ps LSB sizes
  -> with rms better than bin-size
- multiple channels (architecture easy extendable)
- large dynamic range
  -> allow to use one common reference
- robust against power supply noise
- flexible in terms of power consumption / time resolution

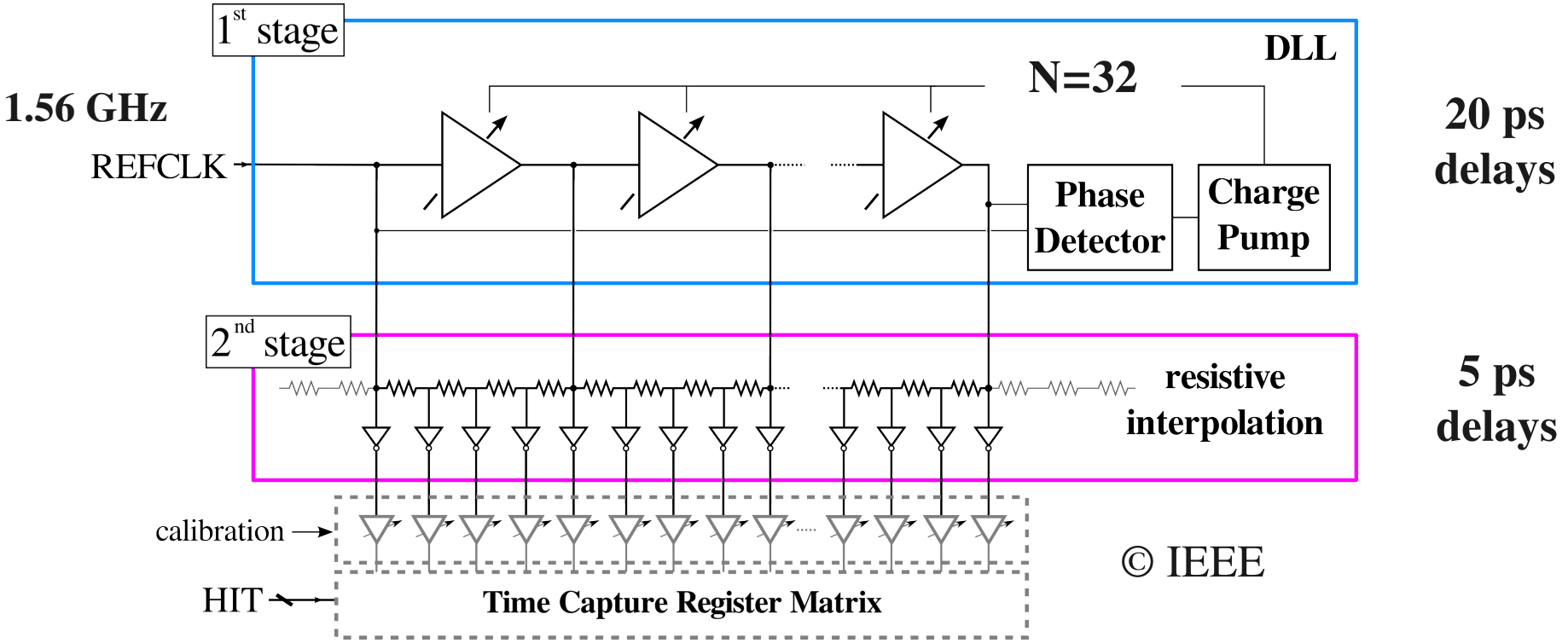
not a complete TDC -> demonstrates resolution of TDC

TDC Architecture



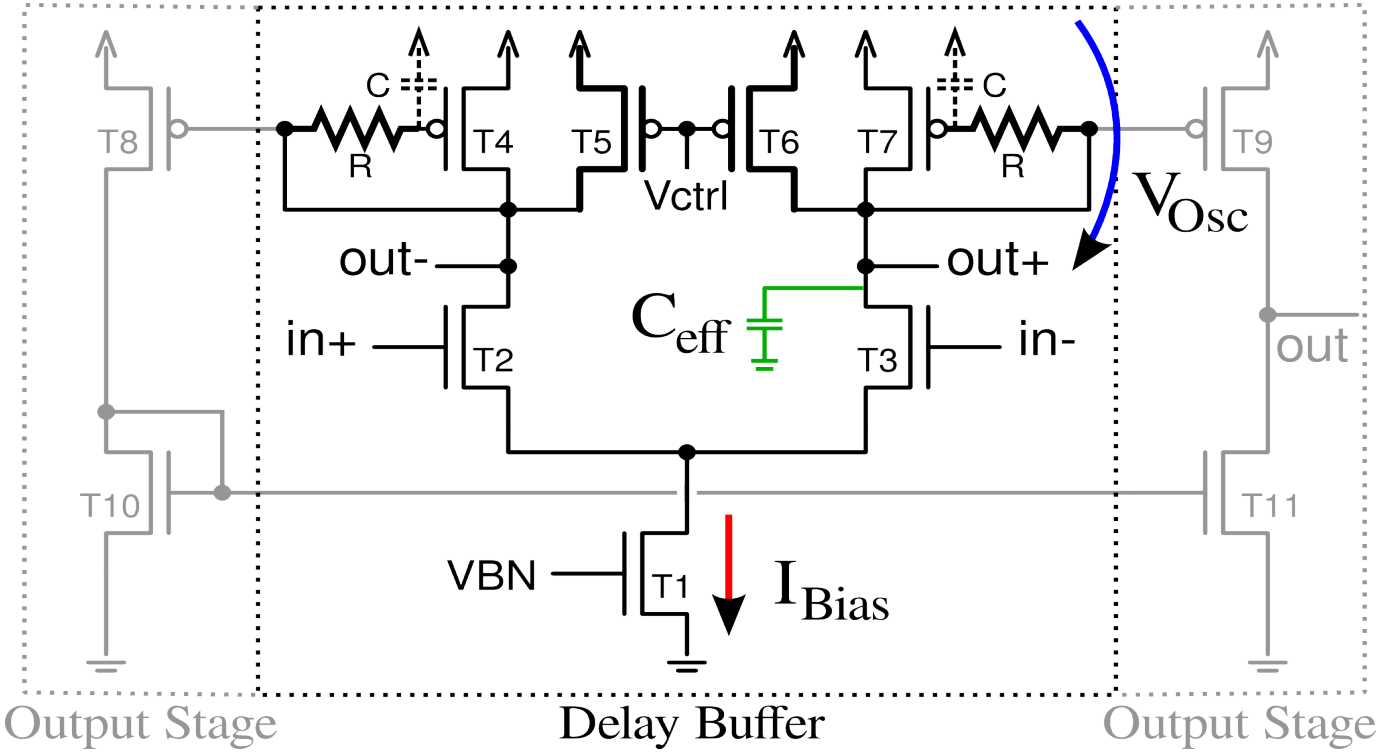
- central interpolator with counter to extend dynamic range
- measurements are referenced to common reference to allow to synchronize multiple TDCs
- DLL for PVT auto calibration and power consumption trade-off
- short propagation delays and fast signal slopes of timing critical signals to reduce jitter
- calibration applied on a group of channels to reduce circuit overhead and calibration time
- relatively constant power consumption make it less sensitive to change in hit rate

Fine-Time Interpolator



- **DLL to control LSB size**
  - -> 32 fast delay elements in first stage - 20 ps
  - -> total delay of DLL 640 ps at 1.56 GHz
- **Resistive Interpolation to achieve sub - gate delay resolutions**
  - -> LSB size of 2nd stage controlled by DLL

Voltage Controlled Delay Cell



- **fully differential cell**
- **voltage controlled**
- **single ended output**

additional zero in signal path

zero location

$$z = -\frac{1}{RC}$$

approximate propagation delay

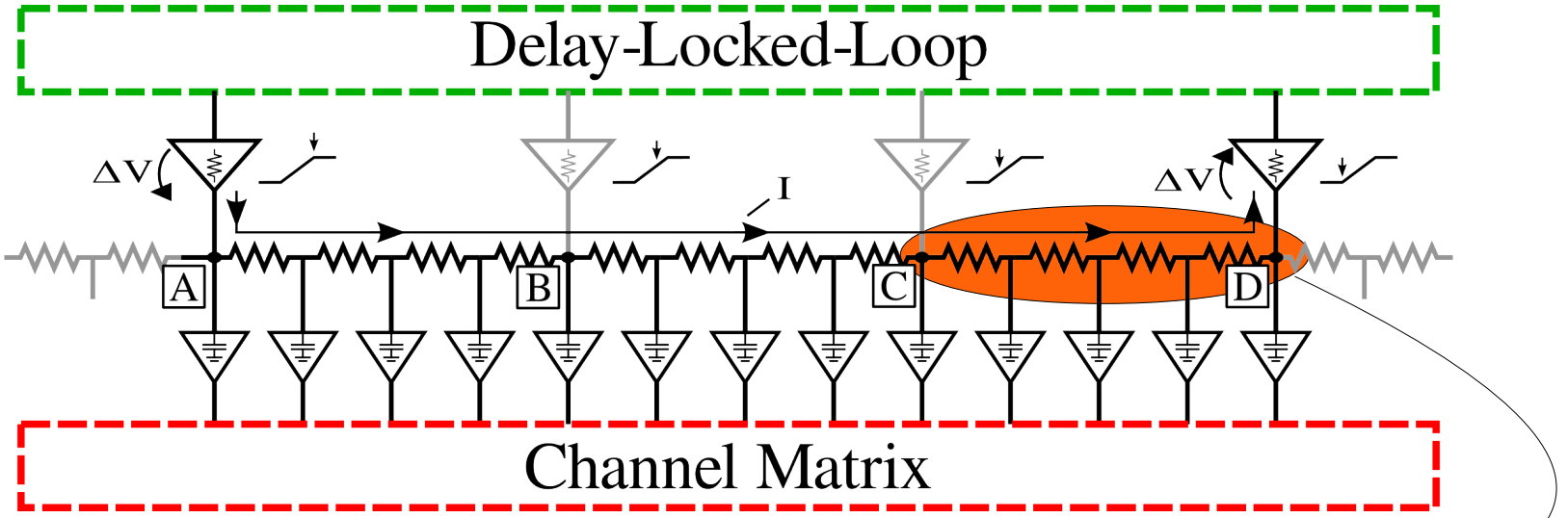
$$\delta \propto \frac{C_{eff} \cdot V_{Osc}}{I_{Bias}}$$

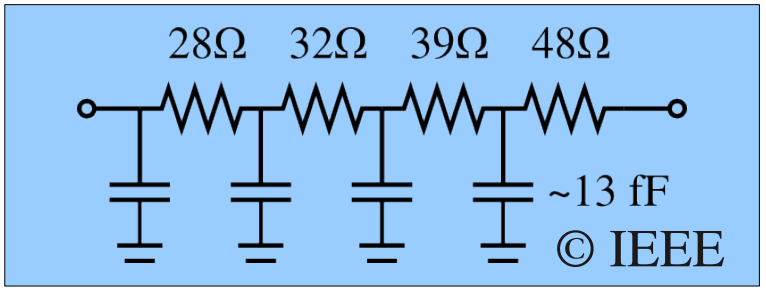
post layout extracted simulation

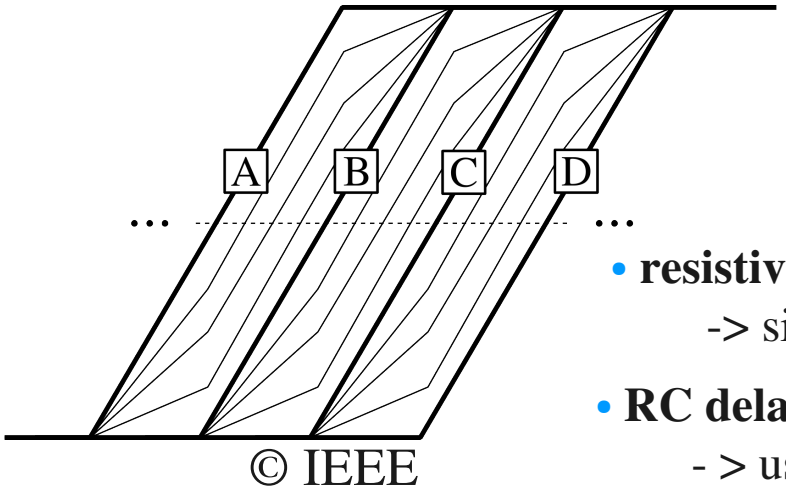
12 ps < 16 ps < 23 ps

@VDD = 1.2 V

Resistive Interpolation

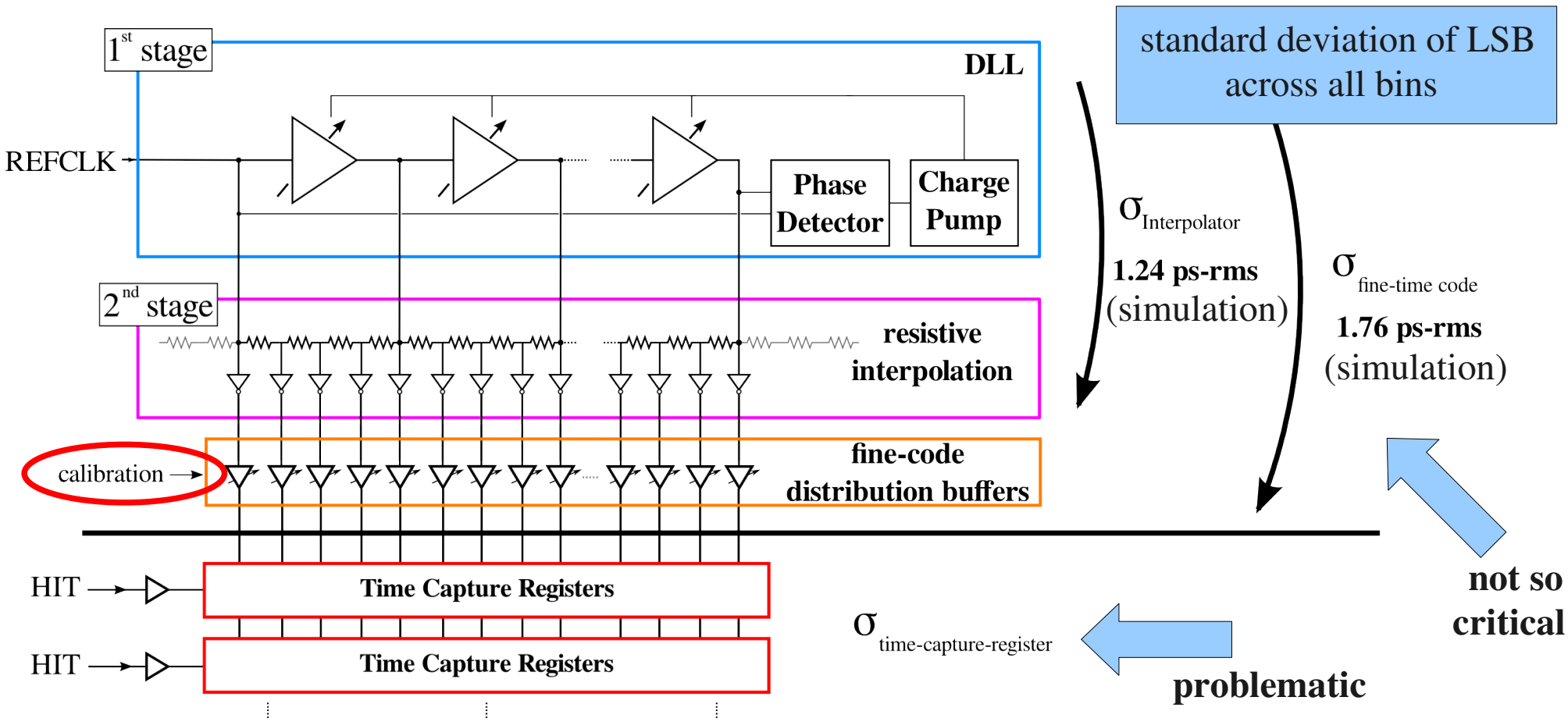






- **resistive voltage divider**
  -> signal slopes bigger than delay
- **RC delay** (capacitive loading)
  - > use small resistances, small loads

Device Mismatch

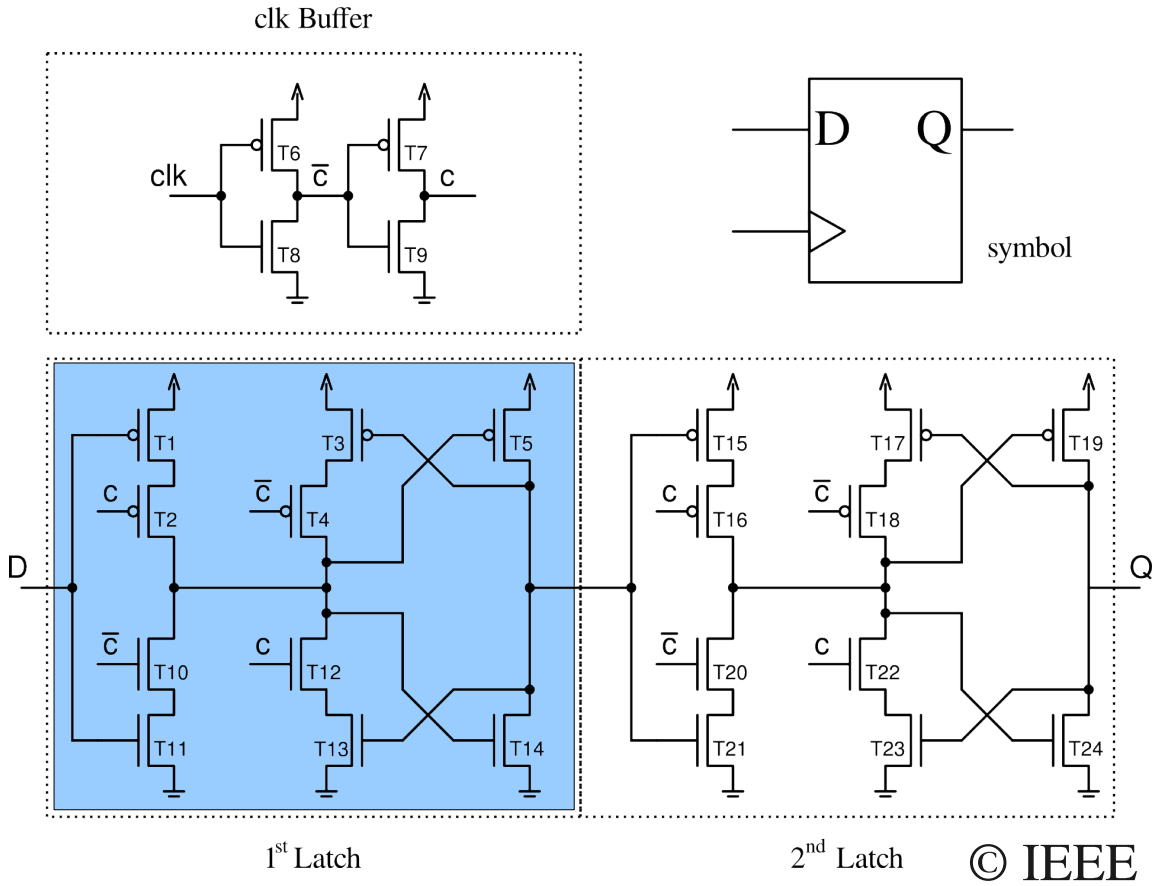


- Calibration can correct for Fine-Time Interpolator and Distribution Buffer mismatch
- Don't want to calibrate each single register
  -> time capture registers require good matching

Time Capture Register

no calibration in FF:

Trade off: power & resolution



1-Latch optimized for timing (3x size of standard cell FF)

σ_{TDC} = 1.31 ps-rms

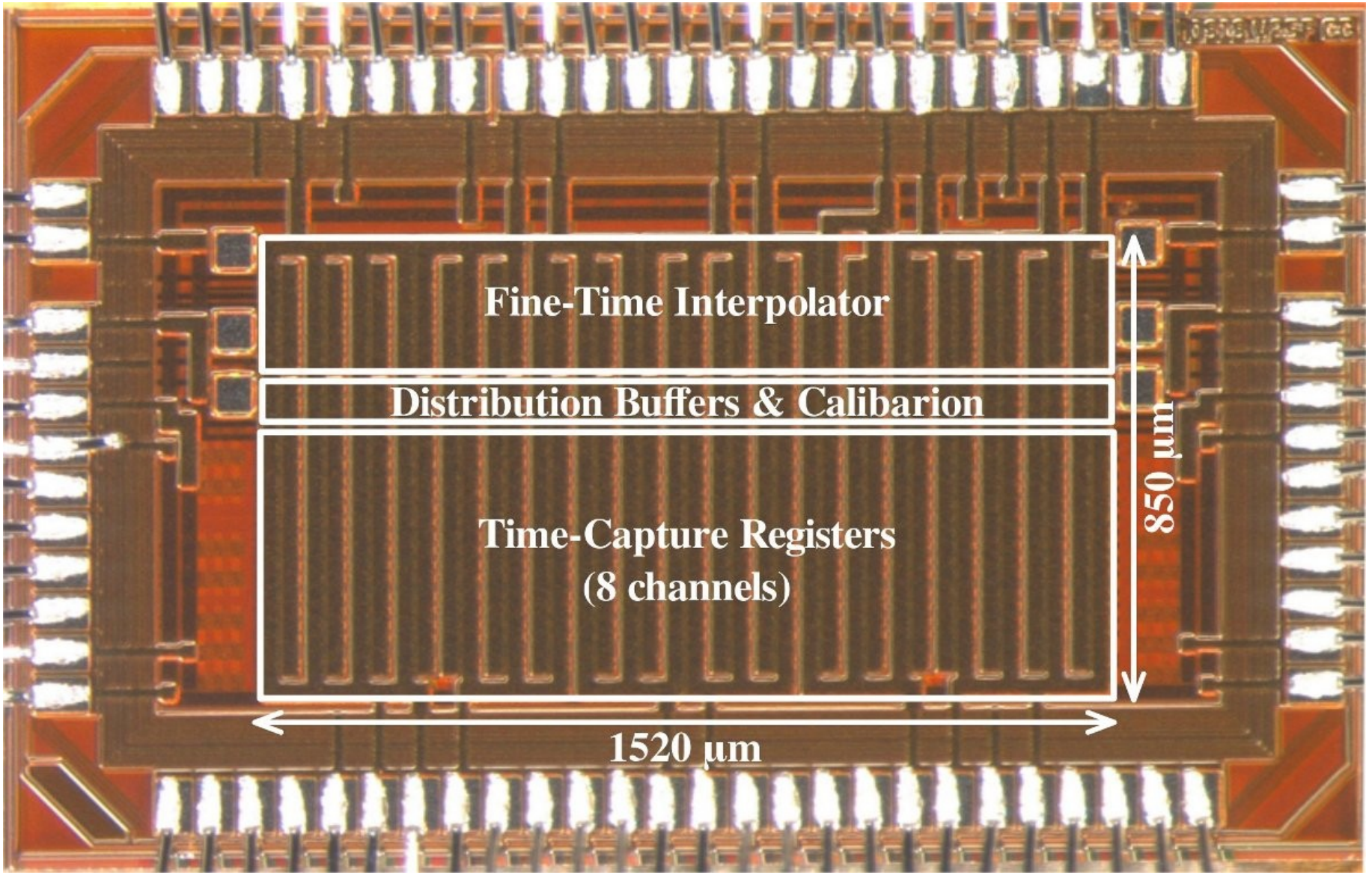
Just about good enough for 5 ps TDC

Outline

- **Time measurements in HEP**
- **Time-to-Digital Converter Concepts**
- **Challenges in Fine-Time Resolution TDC Design**
- **Demonstrator Architecture**
- **Measurement Results**
- **Conclusion**

Demonstrator Photograph

130 nm technology



Channel Configurations

- for easing test always two channels of a kind

compare different time capturing schemes

(not yet characterized)

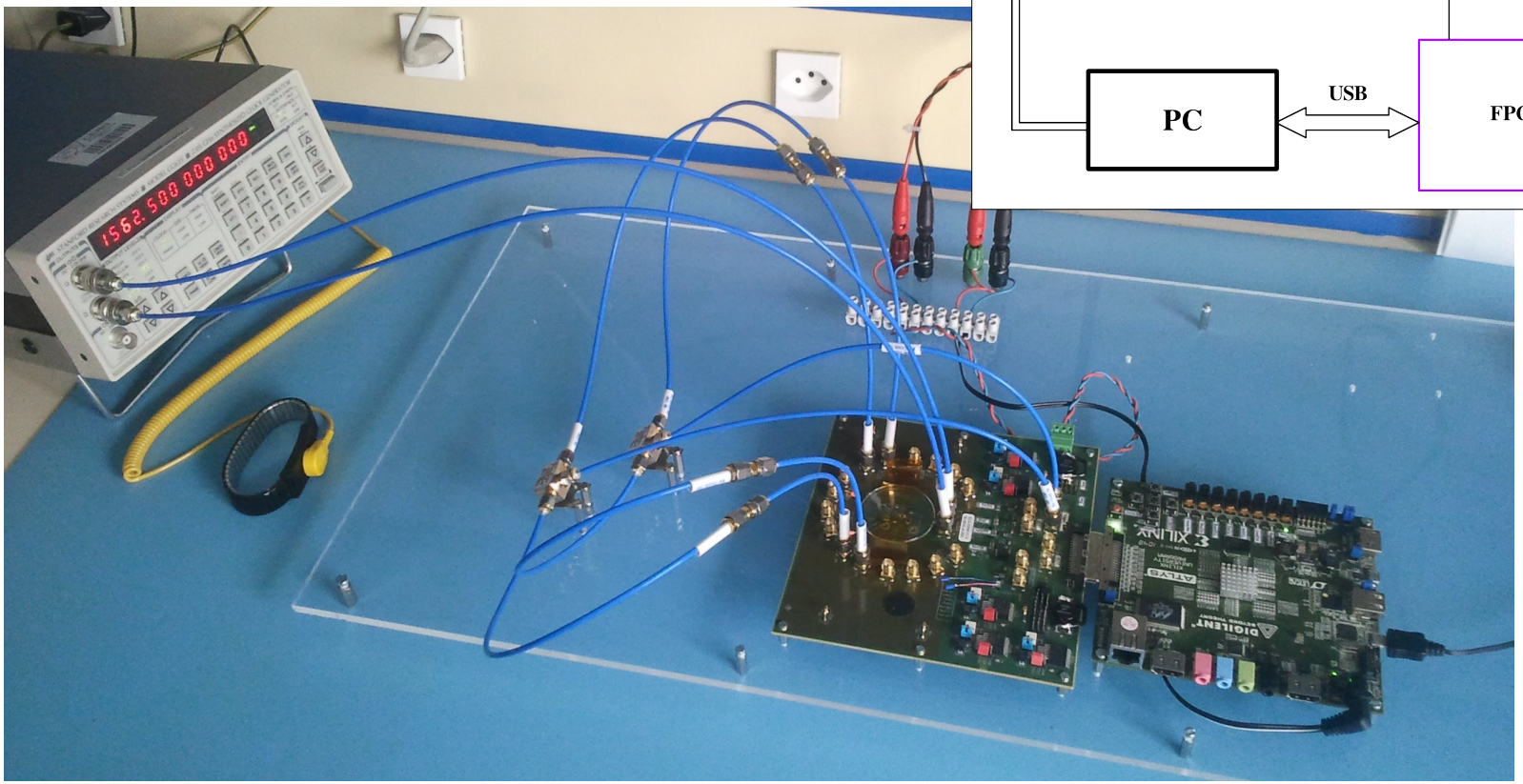
Channel	Input Buffer	Time Capture Register	Capturing Concept
1 & 2	GBT RX	direct drive FF (custom)	data driven
3 & 4	E-Link	standard FF (custom)	event driven
5 & 6	GBT RX	standard FF (custom)	event driven
7 & 8	GBT RX	standard FF (cell lib)	event driven

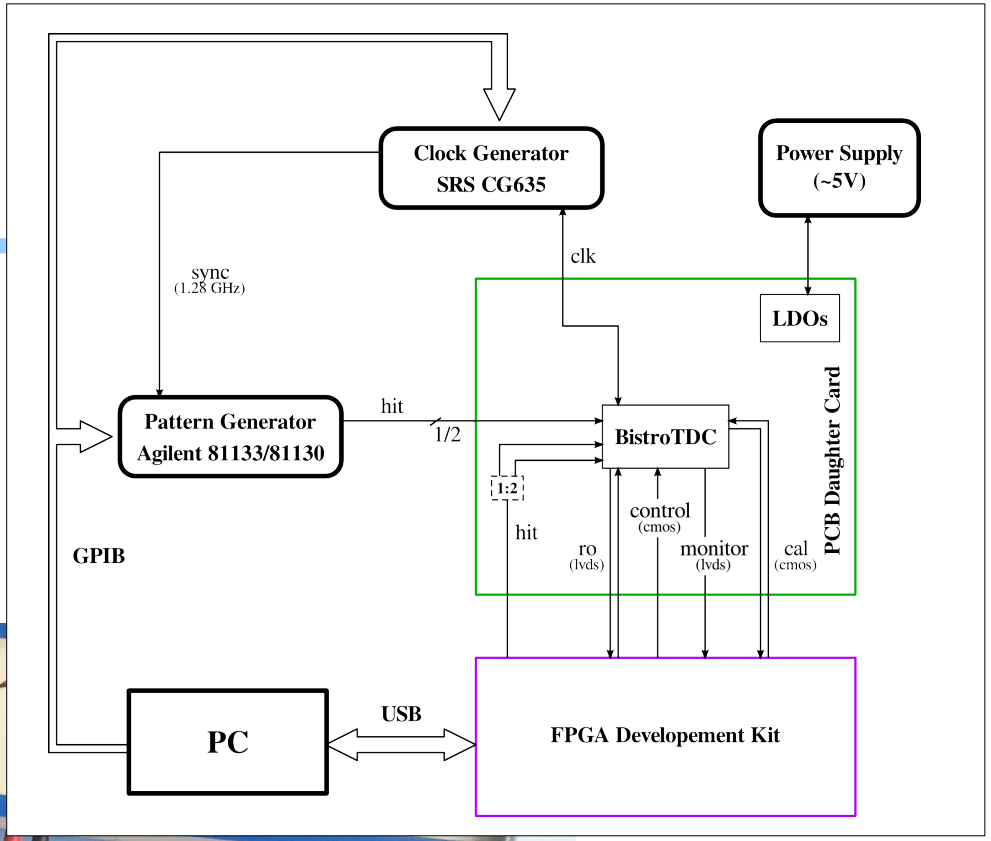
compare input buffer architectures

compare different time-capture-register sizes

Test Setup

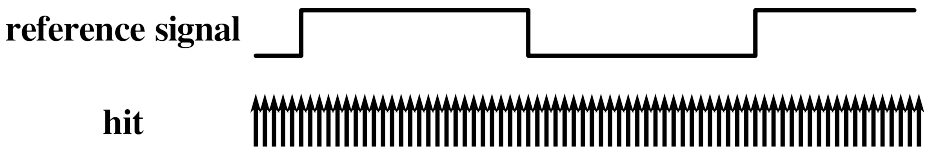
1562.5 MHz = 5 ps **@VDD = 1.3 V**

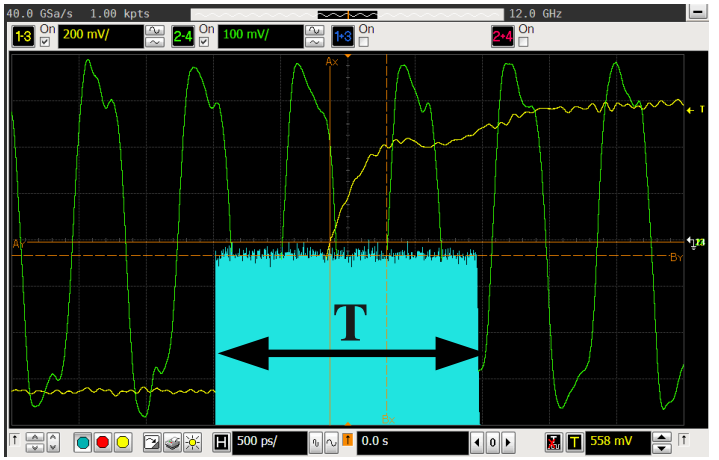




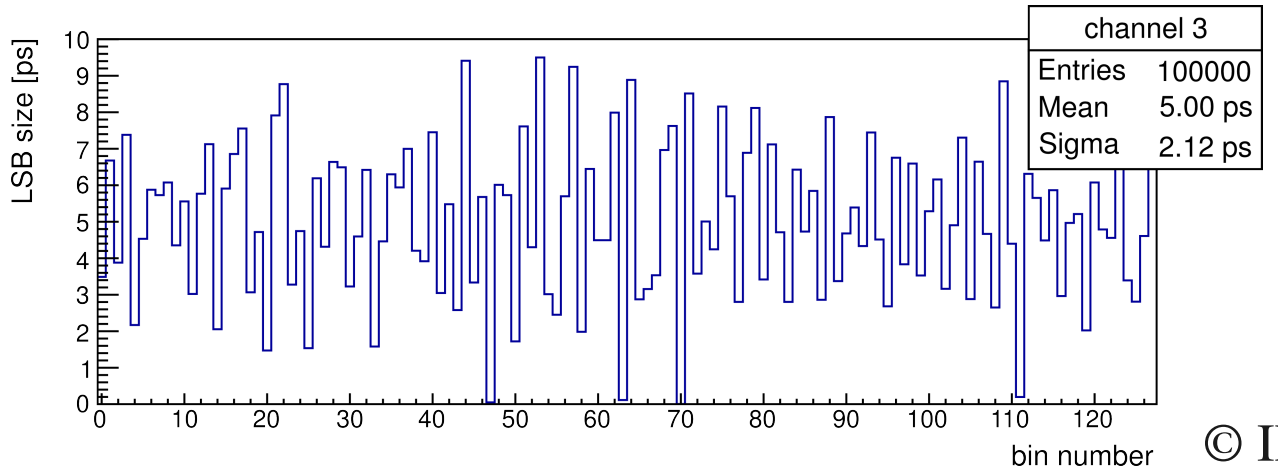
Code Density Test

- Uniformly distributed events across clock cycle
  - asynchronous clock domains
- Number of collected hits => bin size





- **Before Global Calibration**

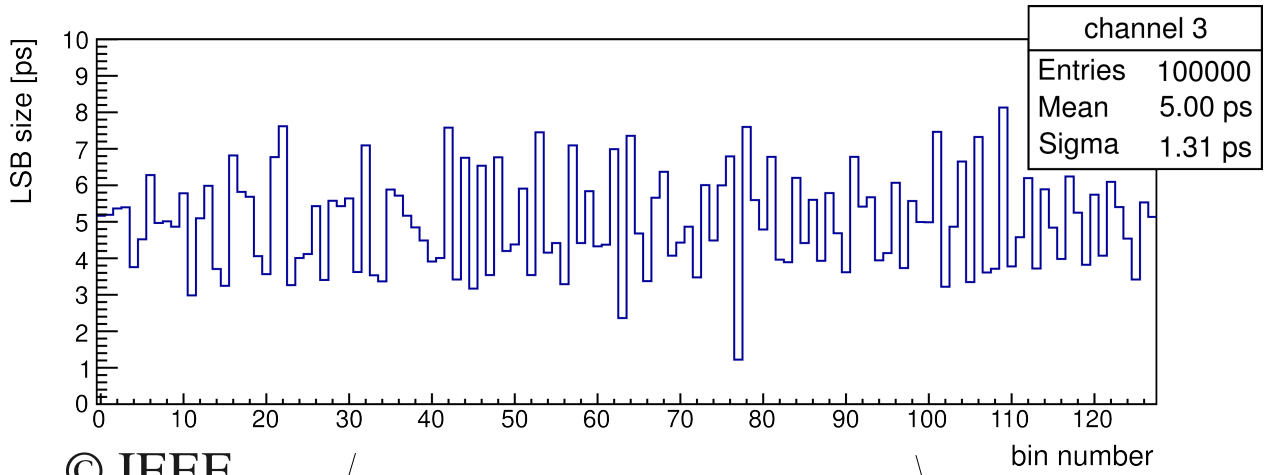


average LSB = 5ps

σ_{LSB} = 2.1 ps

Interpolator Linearity

- **After Global Calibration**



Differential-Non-Linearity

Integral-Non-Linearity

LSB = 5ps

before calibration:

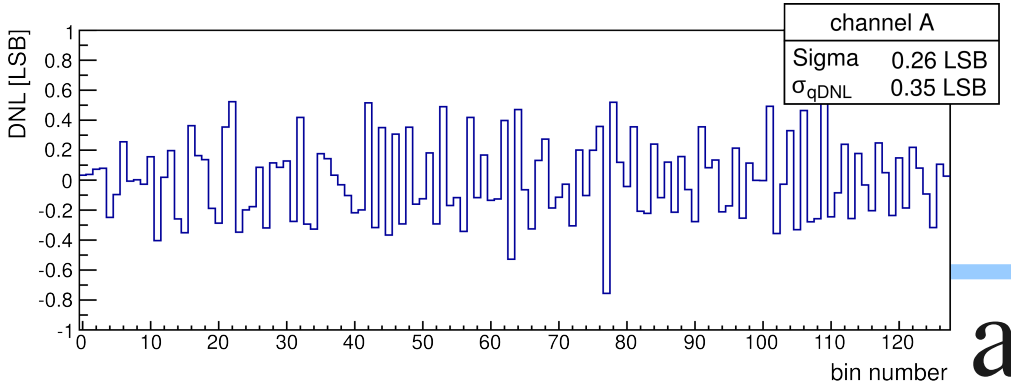
$\sigma_{LSB} = 2.1$ ps

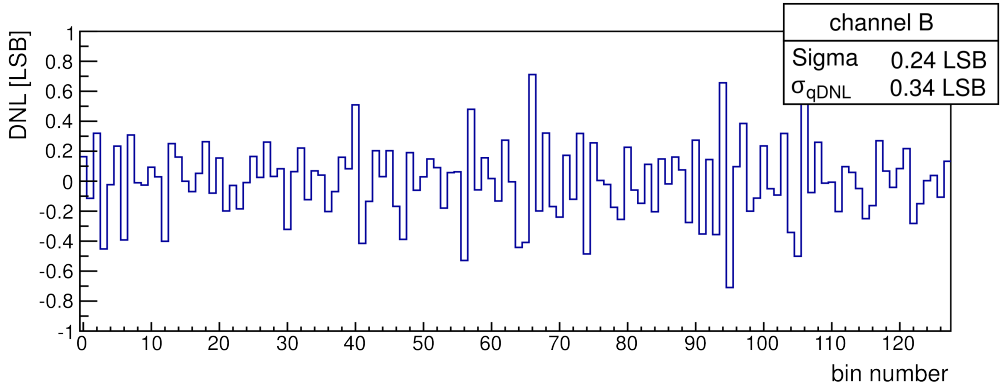
after calibration:

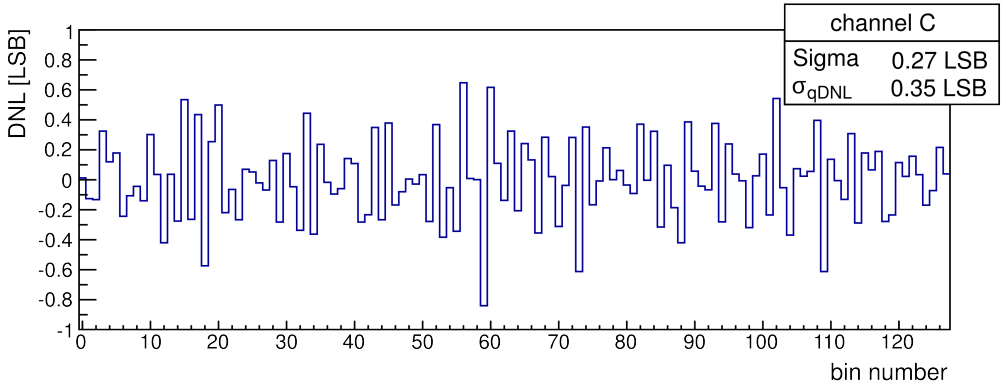
$\boldsymbol{\sigma_{LSB} = 1.3}$ **ps**

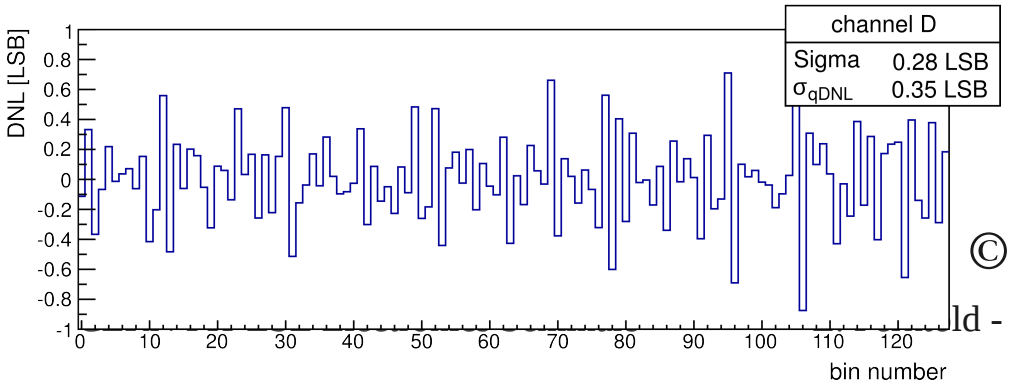
no missing codes

DNL
after global calibration





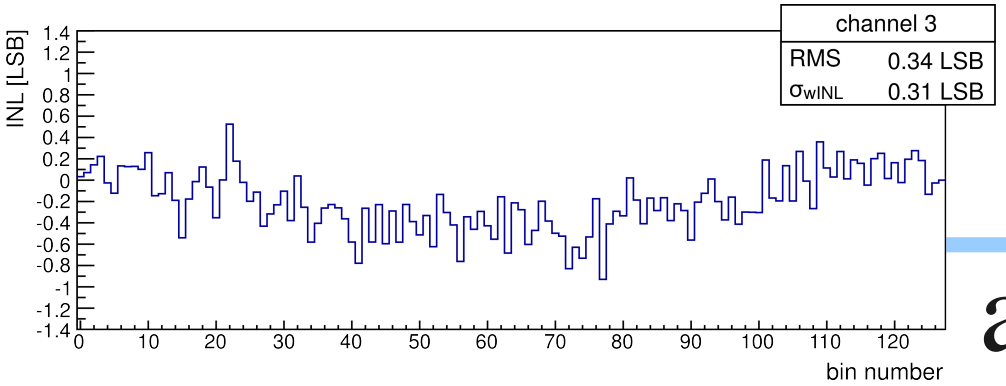


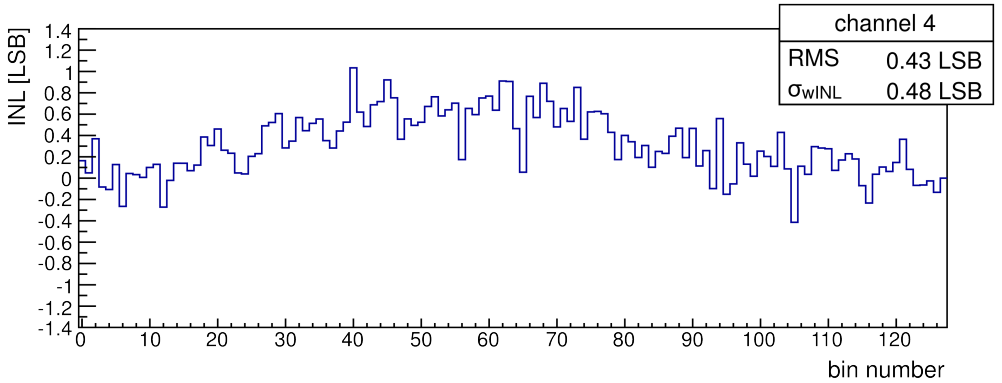


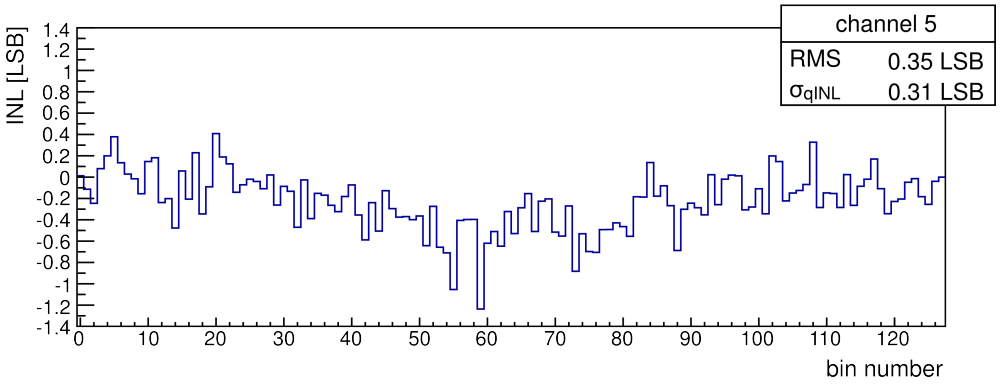
DNL = ± 0.9 LSB

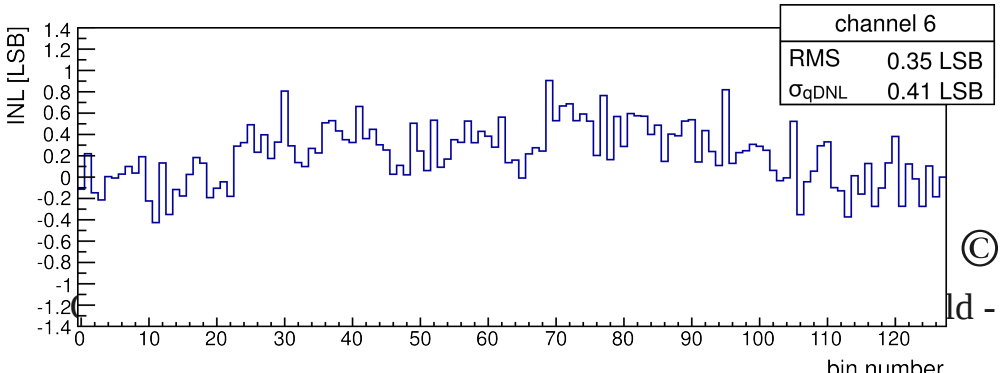
RMS < 0.28 LSB (1.4 ps-rms)

no missing codes









INL
after global calibration

INL = ± 1.3 LSB

RMS = < 0.43 LSB (2.2 ps-rms)

(could correct for INL offline)

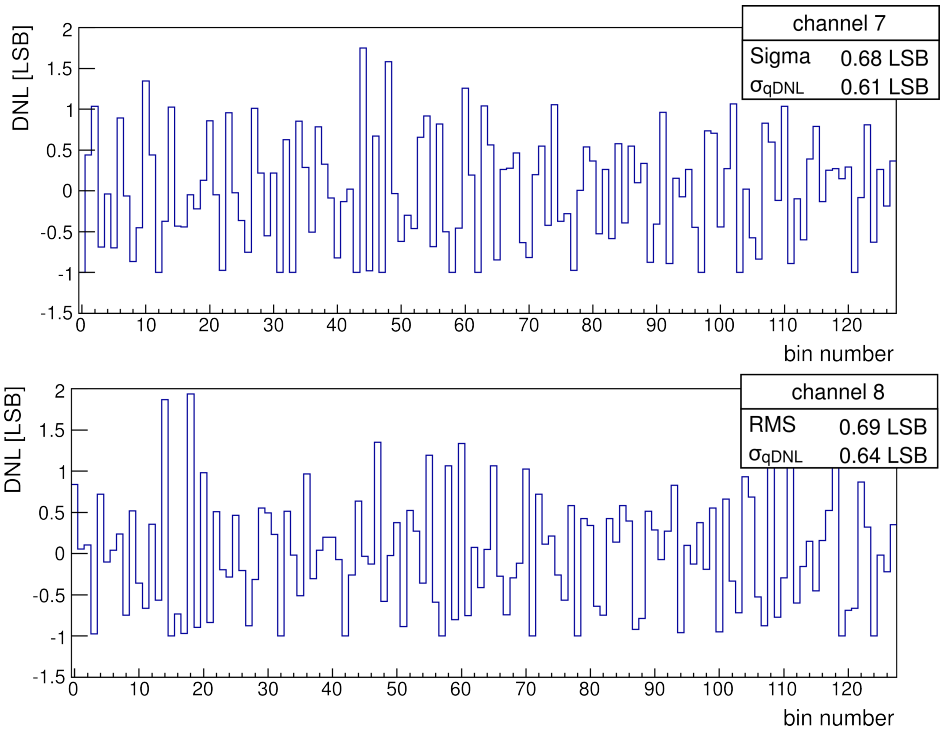
expected rms resolution w/ custom FF:
including quantization noise, INL & DNL

2.3 ps-rms < $\sigma_{qDNL/wINL}$ < 2.9 ps-rms

ideal 5 ps LSB TDC: 1.44 ps-rms

Standard Cell FF - Weak Matching

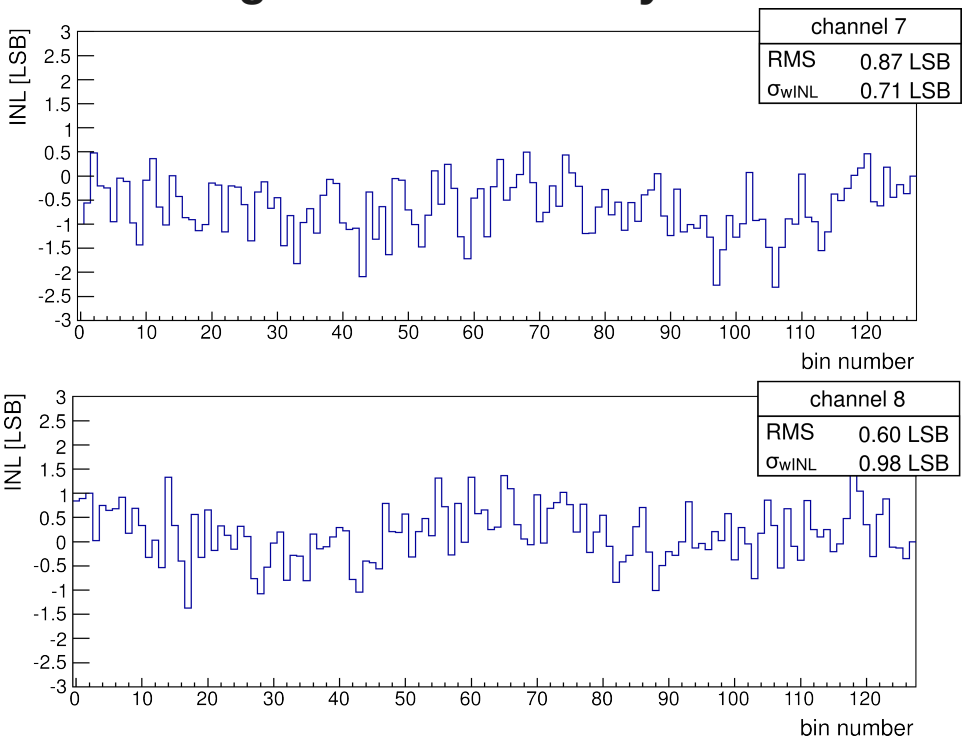
Differential-Non-Linearity



DNL = +2 LSB / -1 LSB

RMS = < 0.69 LSB (3.45 ps-rms)

Integral- Non-Linearity

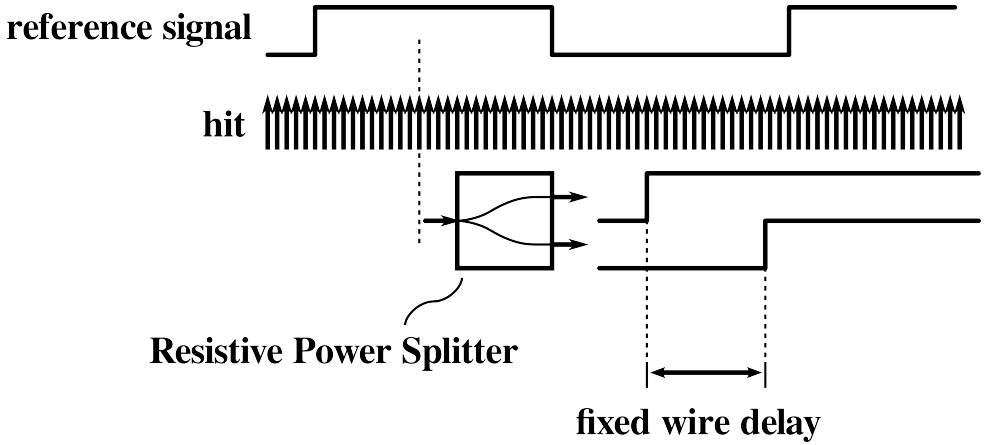


INL = ±2.5 LSB

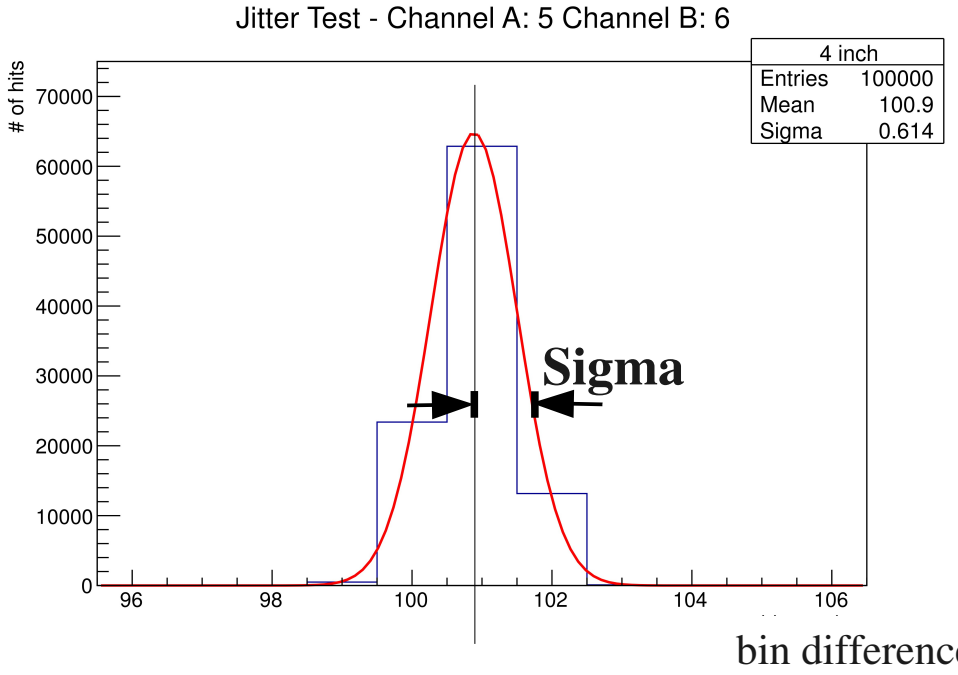
RMS = < 0.87 LSB (4.35 ps-rms)

expected time resolution: < 5.9 ps-rms (w/ standard cell FF)

Double Shot Measurement Principle



- Uniformly distributed events across 1 clock cycle
  - asynchronous clock domains
- Send same hit to two distinct channels
- Delay fixed by wire length differences
- Jitter contribution of hit not canceled out

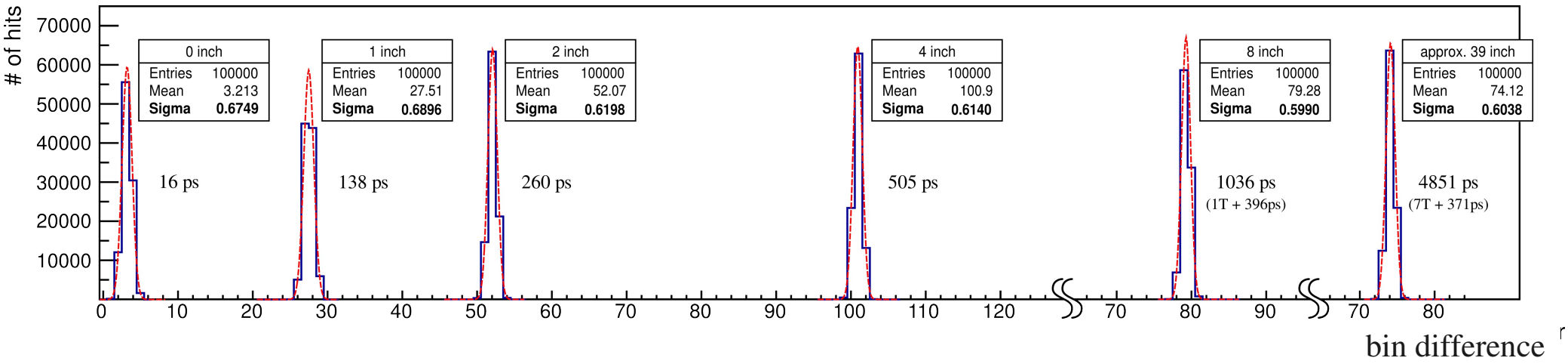


Single Shot Resolution in ps

Sigma*5ps/sqrt(2)

Measured Single Shot Precision

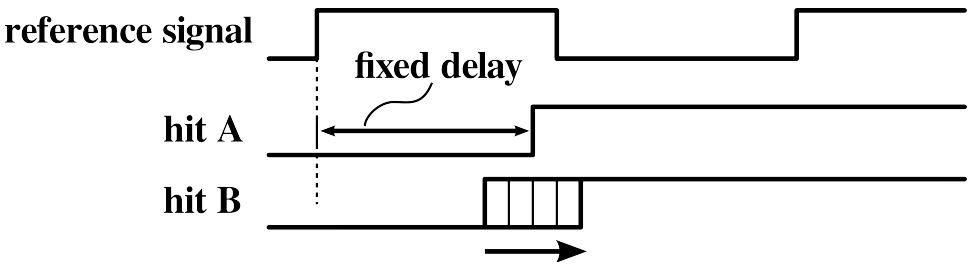
- Three measurement series
  - both hits arriving within one reference clock cycle
  - second hit arrives one clock cycle later
  - second hit arrives multiple clock cycles later (~5ns)



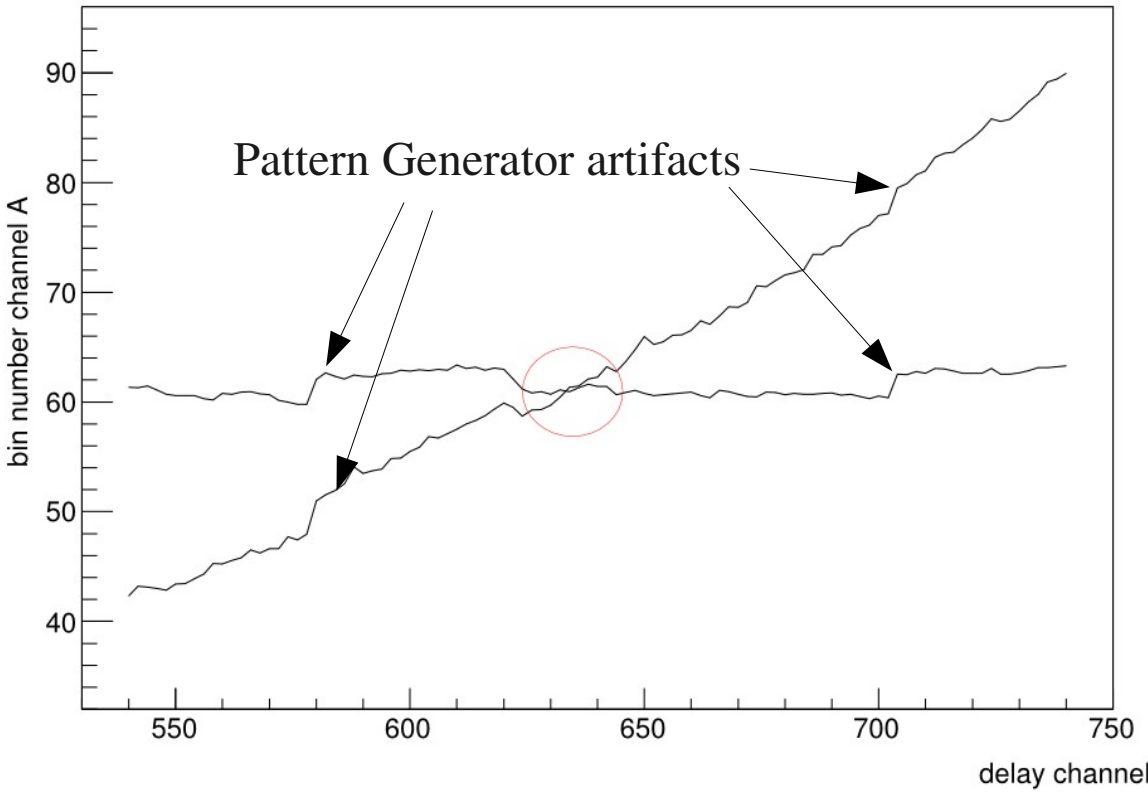
σ_{TDC} < 2.44 ps-rms

- limited by non-linearities of TDC
  - -> very silent setup
  - -> robust architecture

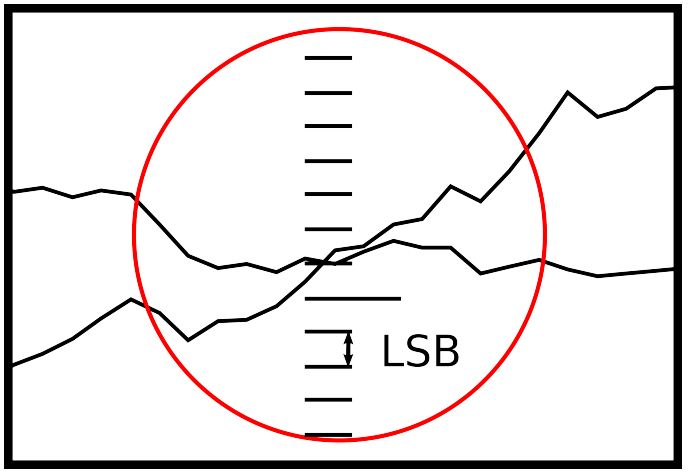
Inter Channel Crosstalk



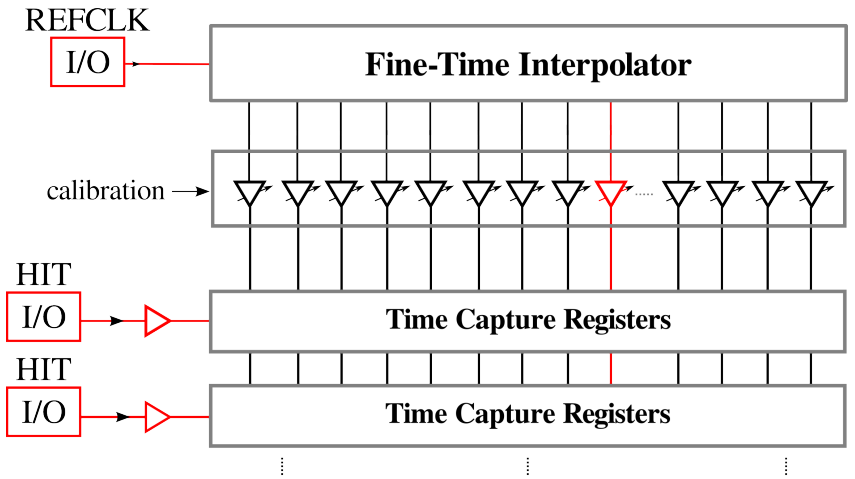
- sweep hit B over hit A
- monitor change in delay of hit A



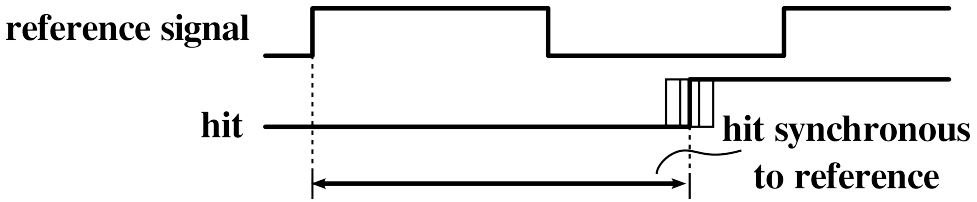
smaller ± 1 LSB

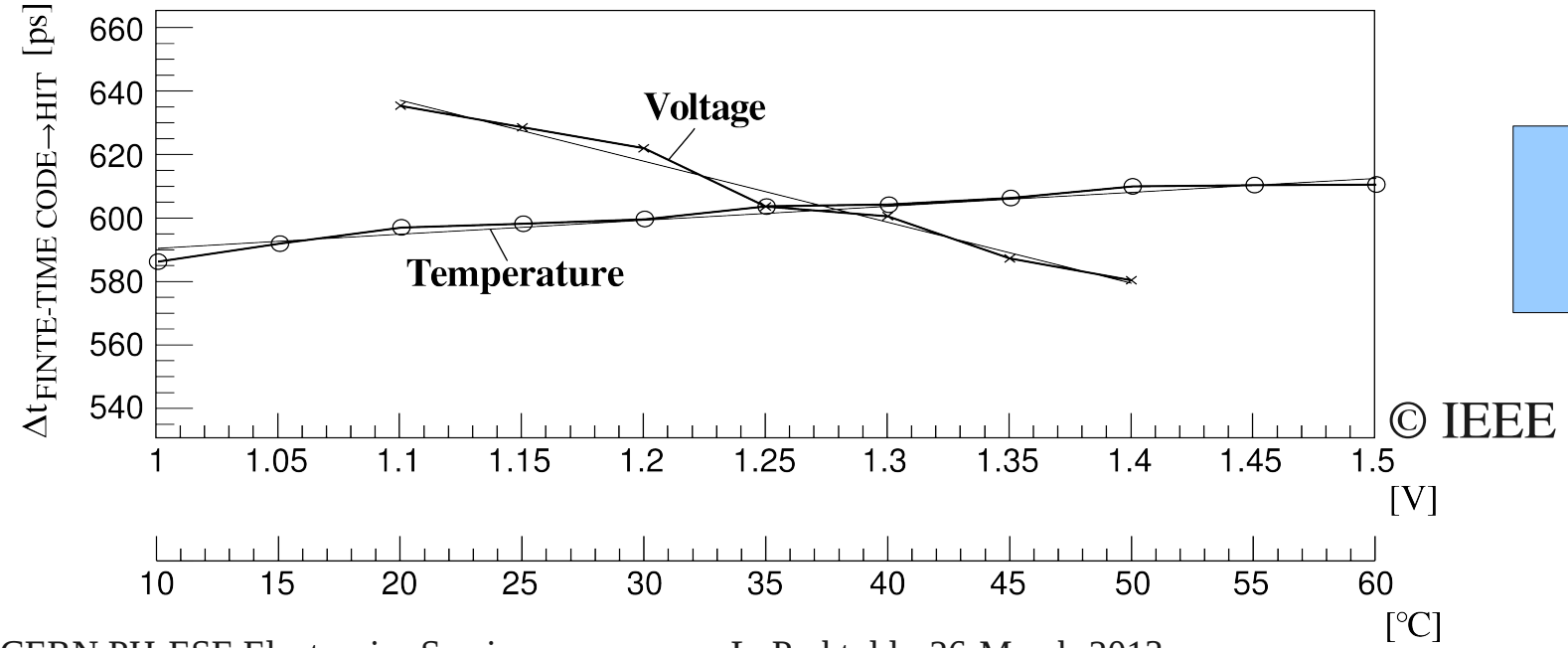


PVT variations



- constant delay path changes wrt VT
- different characteristic for different i/o





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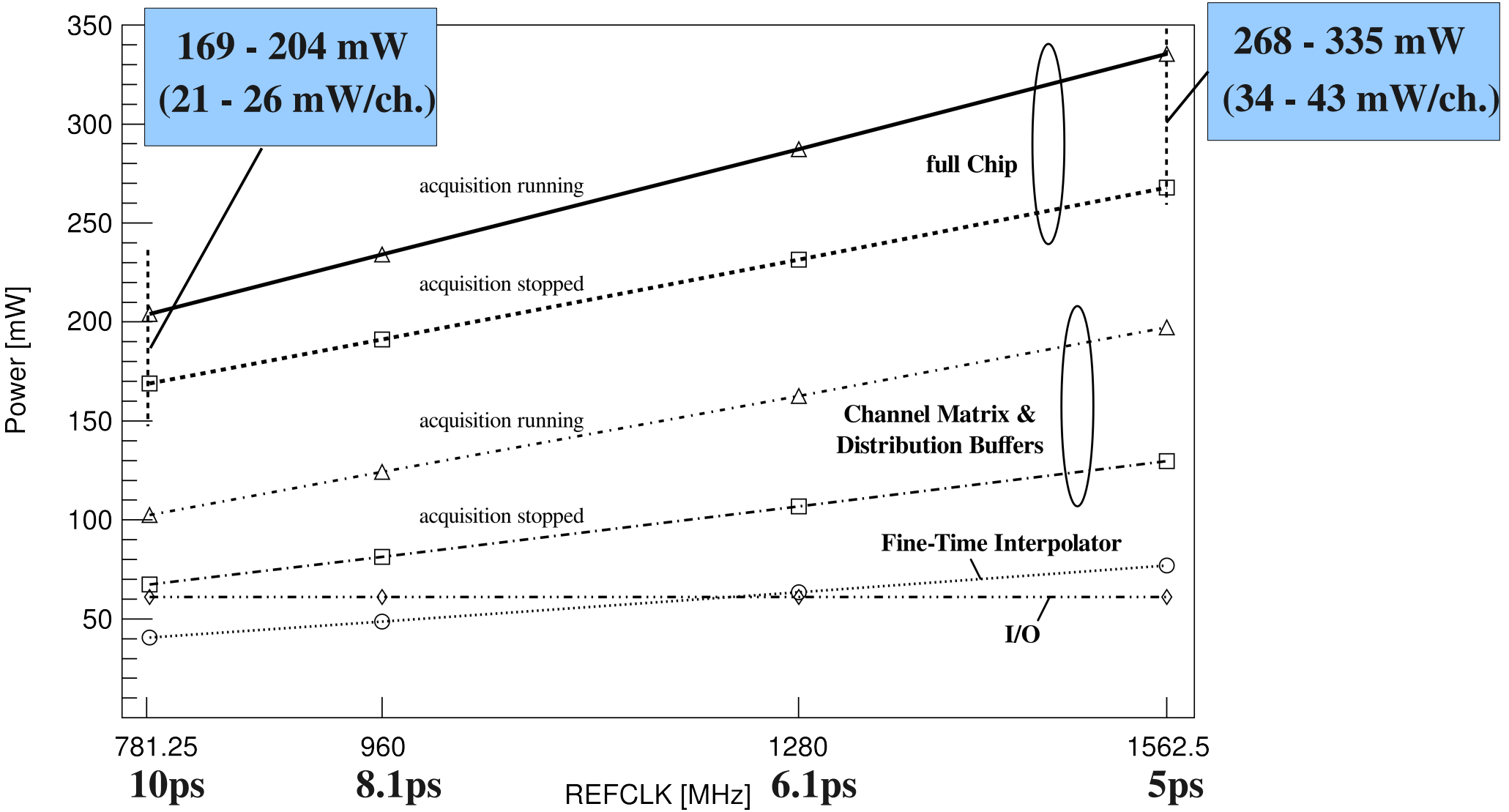
-0.2 ps / mV
0.4 ps / deg

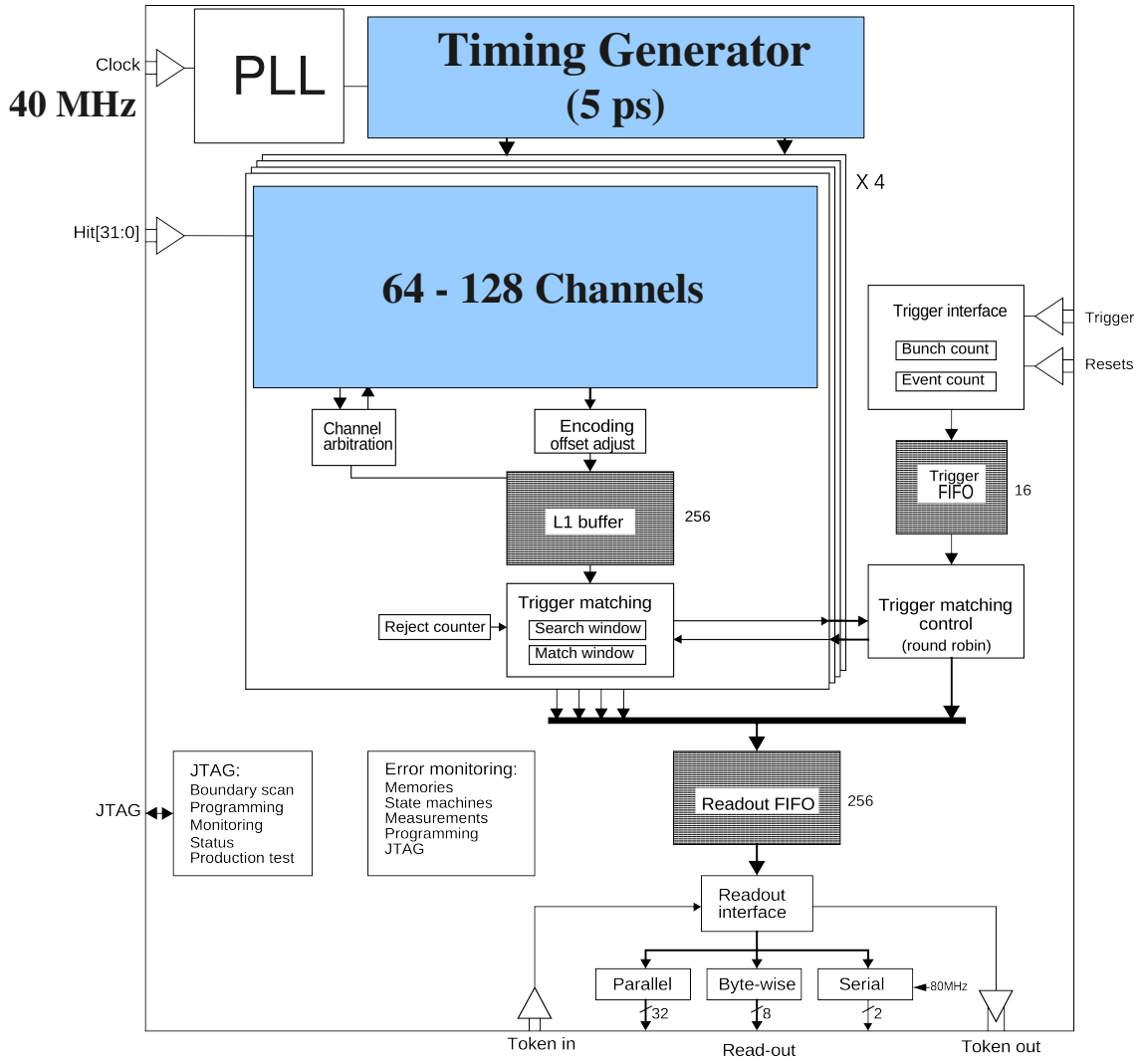
Power consumption

8 channels



Full TDC ASIC

TDC Architecture:



Demonstrator ASIC

- < 3 ps-rms resolution
- < 50 mW/channel
- missing counter, PLL and digital logic

Full TDC

- based on HPTDC
- 64 - 128 channels per ASIC
- 40 MHz input clock
- < 5 ps-rms timing precision
- radiation tolerant
- flexible readout architecture

Outline

- **Time measurements in HEP**
- **Time-to-Digital Converter Concepts**
- **Challenges in Fine-Time Resolution TDC Design**
- **Demonstrator Architecture**
- **Measurement Results**
- **Conclusion**

Conclusion

- A demonstrator ASIC has been designed, constructed and successfully tested.
- Time resolutions as low as 3 ps-rms have been demonstrated
- Device mismatches considerably affect design in the ps-domain
  -> trade off power & resolution & calibration effort
- Macro suitable for a full fine-time resolution general purpose TDC

The end

Thank you for your attention!

Demonstrator Performance Summary	
Technology	130 nm
Supply Voltage	1.3 V
Area	1.2 mm^2
Power Consumption	34 - 42 mW/channel
# of Channels	8
LSB size	5 ps
DNL	± 0.9 ps
INL	± 1.3 ps
Single Shot Precision	< 3 ps-rms
Dynamic Range	640 ps (on chip)

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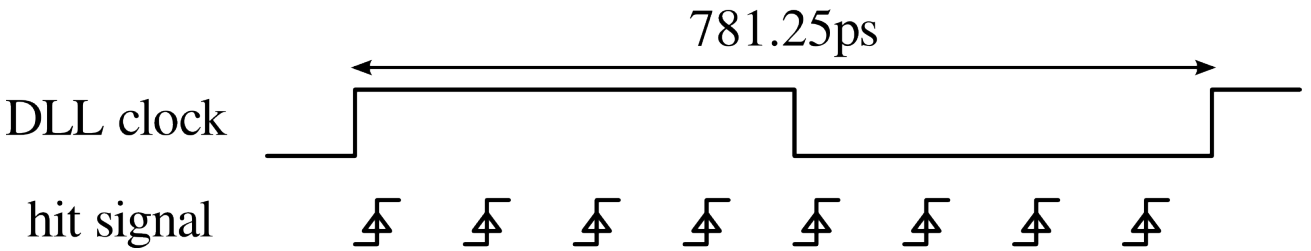
BACKUP

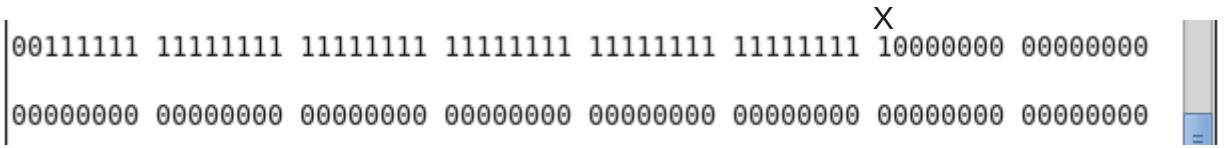
Functional Test (uncal/ DLL)

5-10 measurements



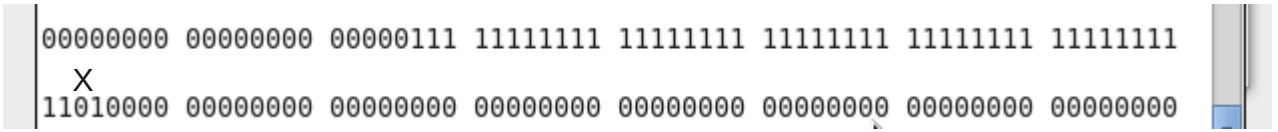
$\Delta t_{osc\text{-}ch7}$ = 445 ps

ch7
0 ps



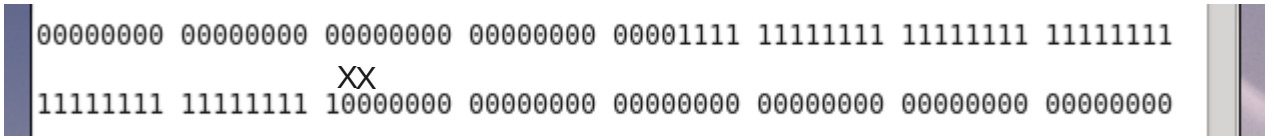
osc. = 12 ps+
bin_{rise} = 2*
t_{TDC} = 12 ps

ch7
100 ps



osc. = 125 ps
bin_{rise} = 21
t_{TDC} = 128 ps

ch7
200 ps



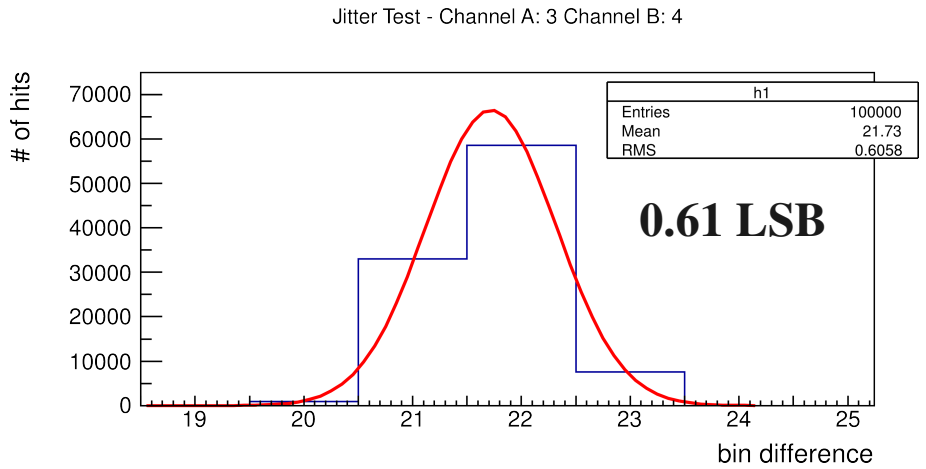
osc. = 215 ps
bin_{rise} = 36
t_{TDC} = 220 ps

+ reference calibration point
* 00-11 transitions represents falling edge. DLL sends inverted signal to profit from stronger NMOS devices.

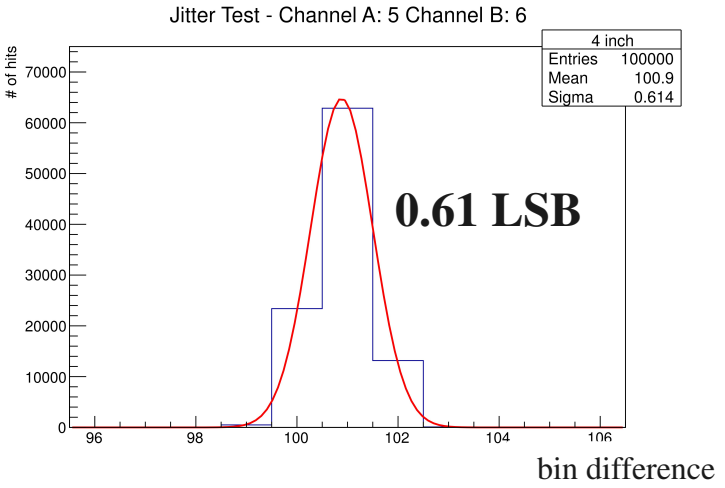
Duty-Cycle = 37 %

I/O Buffer Influence

- **E-Link ~ 1mA**

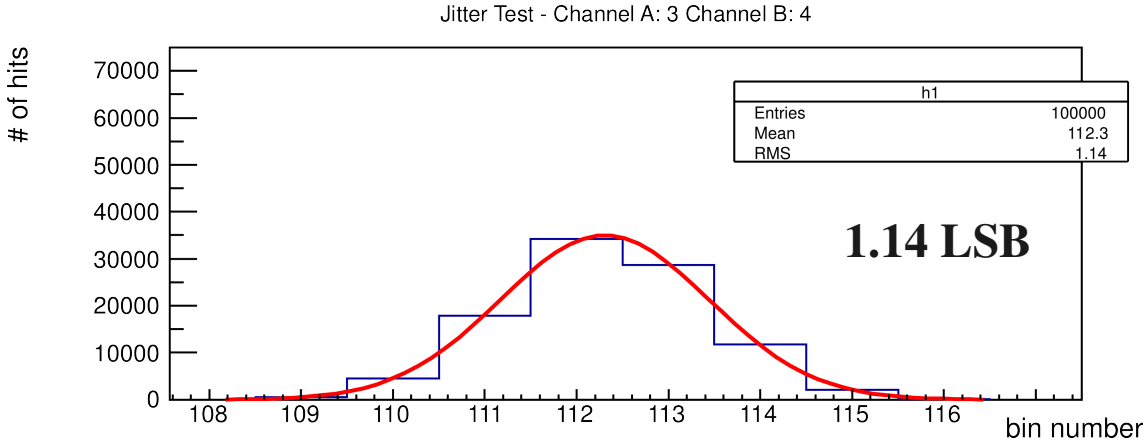


- **GBT RX ~ 10mA**

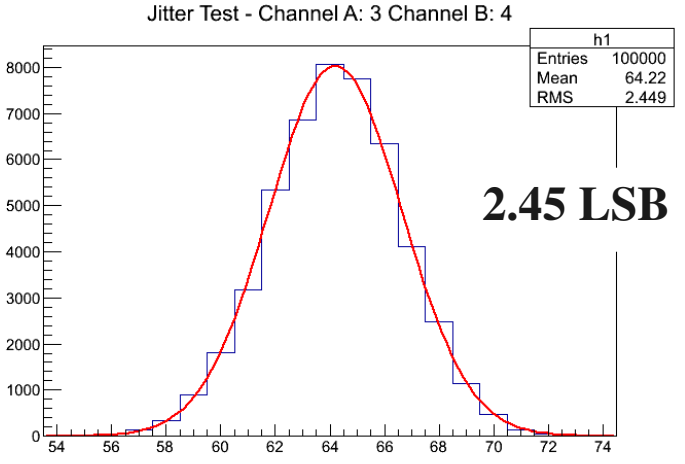


- attention on Vcm level and VDD

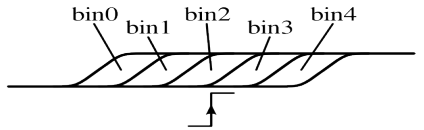
VDD = 1.35 V, Vcm = 1.2 V



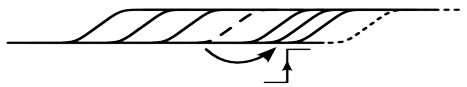
VDD = 1.2 V, Vcm = 1.2 V



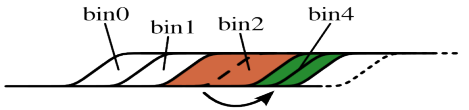
Bin Assignment



111|000

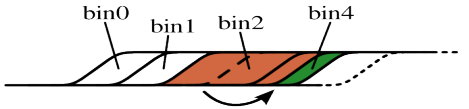


111010 | 0



'fill'

111|010



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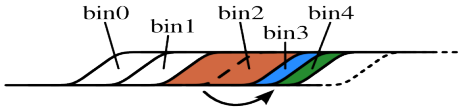
1110|10



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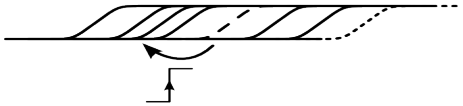
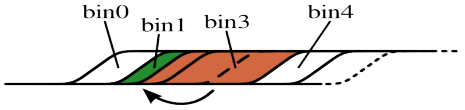
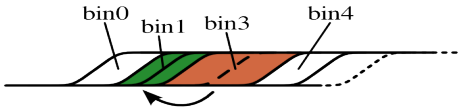


1101|000



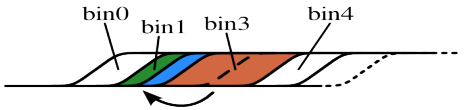
'fill'

1101000



'cut'

1101|000

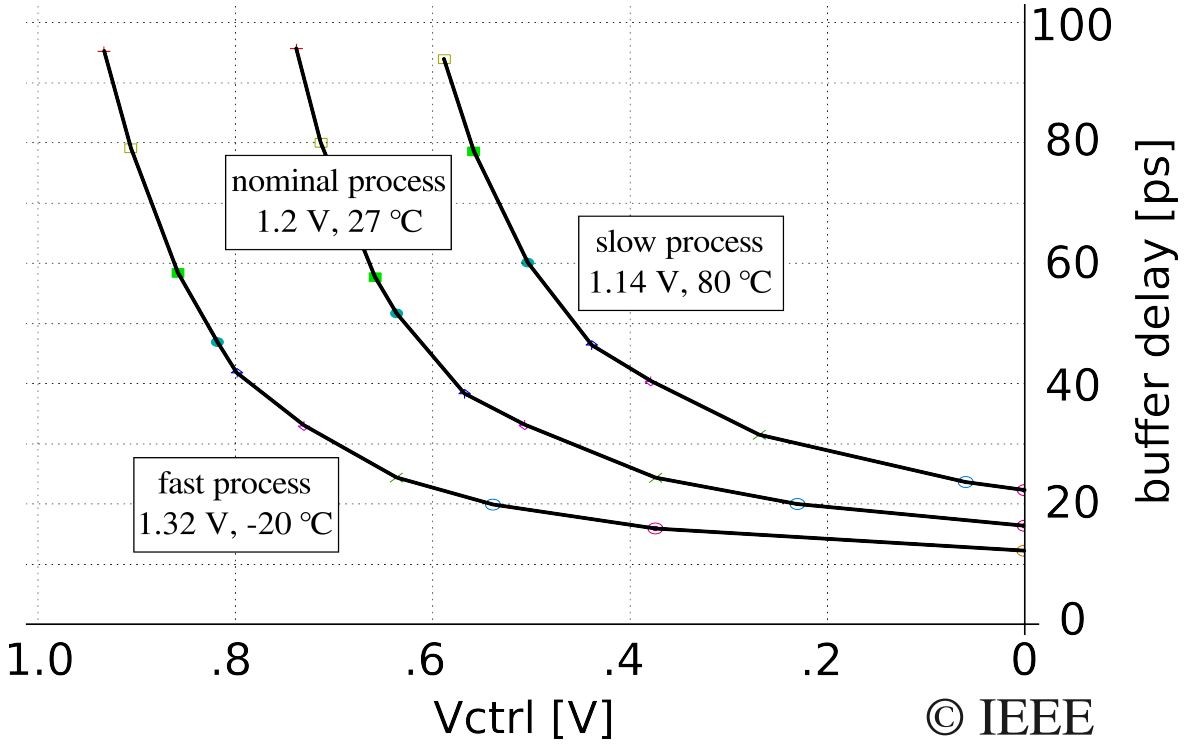


'group'

Reference Clock Frequency

5 ps = 1562.5 MHz

- How fast the delay line can go depends on process variations and operating conditions



Post Layout Extracted

LSB: **12/4 ps - 23/4 ps**

REFCLK: **1.38 - 2.60 GHz**

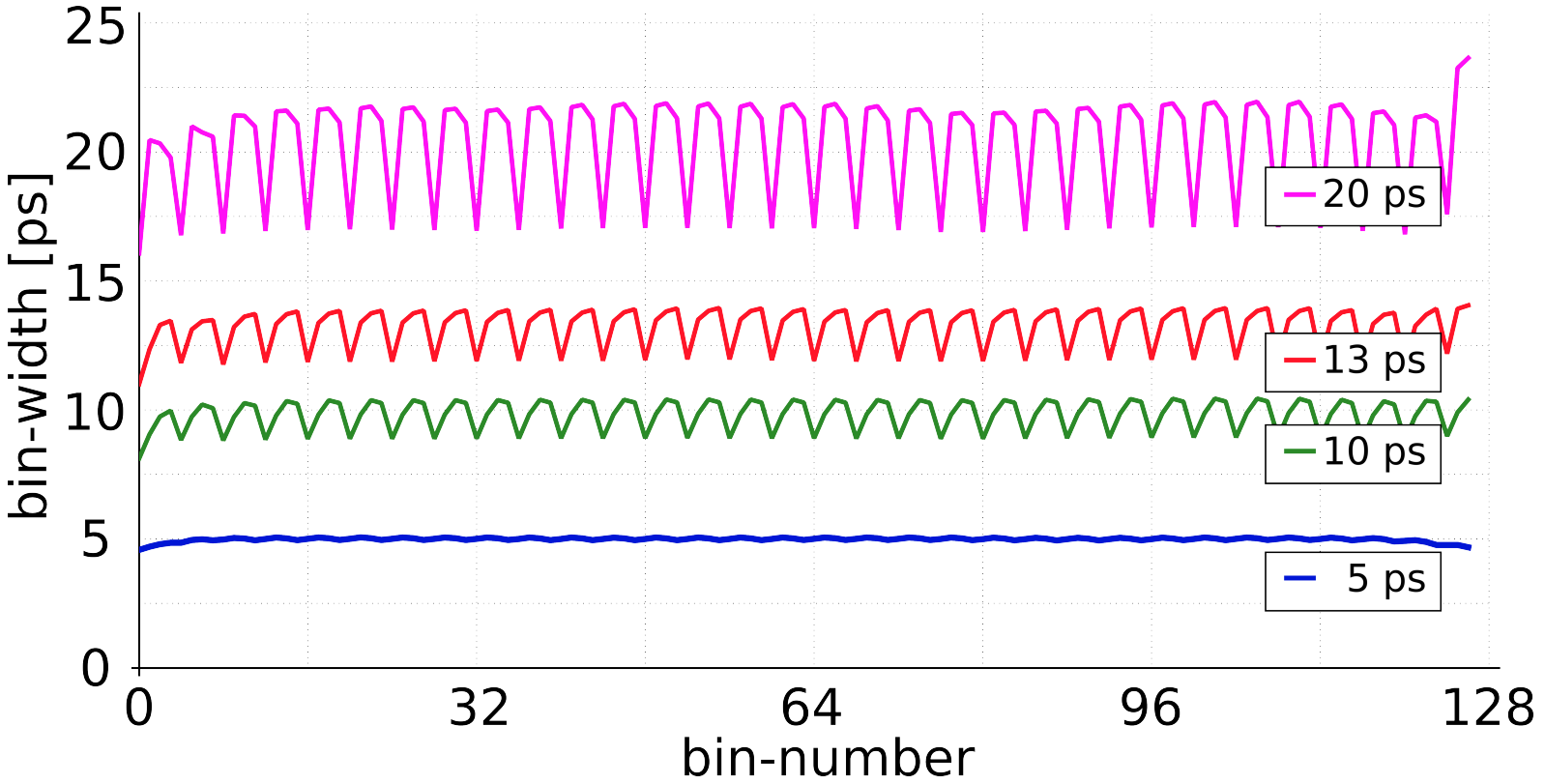
measured max. freq @ 1.2 V

REFCLK: **1.48 GHz**
-> 21/4 ps

little bit on the slow side

VDD = 1.3 V

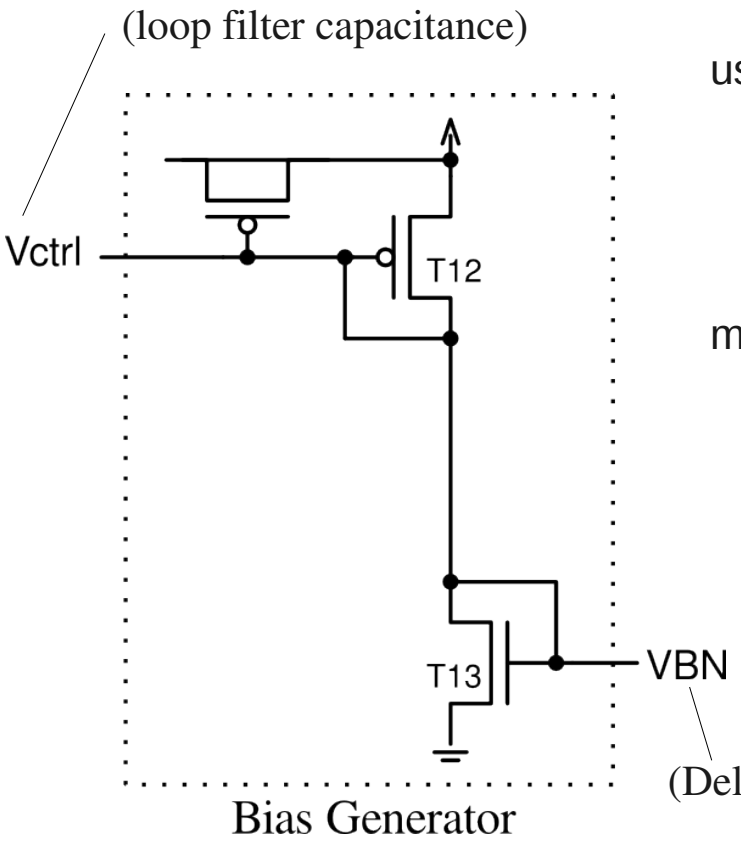
Simulated Bin-Widths



rms = 2.2 ps

rms = 0.1 ps

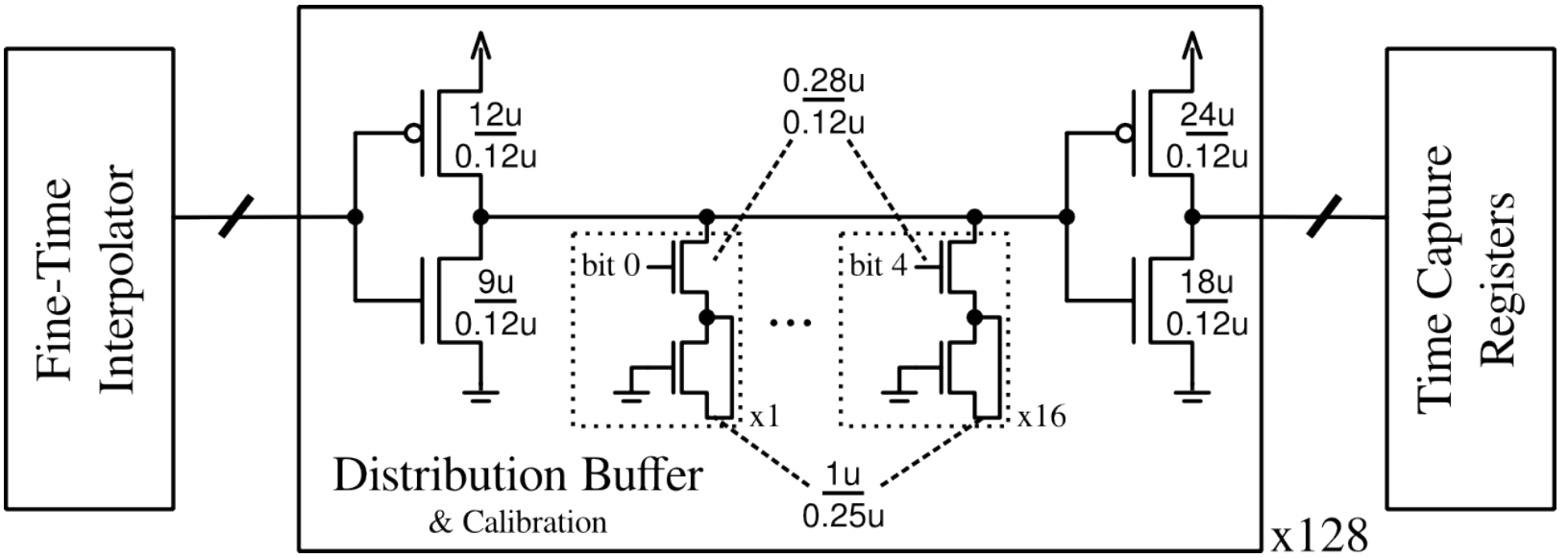
Delay Buffer Biasing



use simple bias to make use of big loop filter capacitance
-> most stable voltage in chip

main control on PMOS:
-> no strong arguments to control PMOS
instead of NMOS but ...
-> big intrinsic capacitive nodes on both controls
-> smaller gain at slower operation

Distribution Buffer w/ Calibration



- binary weighted calibration (5 bits)
- delay can be varied from -16 ps to +15 ps in 1 ps steps (2fF per step)
- can correct INL errors up to 6.4 LSB