AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Multichannel ADC for physics applications

Marek Idzik AGH-UST

Presented works done by:

M.Firlej, T. Fiutowski, Sz. Kulis, J. Moroń, D. Przyborowski, K. Świentek

Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

26 April 2013, CERN

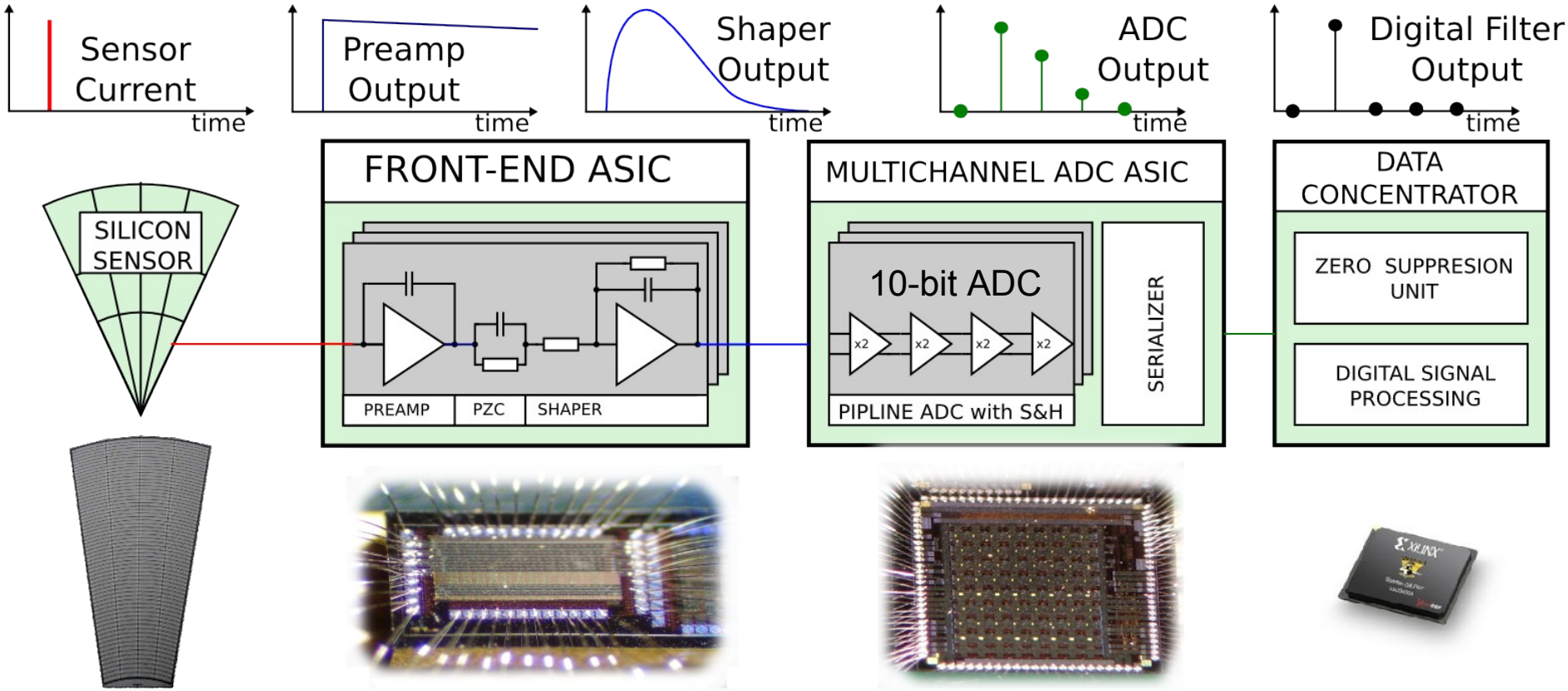
Outline

- Introduction and motivation
- ADC testing issues
- Multichannel digitizer in AMS 0.35 um
- Multichannel SAR ADC in IBM 130 nm
  - SAR architecture considerations
  - Design of 10(6)-bit SAR ADC
  - System level blocks (PLL, SLVS, ...)
- Preliminary tests of prototypes in IBM 130 nm
  - SAR ADC, PLL, SLVS
- Summary

ASIC group, infrastructure and activities at Faculty of Physics of AGH-UST

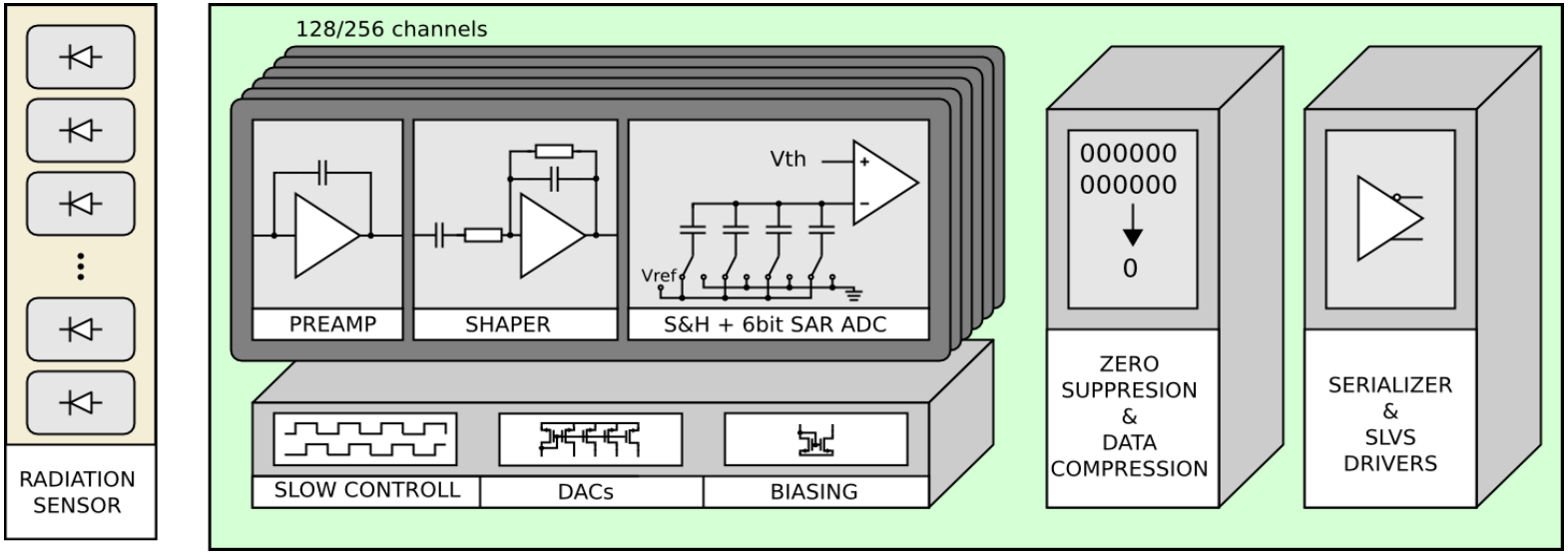
- People: staff 7, phd students 4, master students ~4
- Dedicated labs for microelectronics and detectors:
  - Clean-room class ISO6
  - Equipment: probe-stations (e.g.semi-automatic Cascade), bonder (F&K Delvotec 5330), semiconductor parameter analyzers (Agilent B1500A x 2, HP4145A), spectrum/signal anylezers (Agilent 4395A, N9030A), scopes up to 40GS/s (e.g. Agilent 90804A), generators (e.g. Agilent 81150A, 81160A), semiconductor lasers (Picoquant PDL 800-D with 660nm and 1060nm heads), radioactive sources, precise XYZ moving stages, High Voltage SMU (Keithley SMU237), RLC meters (e.g. Agilent E4980A)
  - Computer power for ASIC design: 2 servers DELL MD710HD (24 cores)+disc array MD3200i, 5 x very fast PCs for fast complex analyses, personal workstations
  - Software (>20 licenses): ASIC design (Cadence, Synopsis, Mentor Graphics), FPGA design (Xilinx), PCB design (Altium)
- Projects: ATLAS, **LHCb**, **ILC/CLIC**, PANDA, SOI, general microelectronics/detector R&D

Motivation
LumiCal detector readout electronics for ILC



- Present readout ASICs developed in CMOS AMS 0.35 um
- Development of new readout in CMOS IBM 130 nm in progress...

Motivation…
Multichannel readout ASIC for LHCb strip tracker



- Complex 128 channel ASIC
  - Preamplifier-shaper, 6-bit ADC, zero supp., serialization
  - Pitch ~40um
- CMOS IBM 130 nm technology
- Application in various detectors
  - TT tracker, VELO strip, IT tracker ?

"Fast" Multichannel 10-bit ADC Commercial and research solutions

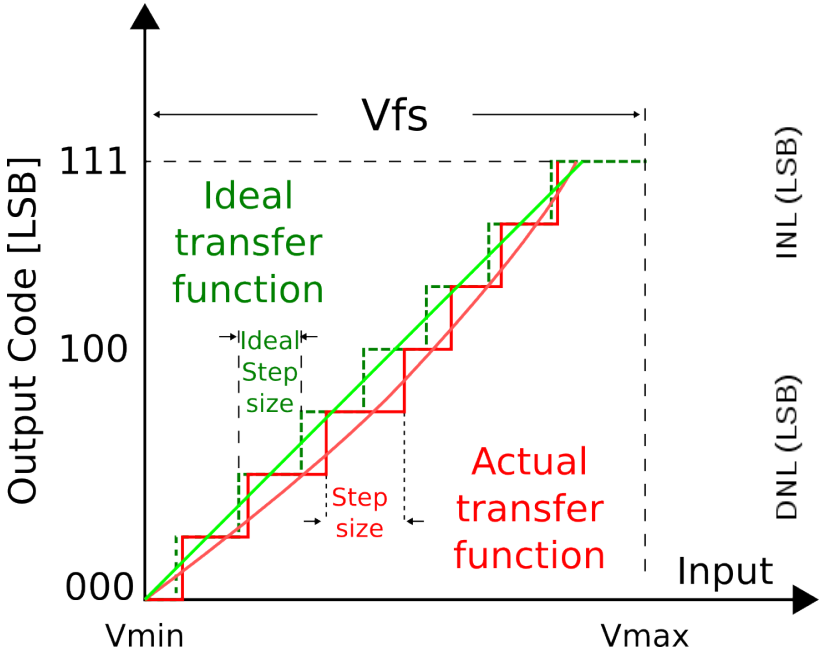
Parameter	Our work	K. Kavani et al ESSCIRC 2002	AD9212 AnalogDevices	ADS5287 TexasInstruments	MAX1434 Maxim
Nr of channels	8	8	8	8	8
Architecture	10-bit pipeline	10-bit pipeline	10-bit pipeline	10-bit pipeline	10-bit pipeline
Serialization	Per channel & per chip	Per chip	Per channel	Per channel	Per channel
Technology	0.35 µm CMOS	0.25 µm CMOS	-	CMOS	BiCMOS
Supply	3.3 V	2.5 V	1.8 V	3.3/1.8 V (A/D)	1.8 V
Max. f_{sample}	25MS/s	20MS/s	65MS/s	65MS/s	50MS/s
Input range	2Vpp	-	2 Vpp	2 Vpp	1.4 Vpp
Power/channel	~1.2mW/MS/s plus I/O (<15%)	41mW@20MS/s	100mW@65MS/s 68mW@40MS/s	74mW@65MS/s 46mW@30MS/s	96mW@50MS/s
Area	8.2 mm^2	4mm^2	9x9mm^2 (package)	9x9mm^2 (package)	14x14mm^2 (package)
INL	<0.68LSB	-	<0.5LSB	<1LSB	<1LSB
DNL	<0.62LSB	-	<0.4LSB	<0.55LSB	<0.5LSB
SINAD	~60.3dB	54.3dB	>=60dB	>=60.4dB	>=60dB
T_{power_ON}	<=10Tclk (~µs)	-	375µs	-	100ms

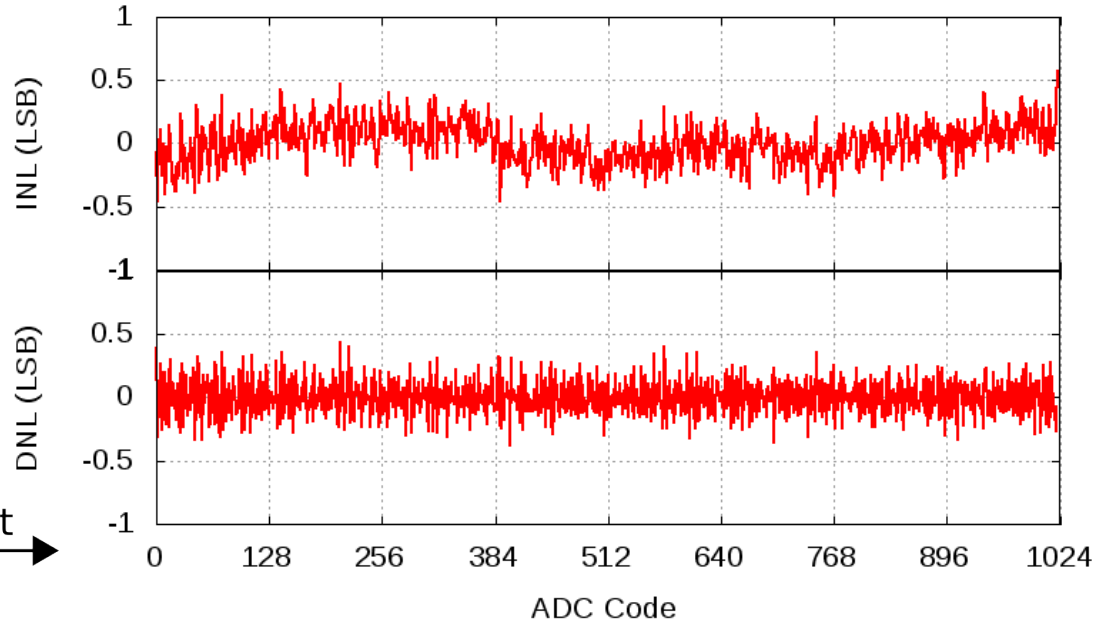
M. Idzik, K. Swientek, T. Fiutowski, Sz. Kulis, D. Przyborowski "A 10-bit multichannel digitizer ASIC for detectors in particle physics experiments", IEEE Trans. Nucl. Sci. v.59 p.294-302 2012

Outline

- Introduction and motivation
- **ADC testing issues**
- Multichannel digitizer in AMS 0.35 um
- Multichannel SAR ADC in IBM 130 nm
  - SAR architecture considerations
  - Design of 10(6)-bit SAR ADC
  - System level blocks (PLL, SLVS, ...)
- Preliminary tests of prototypes in IBM 130 nm
  - SAR ADC, PLL, SLVS
- Summary

ADC testing
Static measurements



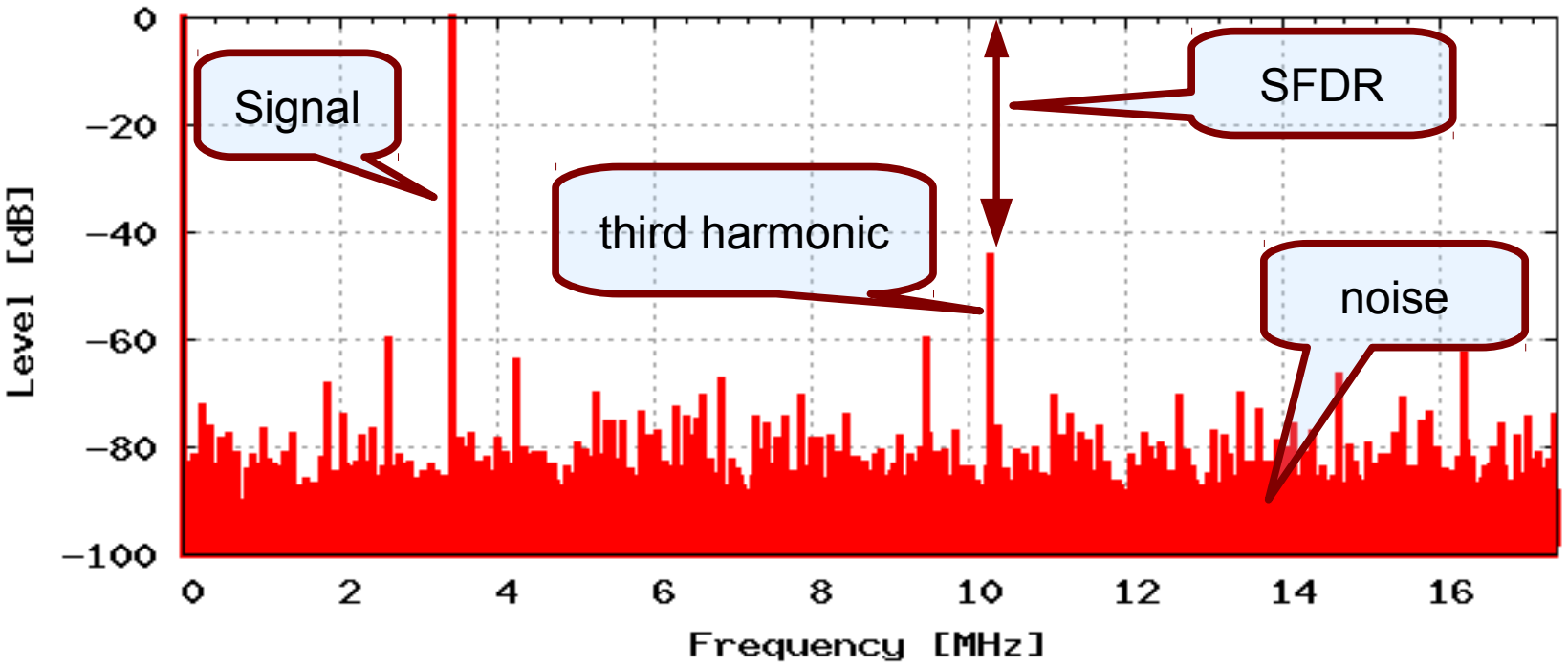


- **DNL** - Differential NonLinearity - the difference between an actual step width and the ideal step width
- **INL** - Integral NonLinearity - deviation of an actual transfer function from a straight line (integrated DNL)

ADC testing
Dynamic measurements

$$ENOB = \frac{SINAD[dB] - 1.76}{6.02}$$

- Single tone, full scale sine wave applied to input of the ADC
- Fourier Transform computed from the collected digital samples



- **SINAD** – Signal to Noise And Distortions
- **THD** – Total Harmonic Distortions
- **SFDR** – Spourious Free Dynamic Range
- **SNHR** – Signal to Non Harmonic Ratio

ADC testing/design
Resolution vs sampling clock jitter

$$V_{IN}(t) = V_A \times \sin(2\pi \times f_{IN} \times t)$$

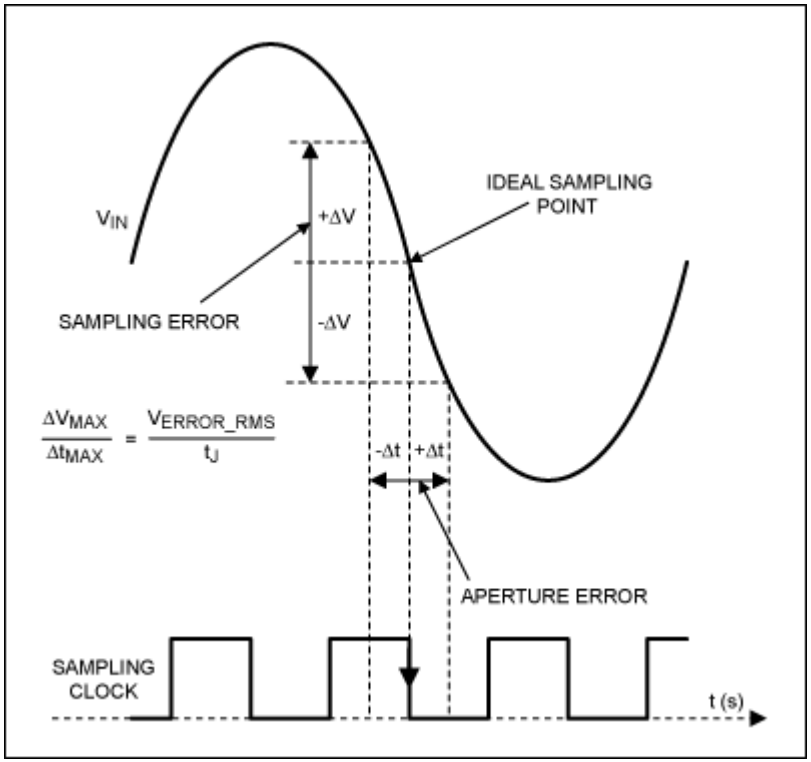
$$\frac{dV_{IN}(t)}{dt} = 2\pi \times f_{IN} \times V_A \times \cos(2\pi \times f_{IN} \times t)$$

$$\left.\frac{dV_{IN}(t)}{dt}\right|_{RMS} = \frac{2\pi \times f_{IN} \times V_A}{\sqrt{2}}$$

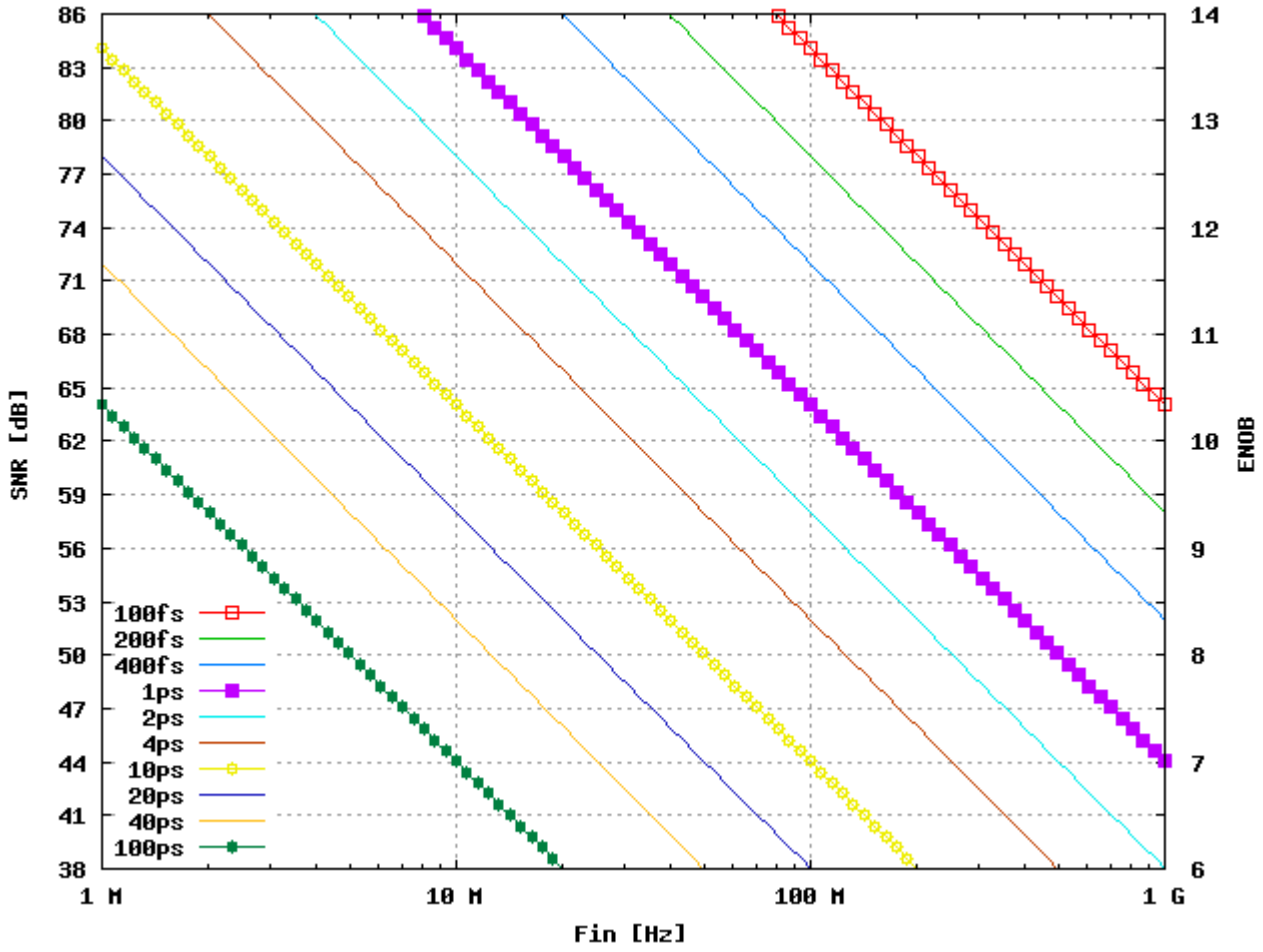
$$\frac{V_{ERROR\_RMS}}{t_J} = \frac{2\pi \times f_{IN} \times V_A}{\sqrt{2}}$$

$$V_{ERROR\_RMS} = \frac{2\pi \times f_{IN} \times V_A \times t_J}{\sqrt{2}}$$

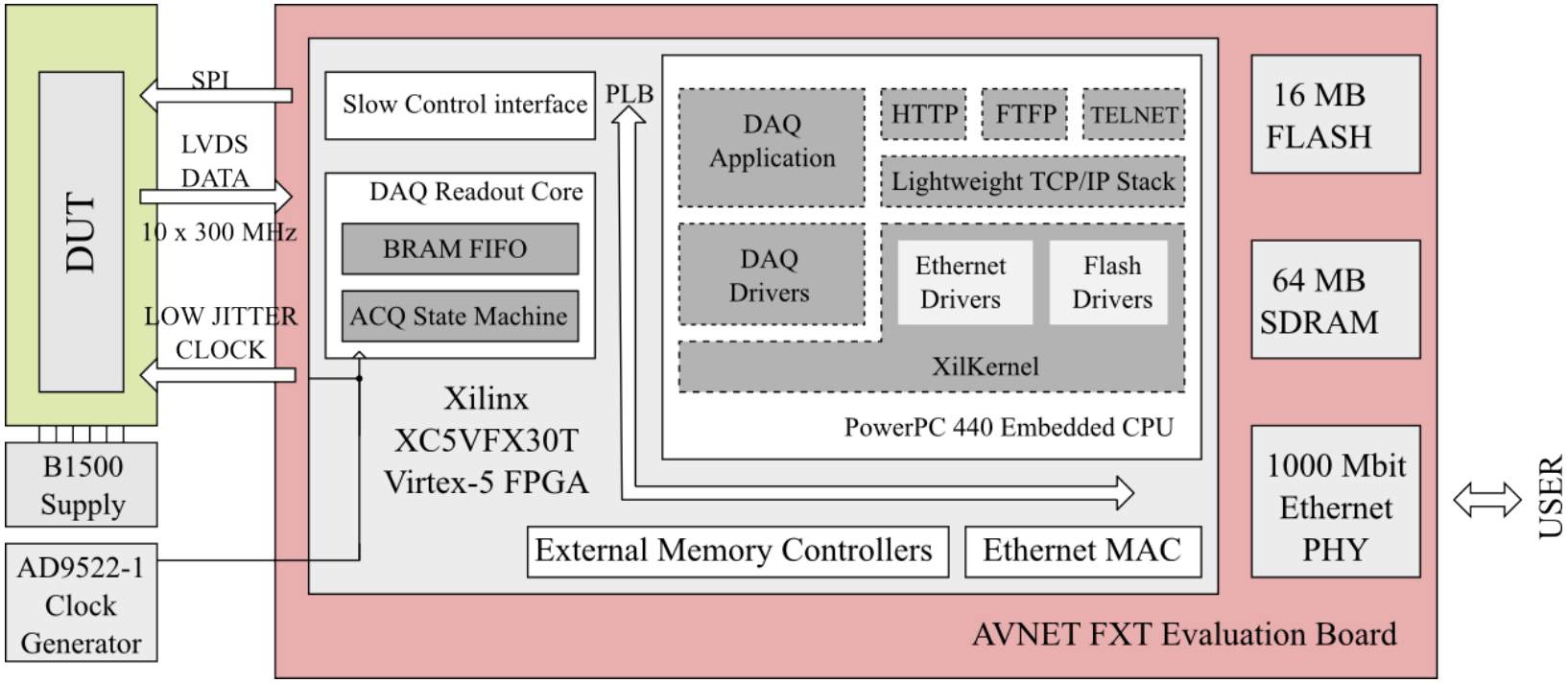
$$SNR = 20\log_{10}\left[\frac{V_{IN\_RMS}}{V_{ERROR\_RMS}}\right] = 20\log_{10}\left[\frac{V_A/\sqrt{2}}{2\pi \times f_{IN} \times V_A \times t_J/\sqrt{2}}\right]$$



ADC testing/design
Resolution vs sampling clock jitter...



ADC testing
FPGA based test setup



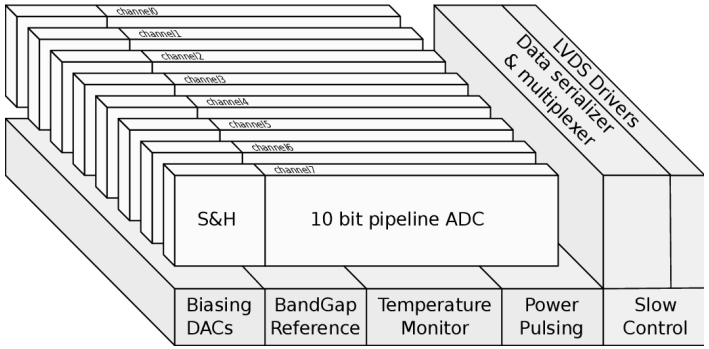
- Capturing data from ADC up to 300 MHz in LVDS standard
- AD9522 external PLL used to provide low jitter sampling clock (<10ps required !)
- Other instruments (power supplies- Agilent B1500A, signal generators- Agilent 81160A) controlled via GPIB/Etherhet by the supervising PC
- Fully automatic ASIC testing

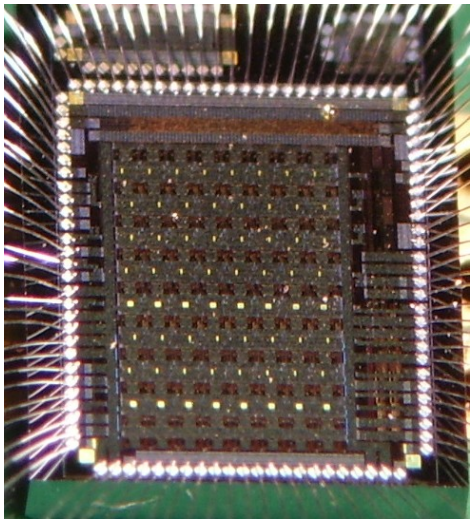
Outline

- Introduction and motivation
- ADC testing issues
- **Multichannel digitizer in AMS 0.35 um**
- Multichannel SAR ADC in IBM 130 nm
  - SAR architecture considerations
  - Design of 10(6)-bit SAR ADC
  - System level blocks (PLL, SLVS, ...)
- Preliminary tests of prototypes in IBM 130 nm
  - SAR ADC, PLL, SLVS
- Summary

Multichannel digitizer Architecture

- Specs&impleentation issues:
  - 8 channels of 10-bit pipeline ADC
  - Technology AMS 0.35um
  - Fully differential ADC
  - Layout with 200um ADC pitch
  - Multimode digital multiplexer/serializer:
    - Serial mode (~250MHz): one data link per all channels (max fsmp ~ 3 MSps)
    - Parallel mode (~250MHz): one data link per channel (max fsmp ~ 25 MSps)
    - Test mode: single channnel output (max fsmp ~50 MSps)
  - High speed LVDS interface (~1GHz)
  - Bootstrapped S/H switches
  - Power pulsing
  - Low power DACs for internal settings
  - BandGap reference source
  - Temperature sensor

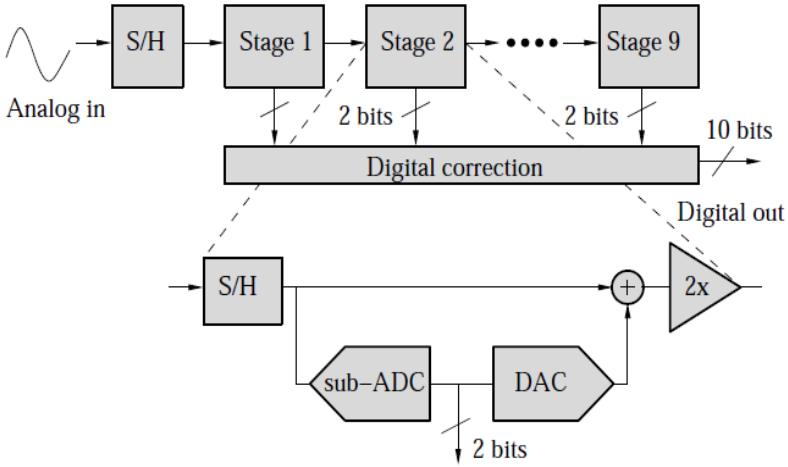


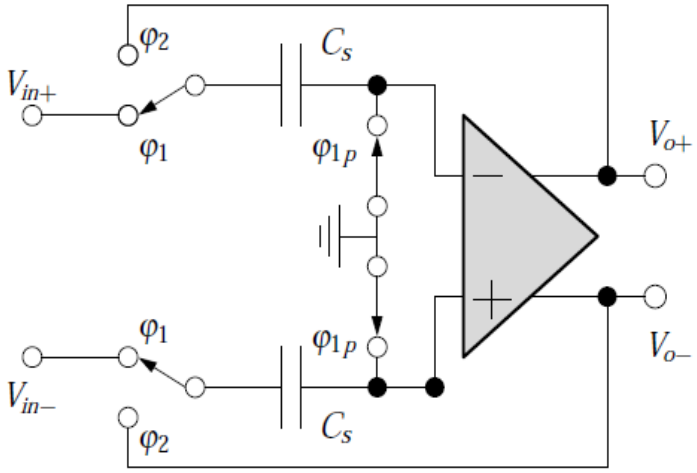


2.6mm x 3.2mm

Three submissions were done (two to develop core ADC) to get final chip

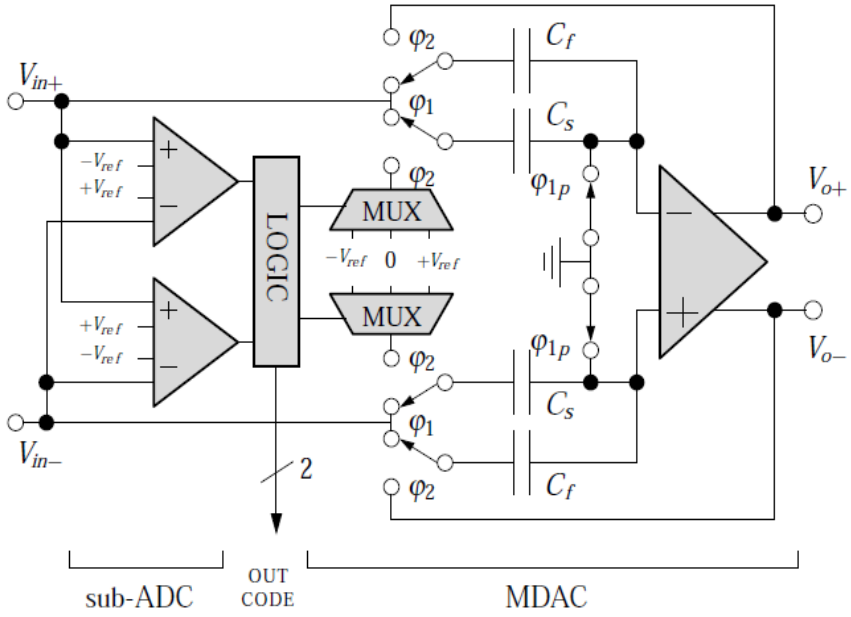
Multichannel digitizer
10-bit pipeline ADC





S/H stage

- High throughput - conversion rate = clock rate
- 1.5 bit per stage - redundancy reduces comparator requirements
- Fully differential architecture

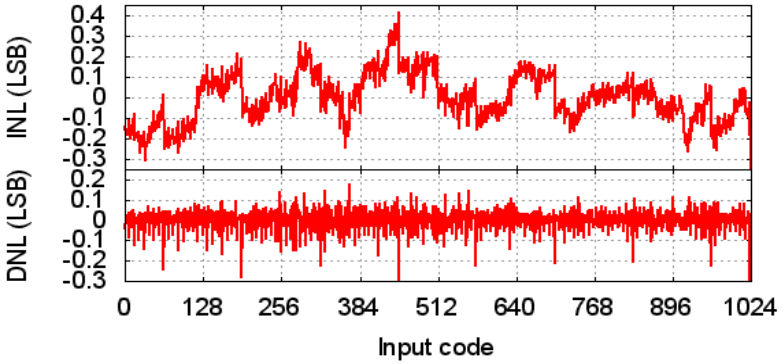


1.5 bit pipeline stage

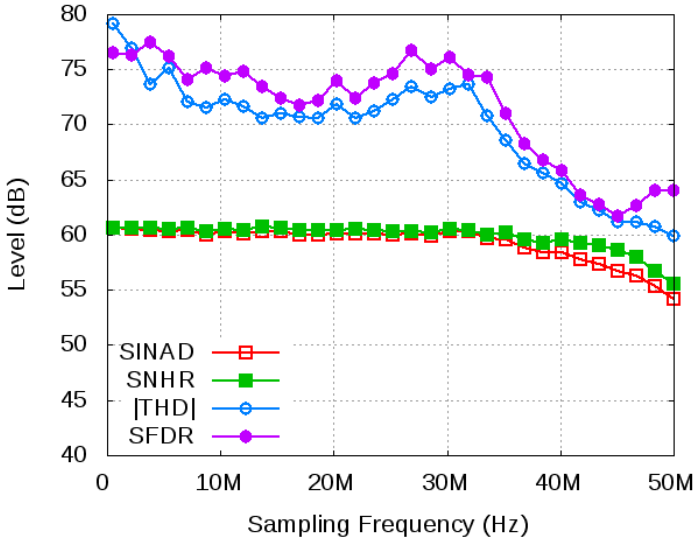
Multichannel digitizer Performance

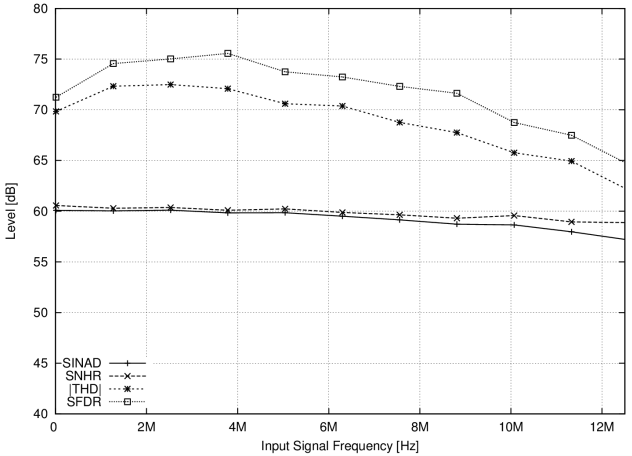
- Performance
  - ENOB=9.7 up to 25 Ms/s (8 channels)
  - INL<0.68, DNL<0.62
  - Sampling rate up to ~25MS/s (multichannel) or up to ~50MS/s (single channel)
  - Power scales linearly with sampling rate ~1.2mW/channel/MHz (without power pulsing)

Static measurements

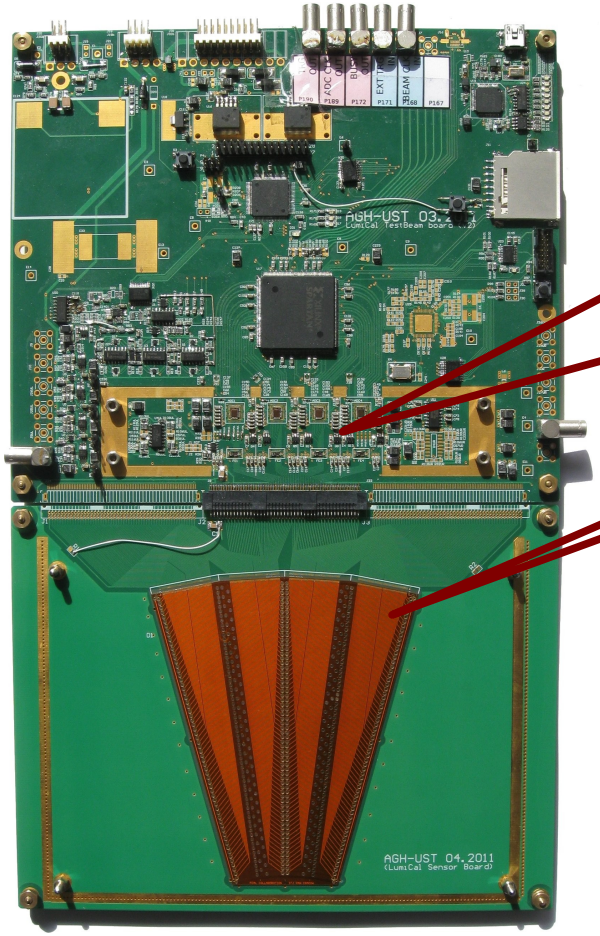


Dynamic measurements

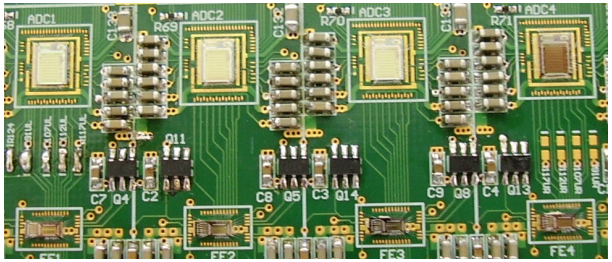




Multichannel digitizer in LumiCal detector



4 pairs of Front-end + ADC



Sensor

- LumiCal detector module with 32 fully equipped channels (Front-end +ADC ASICs) plus FPGA data concentrator is regularly used during FCAL Collaboration test-beams

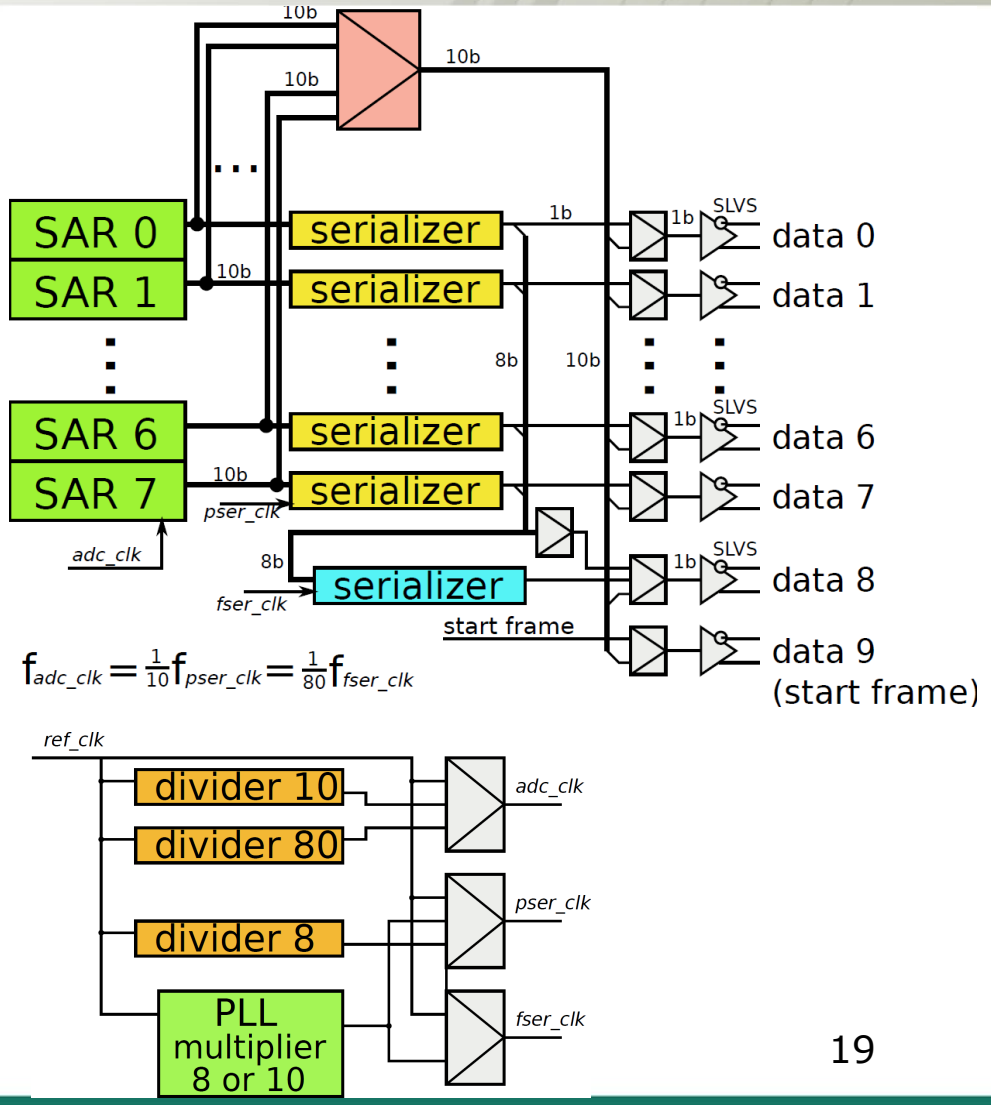
Outline

- Introduction and motivation
- ADC testing issues
- Multichannel digitizer in AMS 0.35 um
- **Multichannel SAR ADC in IBM 130 nm**
  - **SAR architecture considerations**
  - Design of 10(6)-bit SAR ADC
  - System level blocks (PLL, SLVS, ...)
- Preliminary tests of prototypes in IBM 130 nm
  - SAR ADC, PLL, SLVS
- Summary

Design of SAR multichannel ADC

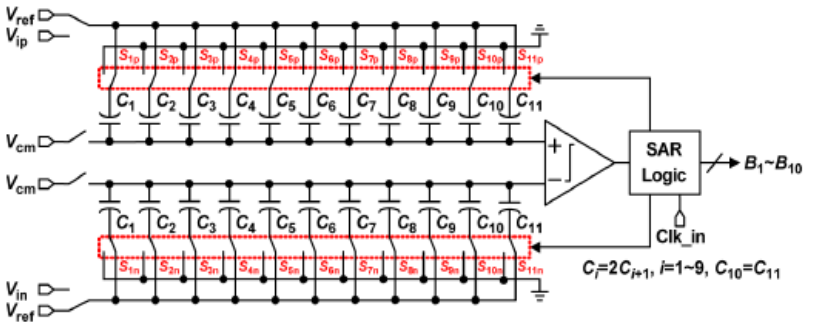
Specifications & implementation issues:

- 8 channels of 10-bit (6-bit) SAR ADC
- Technology IBM 130 nm
- Layout with 146um (40um) ADC pitch
- Multimode digital multiplexer/serializer:
  - Serial mode: one data link per all channels (external clk division or PLL clk generation)
  - Parallel mode: one data link per channel (external clk division or PLL clk generation)
  - Test mode: single channnel output (max fsmp ~50 Msps)
- PLL for data serialization
- High speed SLVS interface (~1GHz)
- Power pulsing
- Generation of short sampling pulse
- Bootstrapped S/H switches
- Voltage reference not yet addressed...
- SingleEnded-to-Differential converter ??



SAR ADC motivation
General features & design considerations

- Power and area-efficient architecture – the same circuitry is used N-times (for N-bit ADC) to approximate the input voltage
- Only one comparator, two DACs and SAR logic needed – fits well to modern digital CMOS
- Limited sampling rates - but with modern CMOS technology (~100nm) up to ~100MSps 10-bit ADCs were reported
  - next conversion cannot be started before completion of previous one
  - sampling time adds to conversion time (not like in pipeline)

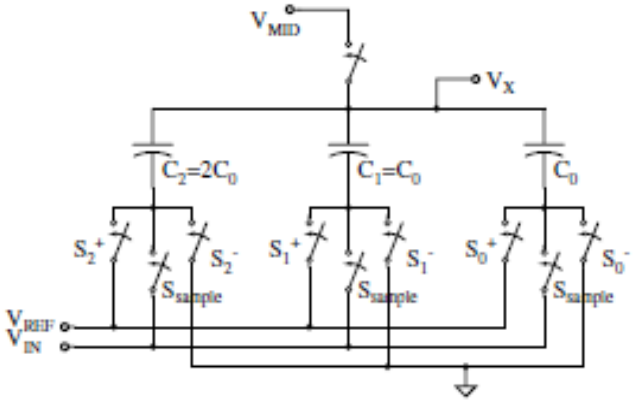


- Comparator – the only analog block
- DAC network serves as sampling capacitance
- Simple digital logic
- Fully differential implementation increases the resistance to disturbances

Why various SAR configurations ? Switching energy

- With CMOS technology scaling digital power consumption is decreasing rapidly - so minimizing analog power (DAC, comparator) is of main interest
- Huge progress has been obtained in the last ~10 years in optimizing capacitive DAC configurations and their switching schemes
- Various DAC switching configurations were proposed
  - Conventional (100% power consumption)
  - 2 step switching (~10% power saving)
  - Charge sharing (~24% power saving)
  - Split capacitor (~37% power saving)
  - Energy saving (~56% power saving)
  - Set and down (~81% power saving)
  - Vcm-based (~87% power saving)
  - Merge Capacitor Switching (MCS) (~93% power saving)
  - Last half year some new were proposed (up to ~98% power saving)

Switching energy – principle
2-bit capacitor array example

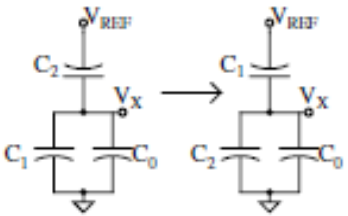


Energy drawn from Vref: $E=V_{ref} * \Delta Q$

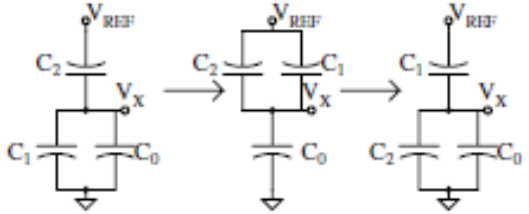
"up" transitions – S_i short to V_{ref}

"down" transitions - S_i short to gnd

1. S_2 "up" transition: $E=C_0V^2_{ref}$
2. If $V_{in}>V_{ref}/2$ then S_1 goes "up": $E=C_0V^2_{ref}/4$, otherwise S_1 goes "down":



Conventional switching: $E=5C_0V^2_{ref}/4$



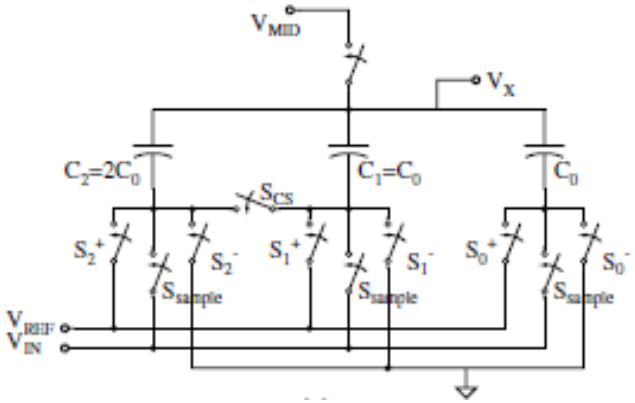
2 step switching: $E=3C_0V^2_{ref}/4$

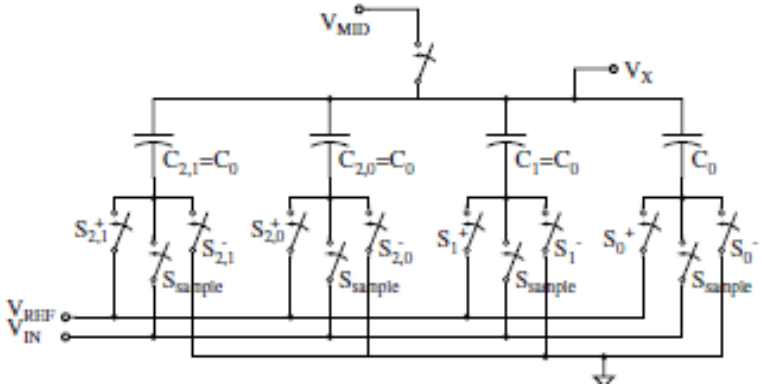
"down" transitions consume much power...

B. P. Ginsburg, A.P.Chandrakasan "An Energy-Efficient Charge Recycling Approach for SAR Converter With Capacitive DAC", IEEE Int. Symp. On Circuits and Systems, May 2005 pp. 184-187

Switching energy – principle
2-bit capacitor array example...

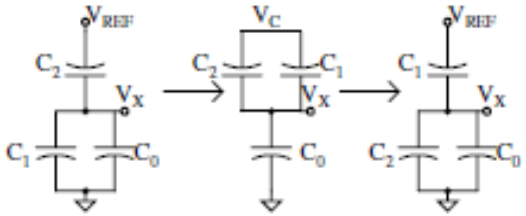
There are other ways to perform “down” transitions:

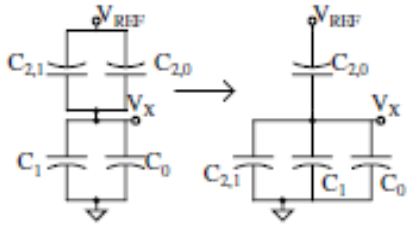




Charge sharing: $E=7C_0V^2_{ref}/12$

Split capacitor: $E=C_0V^2_{ref}/4$

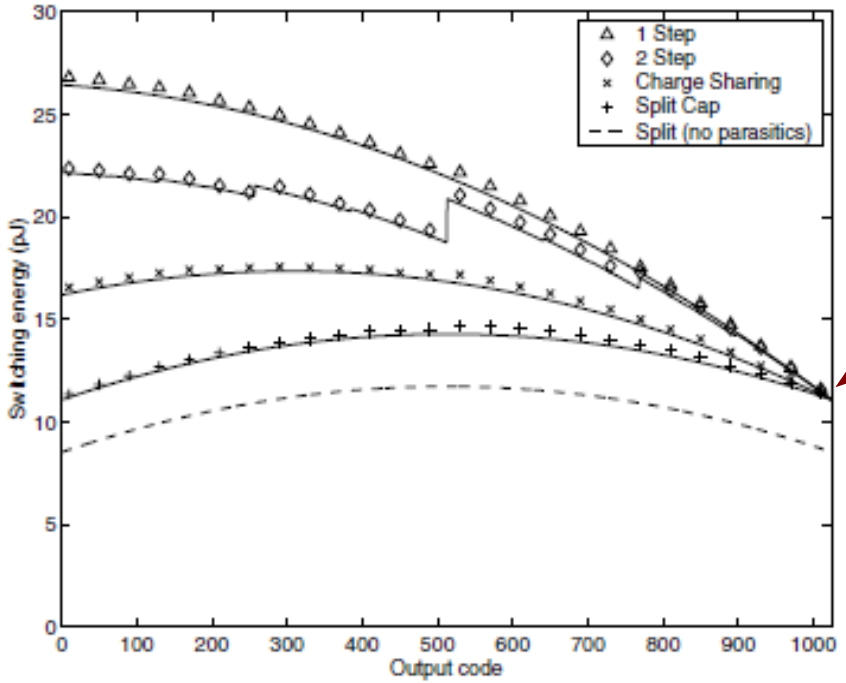




Switching scheme may be optimized to save power in “down” transitions!

Switching energy
Comparison of simple schemes

Switching energy versus output code

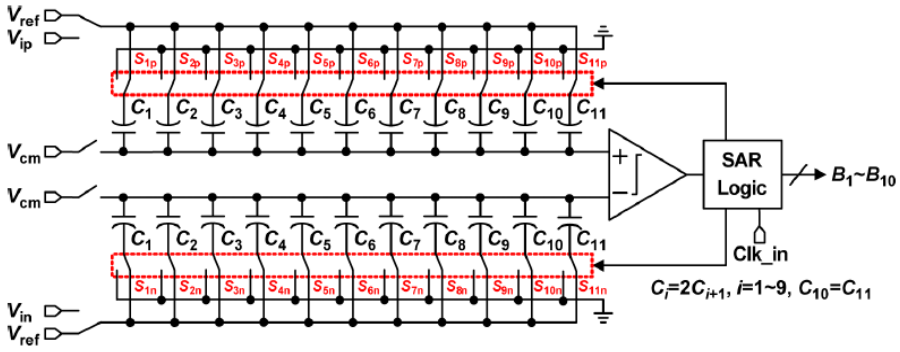


only “up” transitions

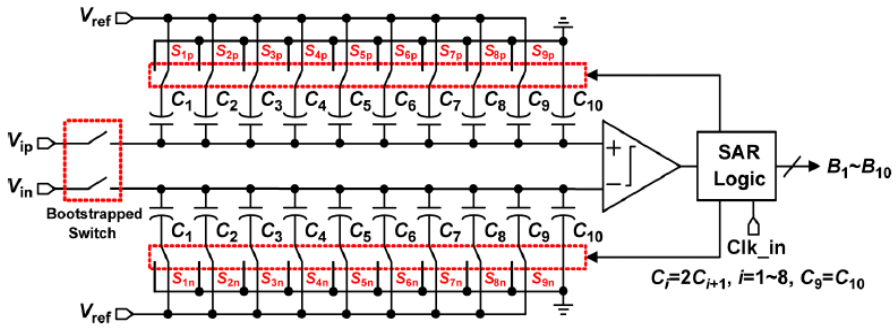
Hspice points vs Matlab model (*from Ginsburg paper*)

Switching energy – more efficient configurations
Set and down vs conventional

Conventional 10-bit SAR

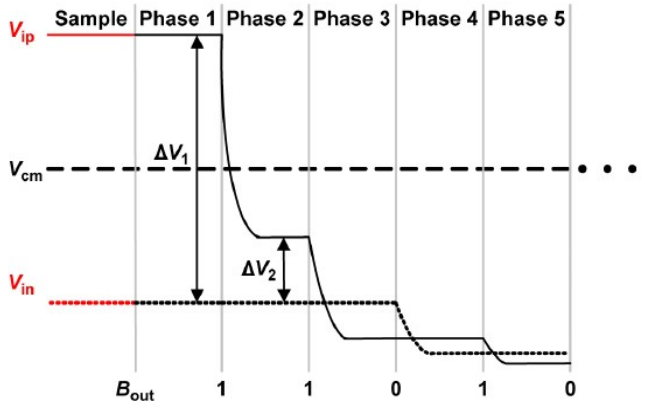


Set and down 10-bit SAR



Set and down SAR ADC:

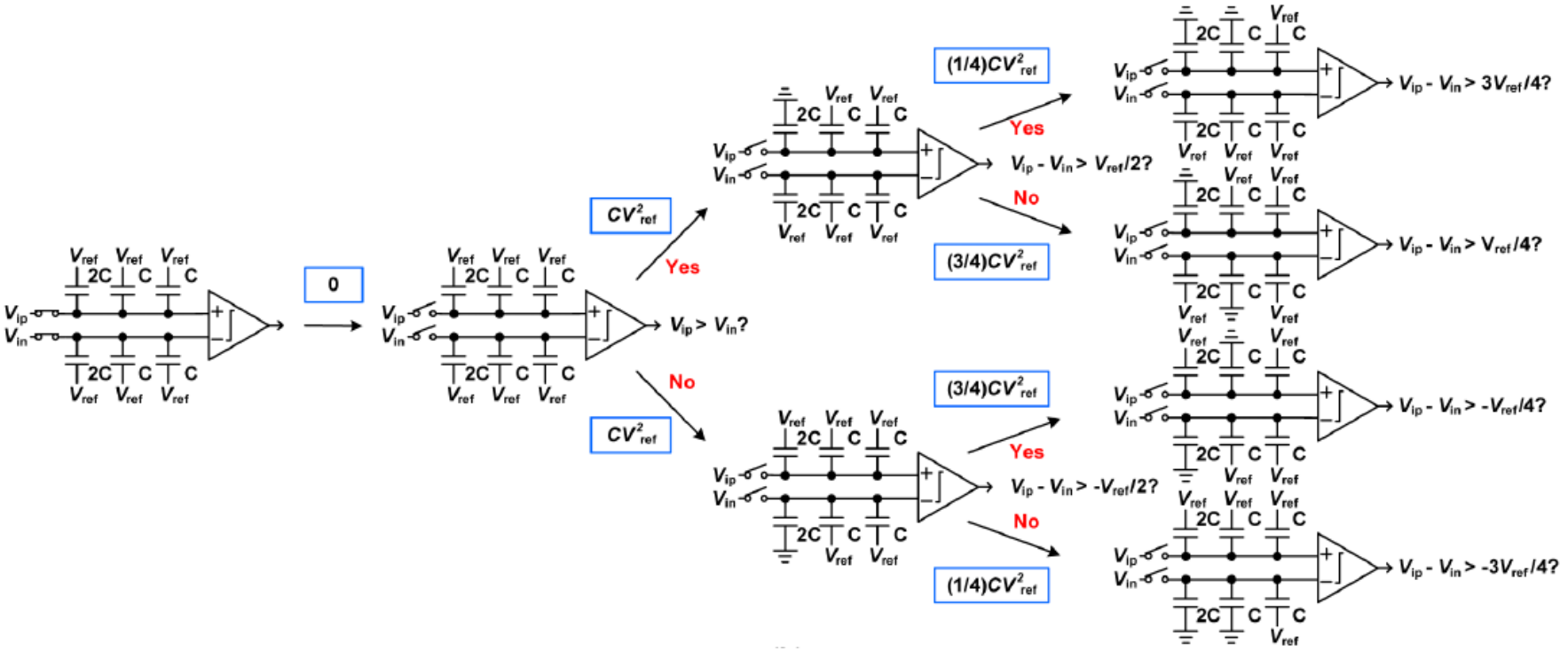
- pair of MSB capacitors less
- V_{in} sampled on top plate
- 1st comparsion done before any switching



Variable common mode...

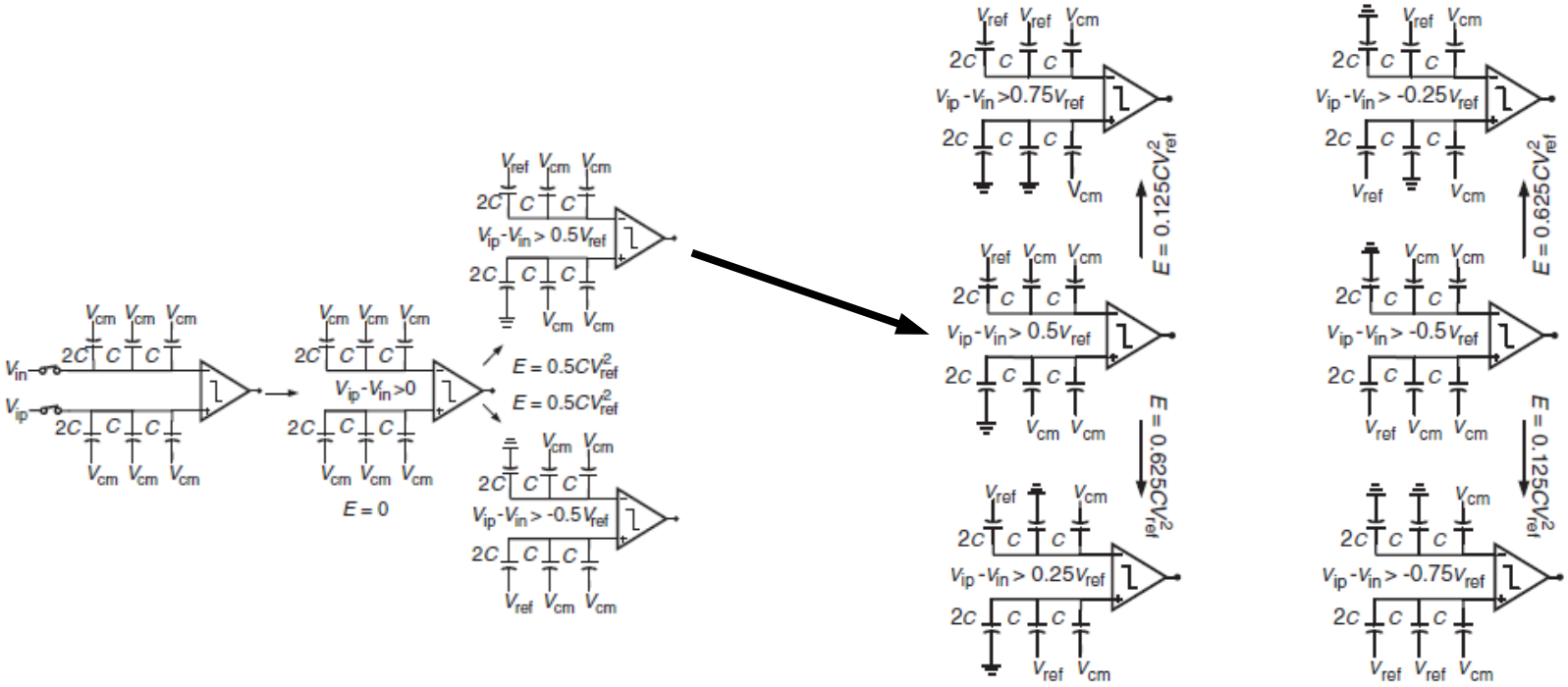
Ch. Ch. Liu, S-J. Chang, G-Y.Huang, Y-Z. Lin "A 10-bit 50MS/s SAR ADC with a monotonic capacitor switching procedure", IEEE Journal of Solid-State Circuits v.45 pp. 731-740, April 2010

Switching energy – more efficient configurations
Set and down 3-bit SAR ADC example



Switching energy ~81% less than conventional SAR ADC

Switching energy – more efficient configurations
Merge Capacitor Switching (MCS) SAR ADC

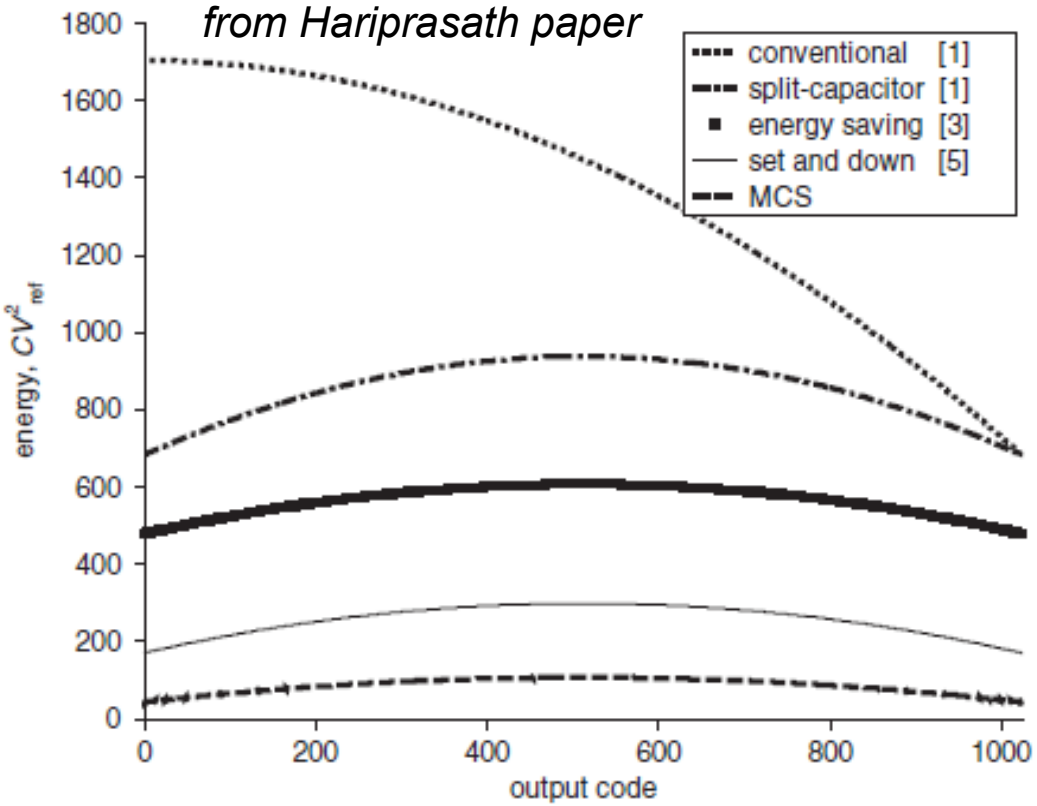


Switching energy ~93% less than conventional SAR ADC

Such switching scheme is used in our present design

V. Hariprasath, J. Guerber, S-H. Lee, U-K. Moon "Merged capacitor switching based SAR ADC with highest switching energy-efficiency", Electronics Letterss v.46 No.9 April 2010

SAR switching energy
Merge Capacitor Switching (MCS)...



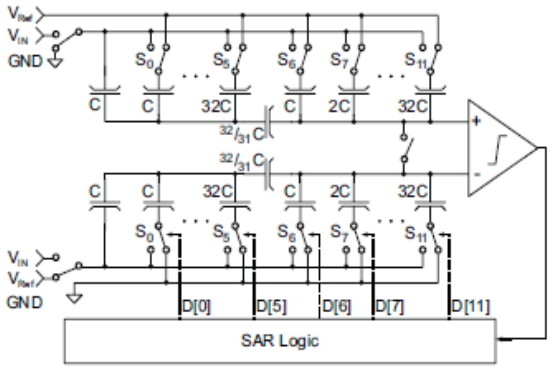
Within last ~half year new papers with even more efficient schemes were published...

Outline

- Introduction and motivation
- ADC testing issues
- Multichannel digitizer in AMS 0.35 um
- **Multichannel SAR ADC in IBM 130 nm**
  - SAR architecture considerations
  - **Design of 10(6)-bit SAR ADC**
  - System level blocks (PLL, SLVS, ...)
- Preliminary tests of prototypes in IBM 130 nm
  - SAR ADC, PLL, SLVS
- Summary

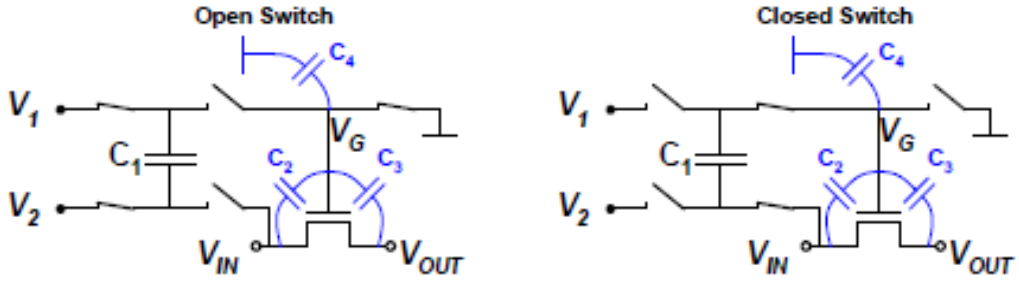
Design of SAR ADC
Implementation issues

- Split DAC architecture
  - allows using higher unit capacitance for the given total DAC capacitance. It helps to bypass the problem of relatively high C_{min} available in CMOS technologies – allows to decrease the effective "LSB capacitance" and so power consumption
- Asynchronous logic
  - no fast clock needed for bit cycling
  - only sampling pulse needed for digital control
  - sampling pulse (trigger) does not need to be periodic
- Dynamic comparator
  - alows to obtain zero static power consumption and so "power pulsing" is given for freel
- Bootstrapped sampling switch
  - improves ADC linearity

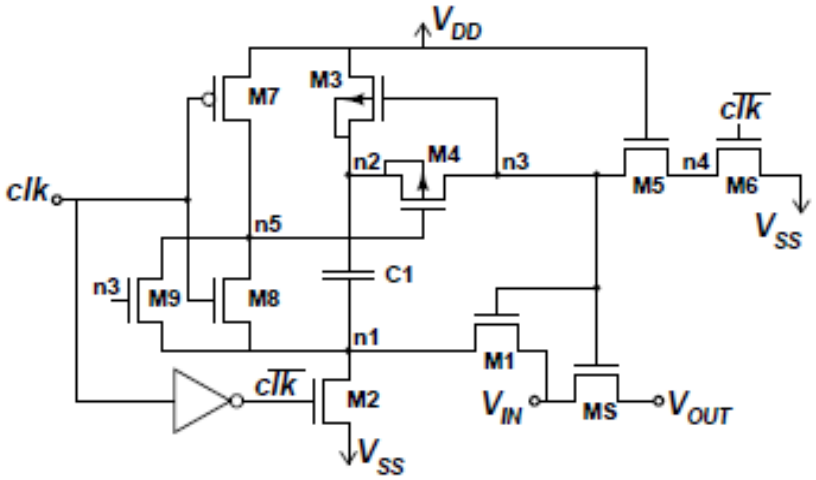


Design of SAR ADC
Bootstrapped S/H switch

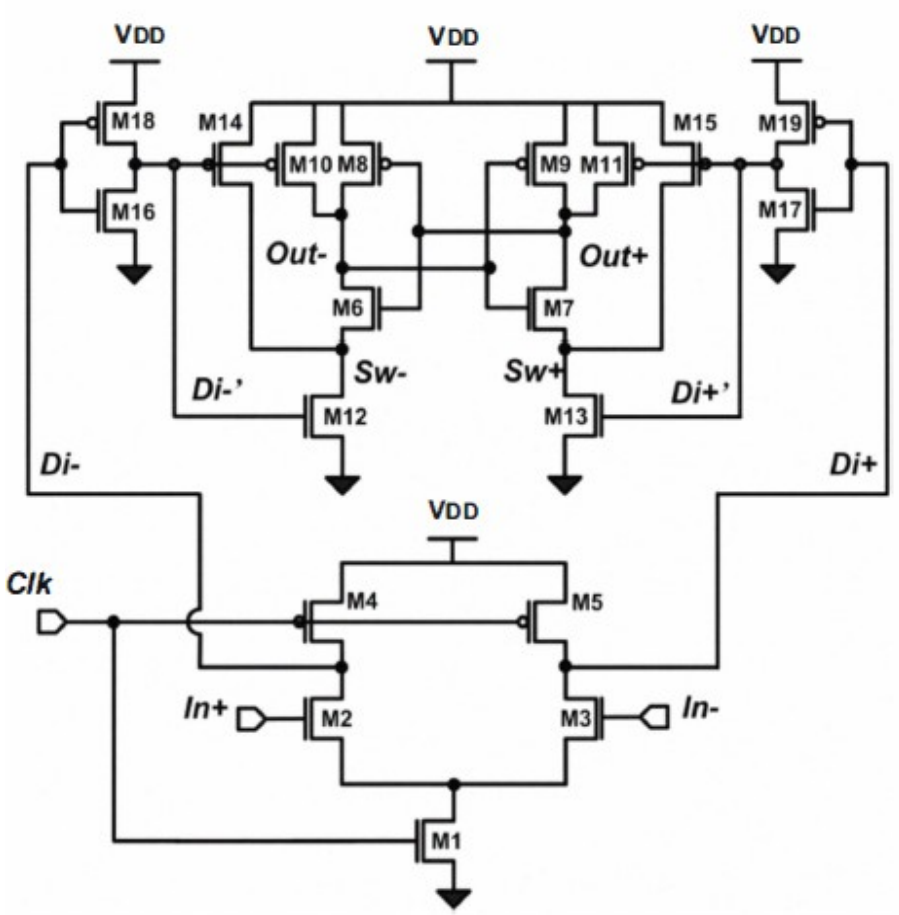
Idea



Implementation



Design of SAR ADC
Dynamic comparator



H.J. Jeon, Y-B. Kim, M. Choi "Offset voltage analysis of dynamic latched comparator", IEEE 54th Int. Midwest Symp. On Circuits and Systems, 2011

Design of SAR ADC – DAC capacitors
Noise and matching considerations

Noise

Thermal switch noise of sampling circuit – kT/C

$kT/C < \sigma^2/12$

$kT/C < (V_{ref}/2^N)^2/12$

$C > 12\ kT\ (2^N/V_{ref})^2$

For V_{ref}=1 V:

N=6 bits C > 0.2 fF

N=8 bits C > 3.3 fF

N=10 bits C > 52 fF

N=12 bits C > 830 fF

Switch noise is negligible

Matching

VNCAP M1-M2 ~0.4fF/um^2

MIMCAP ~2fF/um^2

Mis-match % (3σ)

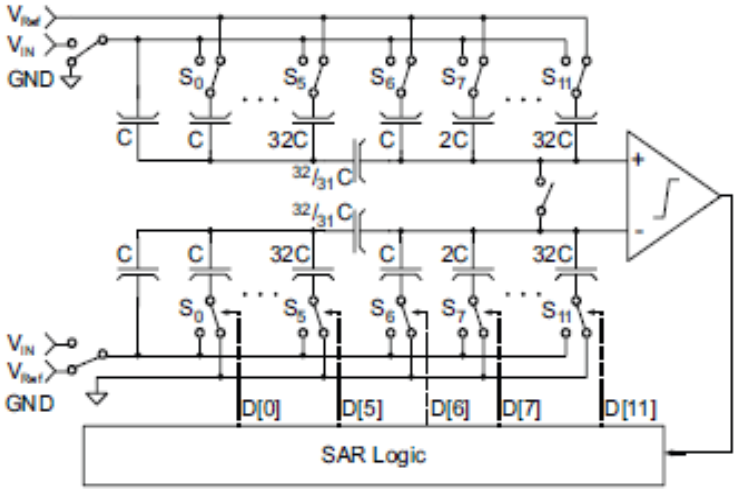
VNCAP 10x20 um^2 (~80fF) ~5%

MIMCAP 6x7 um^2 (~80fF) ~0.7%

MOM – no model exist, matching unknown...

MIMCAP has high density and good matching

Design of 10-bit SAR in IBM 130nm



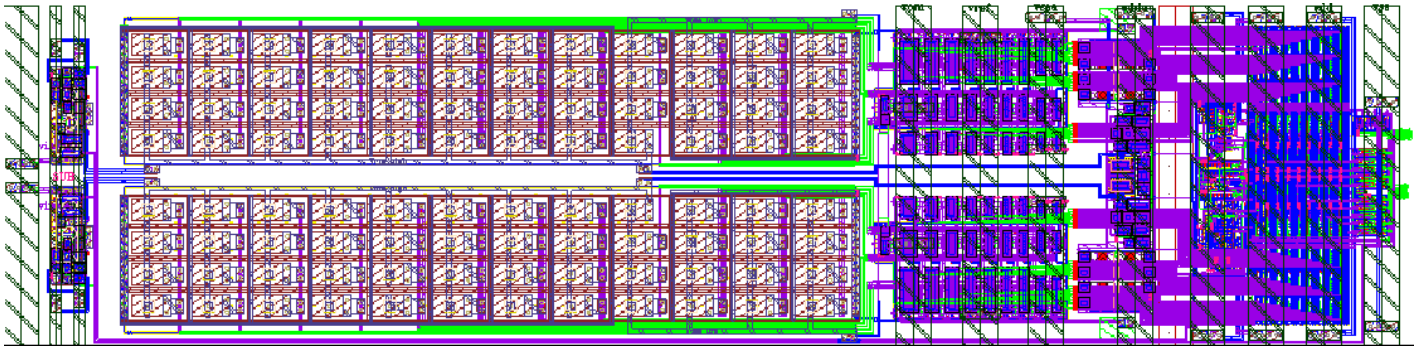
Designs of 10-bit ADC

- Architecture: SAR ADC with segmented/split DAC
- Asynchronous SAR logic – No-bit clk
- Scalable frequency (up to ~50 MS/s) and power consumption
- 1-2mW at 40MS/s
- 146um pitch
- Fabricated in 2012 (2 prototypes)

Design of 6-bit ADC

- Architecture: SAR ADC with segmented/split DAC
- Asynchronous SAR logic – No-bit clk
- Scalable frequency (up to ~100 MS/s) and power consumption
- ~300uW at 40MS/s
- 40um pitch
- Fabricated in 2012

Design of 10-bit SAR in IBM 130nm

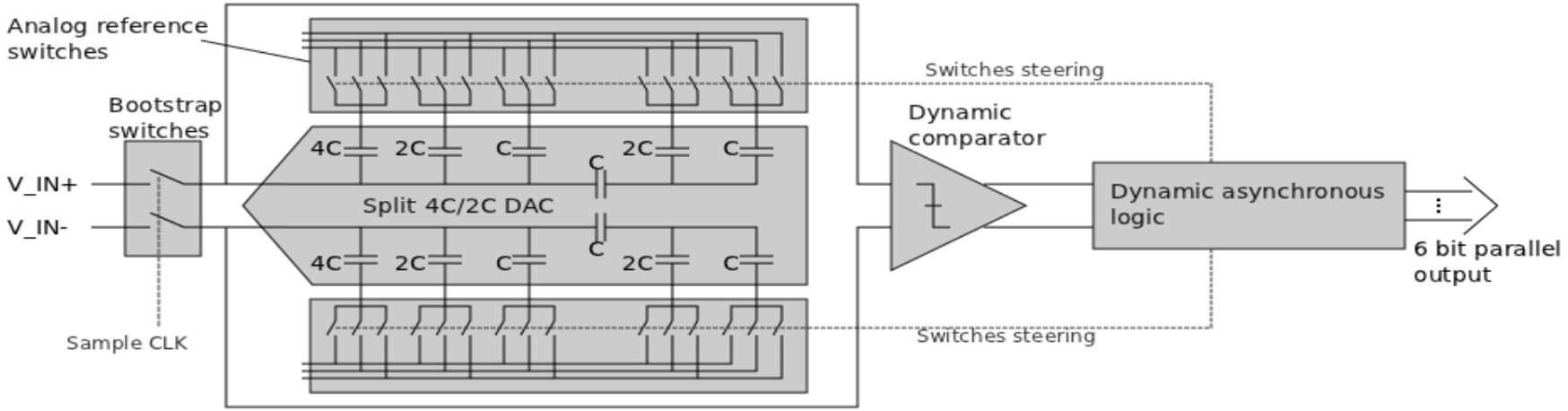


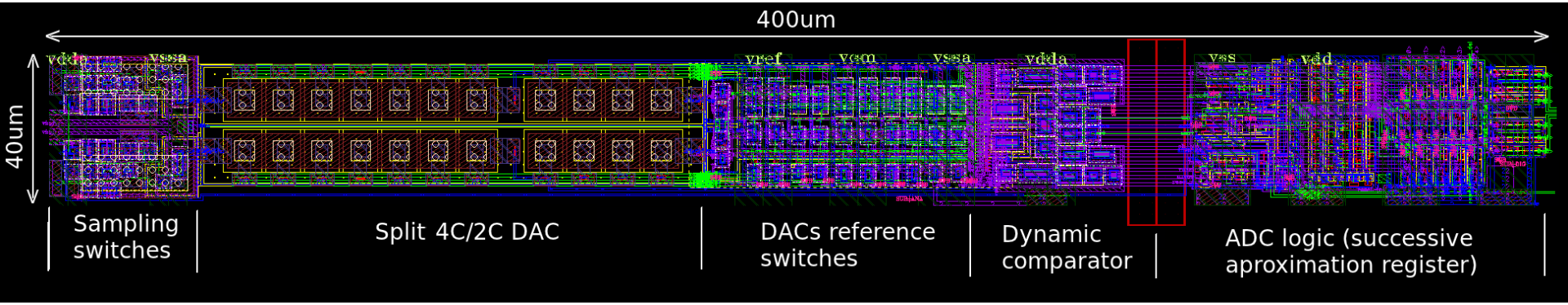
SAR DAC channel 600um x 146um

Two slightly different designs in IBM 130 nm submitted

- Simulated ENOB ≈ 9.5-9.7 bits
- Maximum sampling rate ~50 MS/s
- Power consumption ≈ 1-1.4mW @ 40 MS/s
- Slightly different DAC capacitance splitting in 2 prototypes
- No dummy capacitors in DAC network!

Design of 6-bit SAR ADC in IBM 130 nm

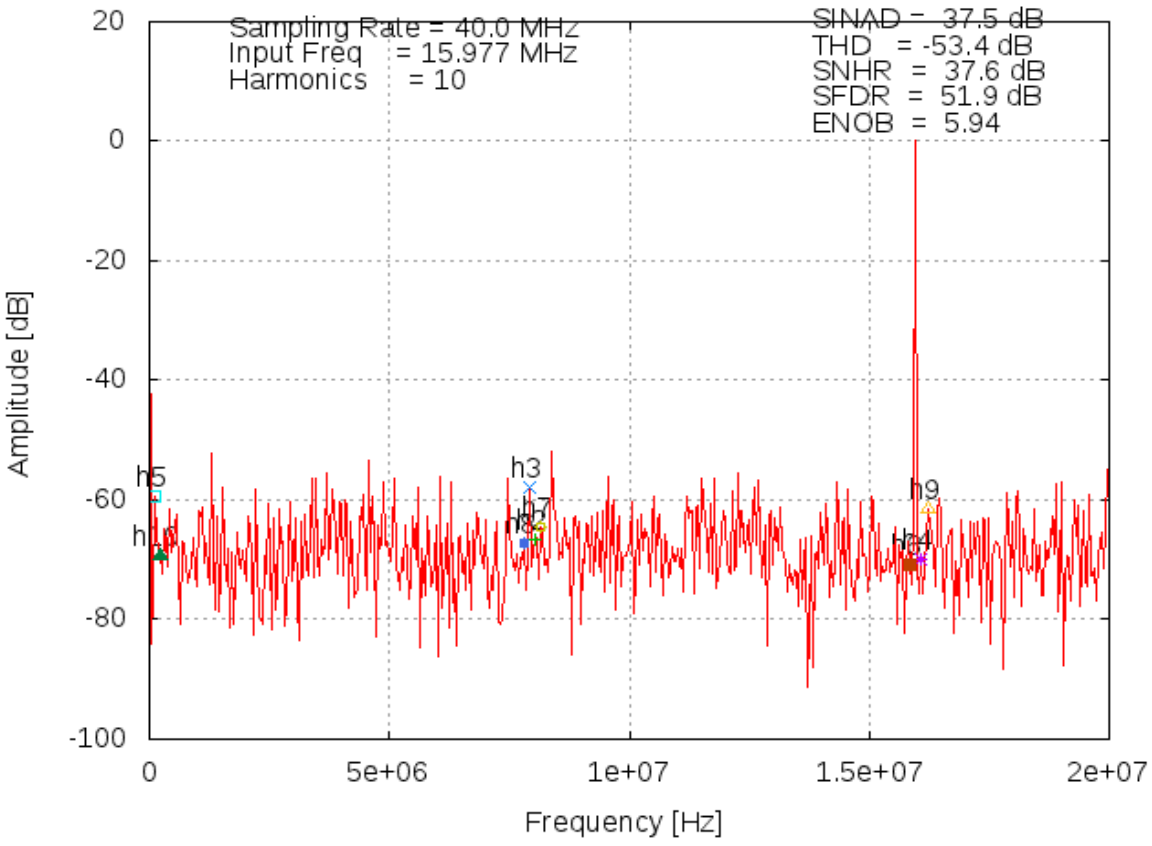




- Single channel: 40um x 400um (area 0.016 mm^2)
- Custom capacitor p-cell layout done to obtain 40um pitch

Simulation of 6-bit SAR ADC
Example of dynamic performance

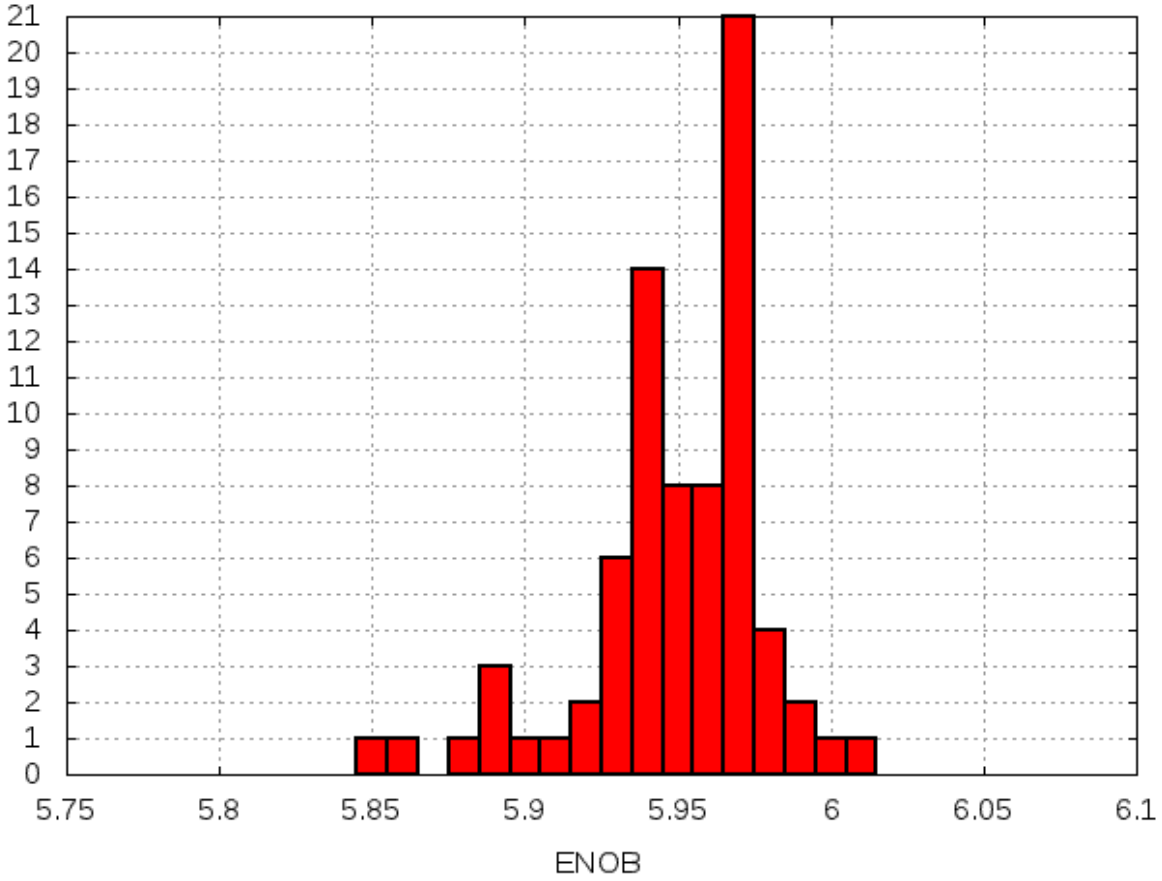
Dynamic parameters obtained from discrete Fourier analyses of 1024 samples of input sine wave.



Post-layout simulation results at 40MS/s:

- SINAD ≈ 37.5 dB
- ENOB ≈ 5.94 bits

Simulation of 6-bit SAR ADC
Example of Monte-Carlo mismatch analysis



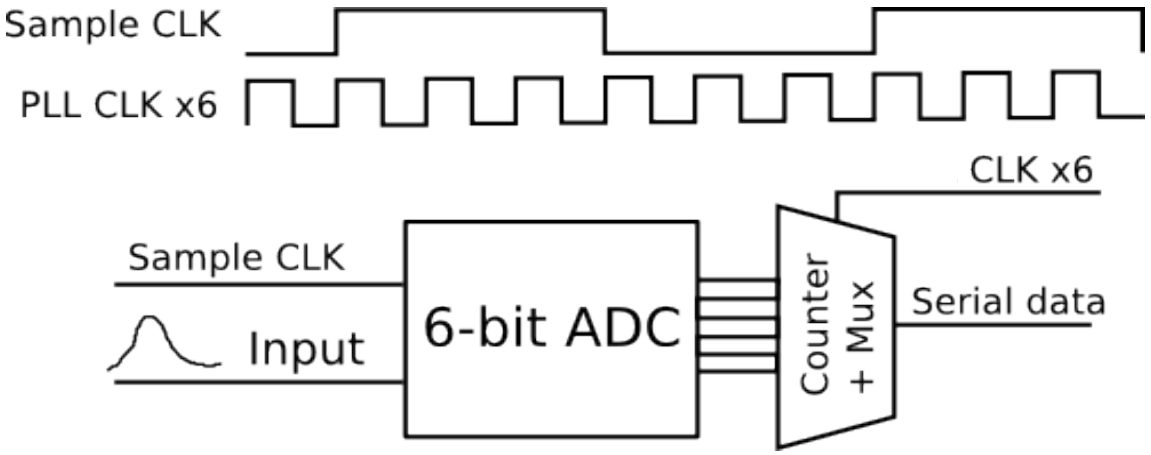
Simulation performed 100 times

ENOB always above 5.8 bits, average 5.95 bits

Outline

- Introduction and motivation
- ADC testing issues
- Multichannel digitizer in AMS 0.35 um
- **Multichannel SAR ADC in IBM 130 nm**
  - SAR architecture considerations
  - Design of 10(6)-bit SAR ADC
  - **System level blocks (PLL, SLVS, …)**
- Preliminary tests of prototypes in IBM 130 nm
  - SAR ADC, PLL, SLVS
- Summary

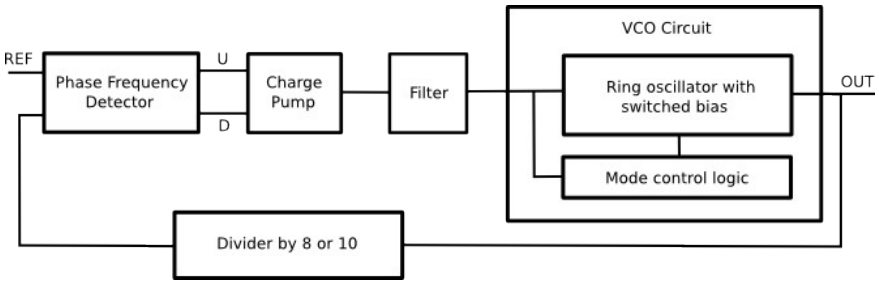
Design of PLL for data serialization
Example of 6-bit ADC

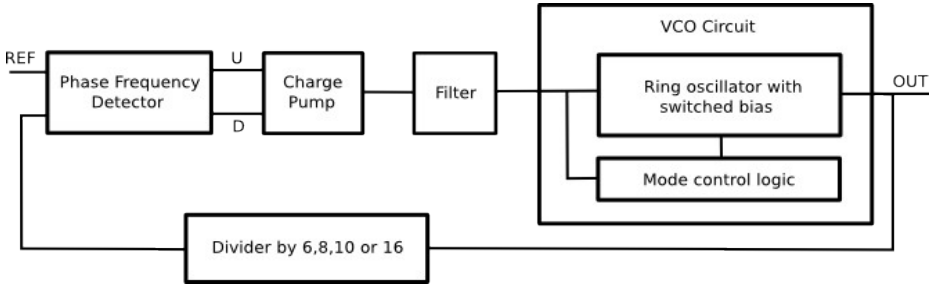


PLL needed to multiply Sample CLK frequency by 6 (in this example)

- Flexible PLL needed for our applications
  - different division factors needed for 6(10)-bit ADCs and maybe also for different numbers of ADC channels
  - scalable frequency PLL needed for scalable sampling rate ADC
- Low power consumption is default requirement

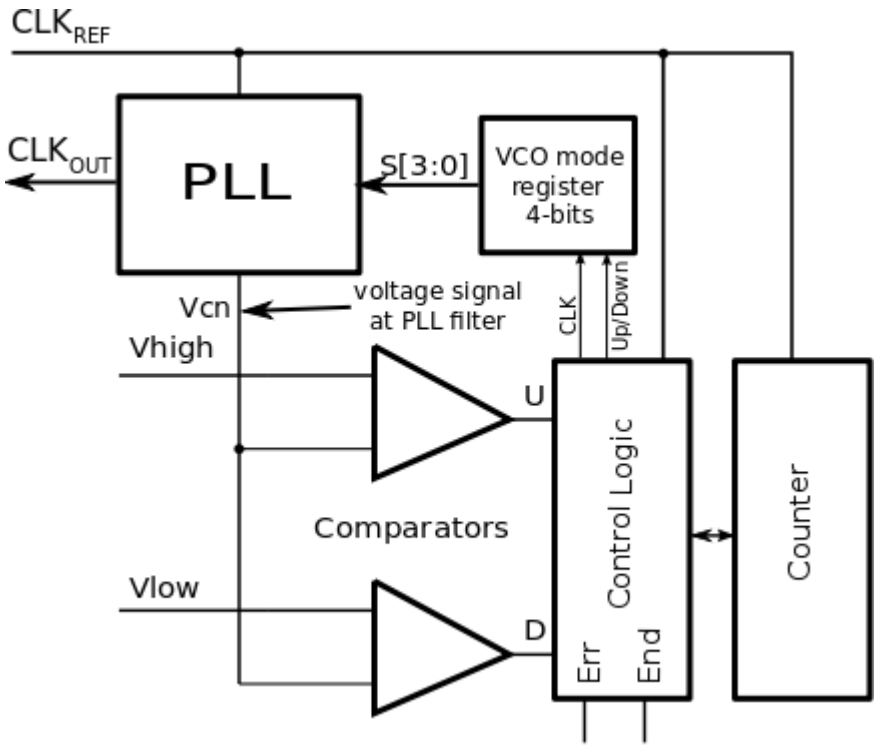
Design of PLL for data serialization





- Design specifications:
  - Architecture – type II PLL with 2nd order filter
  - Technology - IBM130 nm
  - Scalable frequency and power consumption
  - Automatically switched VCO range (narrow ranges for small jitter)
  - Configurable division factors
  - Very low power consumption

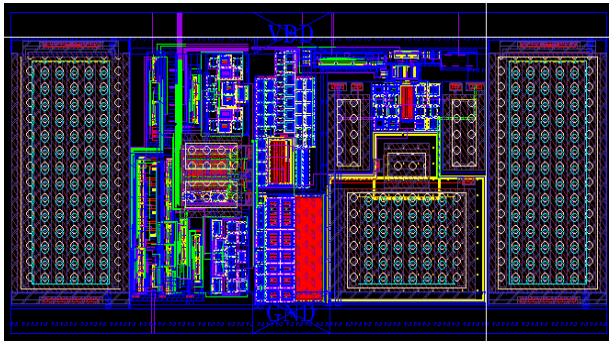
PLL - principle of automatic VCO mode change



- Comparators check whether a voltage signal at the PLL filter (Vcn) is grater than Vhigh or lower than Vlow.
  - If Vcn > Vhigh (VCO too slow) for certain period (measured by counter) control logic switches the mode register to faster mode (up).
  - If Vcn < Vlow (VCO too fast) VCO mode register is switched to slower mode (down).
  - When Vcn voltage stays between Vhigh and Vlow the mode is not changed.

PLL prototypes in IBM 130nm

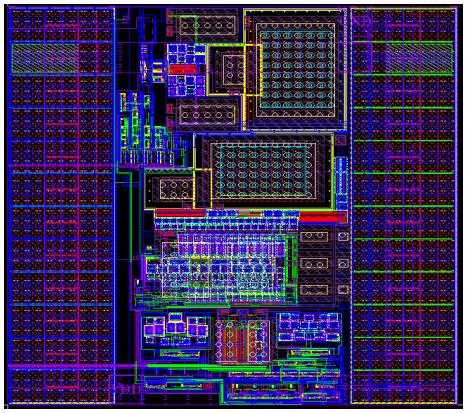
1st prototype



- Output frequency range 60 – 520MHz
- Simulated power ~0.2mW @ 500MHz
- Low area 200x160 um
- Automatically changed VCO modes
- PLL divider by 8 or 10
- Used for 10-bit ADC serialization

Fabricated in mid 2012

2nd prototype

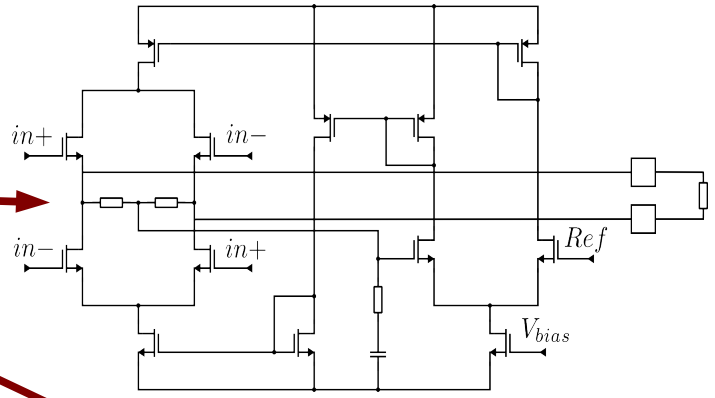


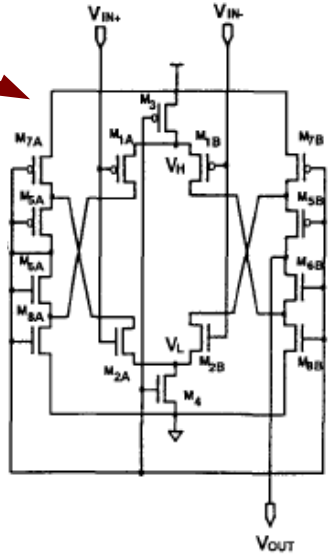
- Output frequency range 8MHz - 3GHz
- Simulated power ~1mW @ 3GHz
- Low area 300x300 um
- Automatically changed VCO modes
- PLL divider by 6, 8, 10 or 16
- Used for 6(10)-bit ADC serialization

Fabricated at the end of 2012

Design of SLVS interface

- Specifications:
  - Architecture
    - Driver – based on Boni paper
    - Receiver – based on self-biased amplifier (Bazes paper)
  - Technology – IBM 130 nm
  - Maximum frequency ~1GHz
  - Pitch matched to pads. Driver/receiver integrated with 2 pads (146um pitch)

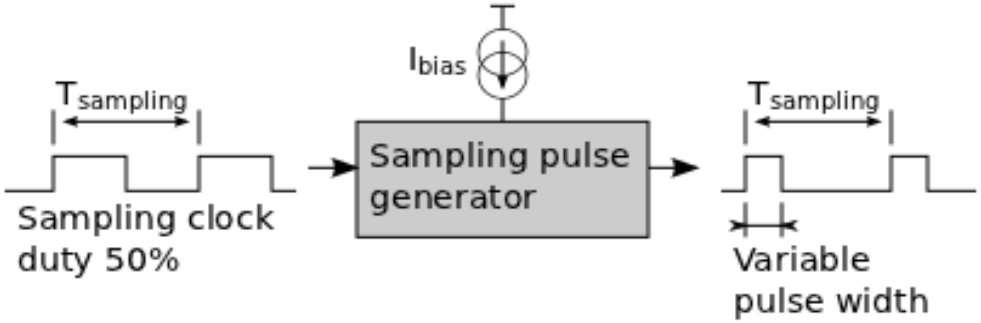


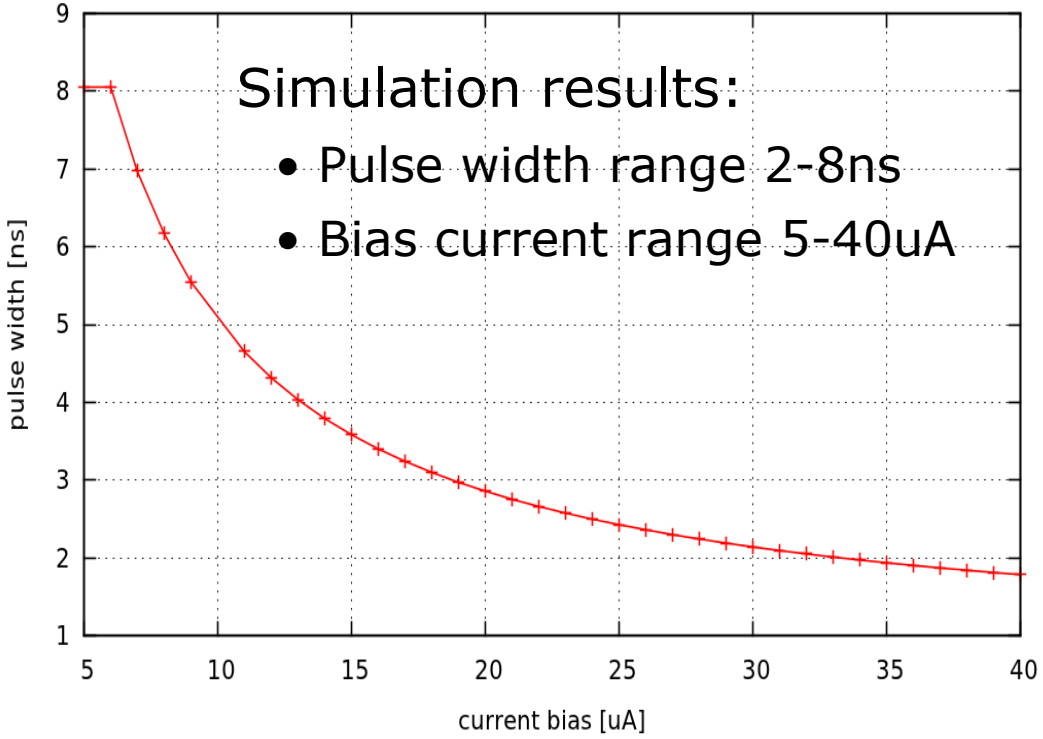


A. Boni, A. Pierazzi, D. Vecchi, LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35 µm CMOS, IEEE J. Solid-State Circuits, vol. 36, no. 4, pp. 706–711, April 2001

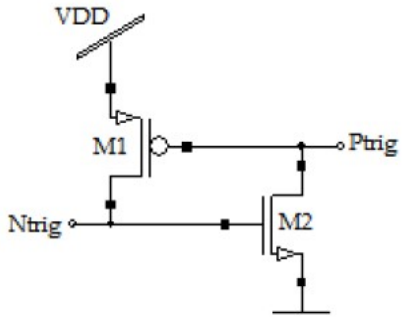
M. Bazes, Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers, IEEE J. Solid-State Circuits, vol. 26, no. 2, pp. 165–168, February 1991.

Design of sampling pulse generator



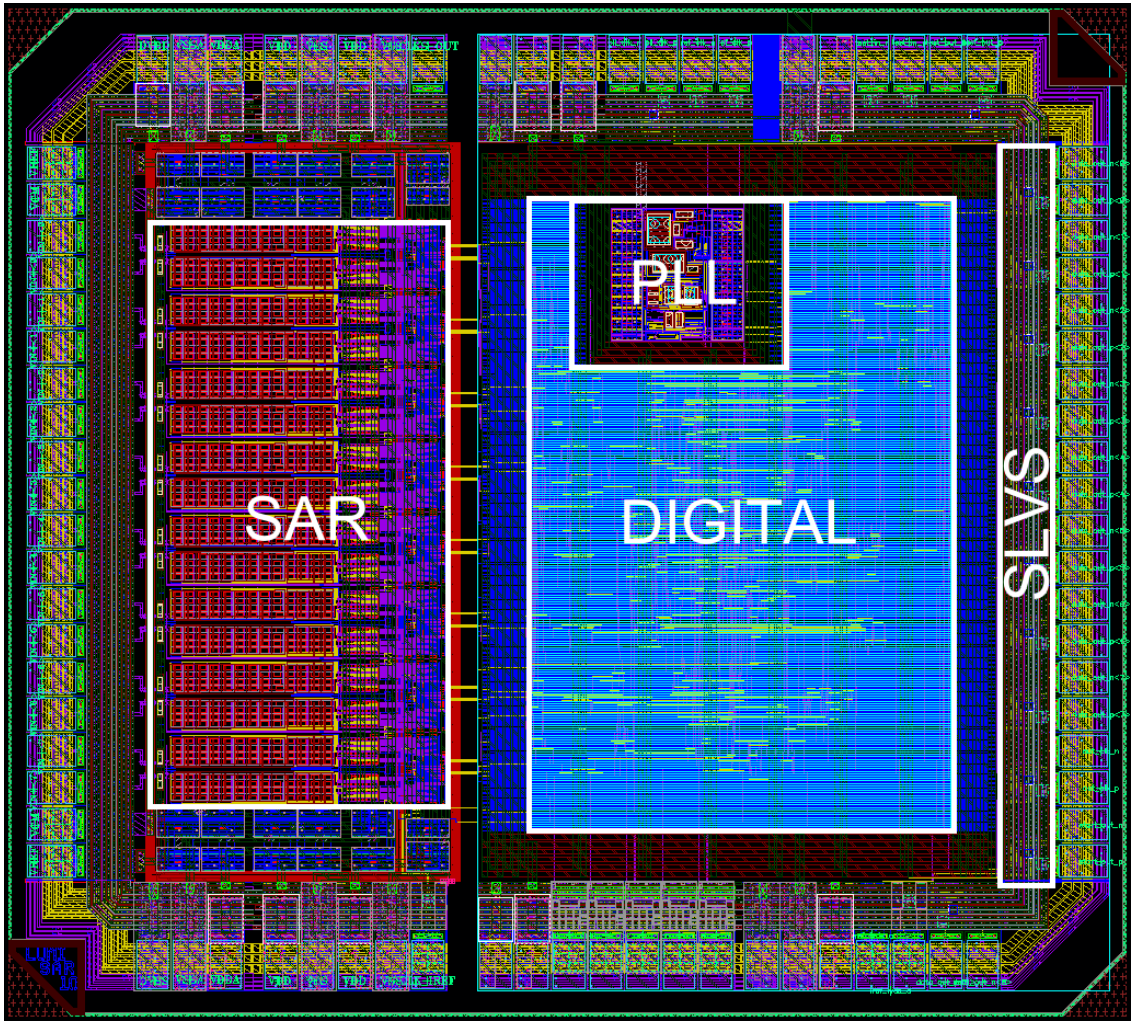


Generator of sampling pulse converts 50% duty external sampling clock into internal variable width pulse (controlled by Ibias)



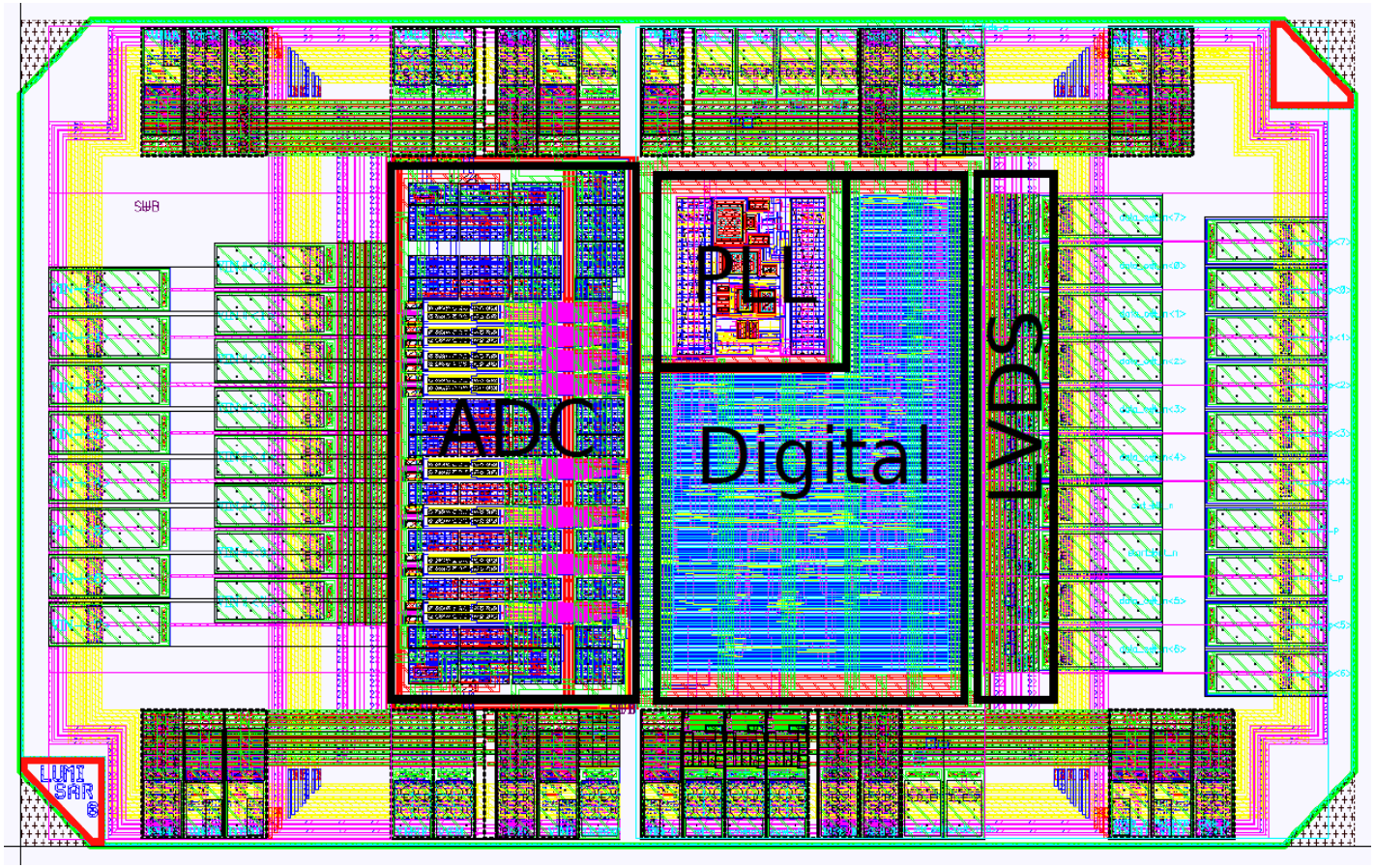
Pulse generator design is based on MOS thyristor delay circuit.

Layout of 8 channel 10-bit SAR ADC in IBM 130 nm



2200um x 2000um

Layout of 8 channel prototype of 6-bit SAR ADC in IBM 130 nm



2340um x 1380um

Outline

- Introduction and motivation
- ADC testing issues
- Multichannel digitizer in AMS 0.35 um
- Multichannel SAR ADC in IBM 130 nm
  - SAR architecture considerations
  - Design of 10(6)-bit SAR ADC
  - System level blocks (PLL, SLVS, ...)
- **Preliminary tests of prototypes in IBM 130 nm**
  - **SAR ADC, PLL, SLVS**
- Summary

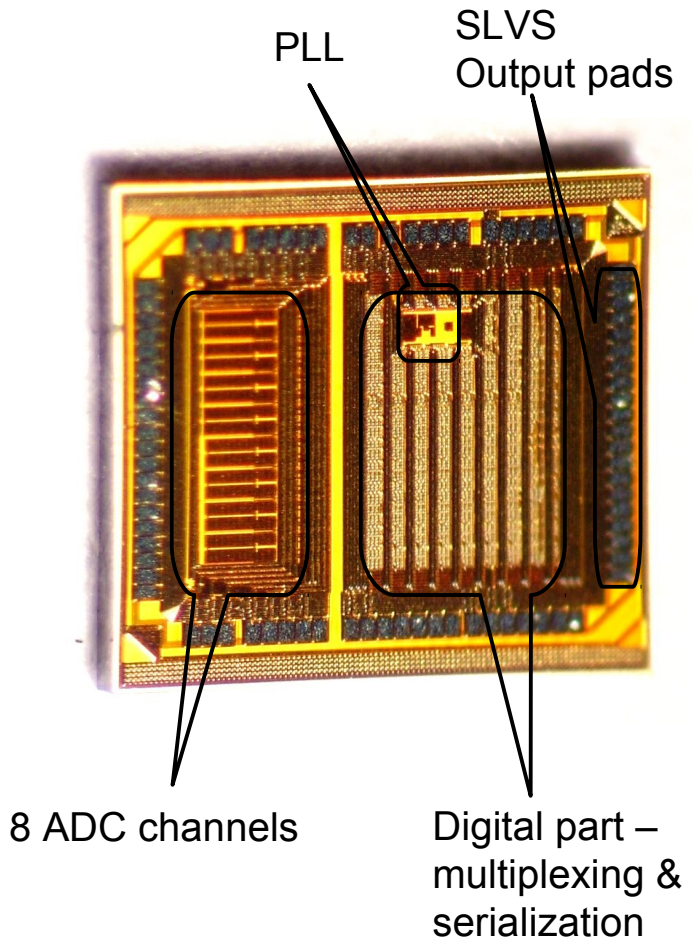
Prototypes under tests… 10-bit ADC, PLL, SLVS

Prototype of 10-bit ADC

- SAR ADC with segmented DAC
- Scalable frequency (up to ~50 MS/s) and power consumption
- Simulated power consumption 1-2mW at 40MS/s
- 146um pitch

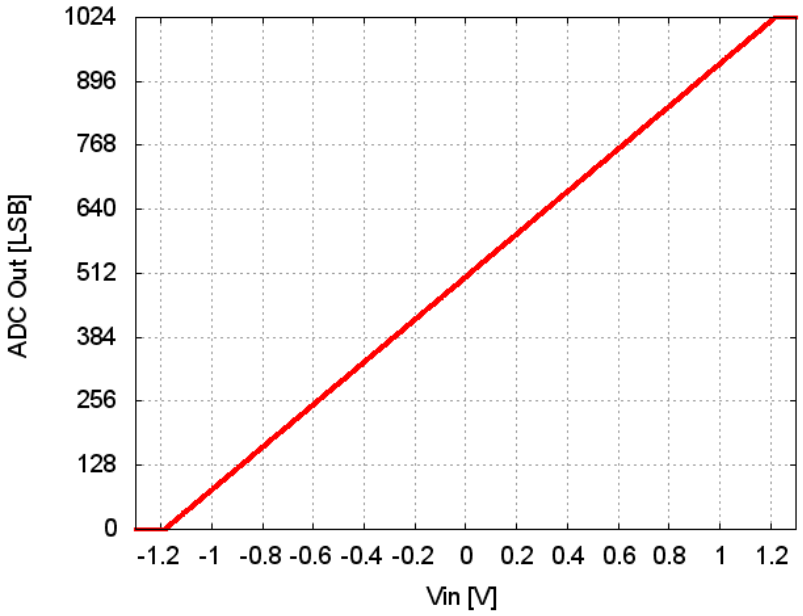
Prototype of PLL

- Type II PLL with 2nd order filter
- Scalable frequency&power
- Automatically switched VCO frequency range 8MHz – 3GHz
- VCO frequency division by 6, 8, 10 or 16
- Simulated power consumption ~1mW at 3GHz

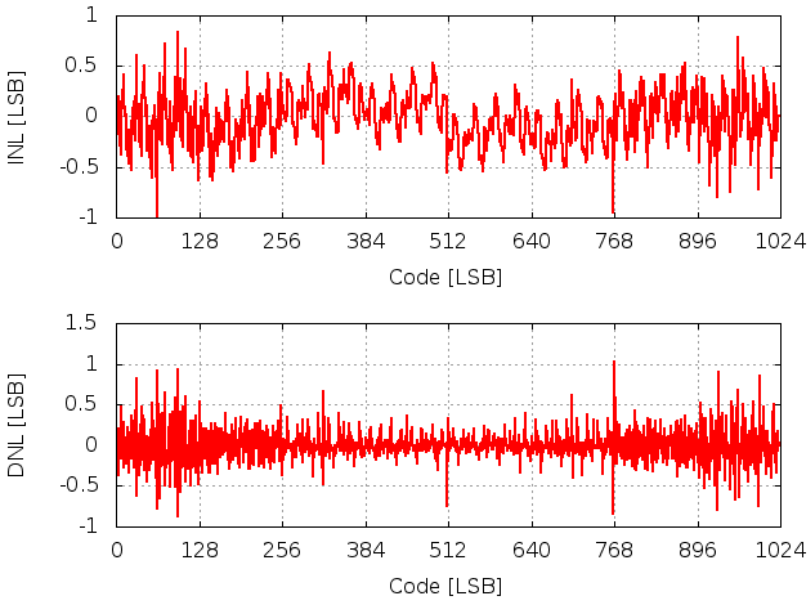


Preliminary measurements of 10-bit SAR ADC
Static measurements

Transfer function

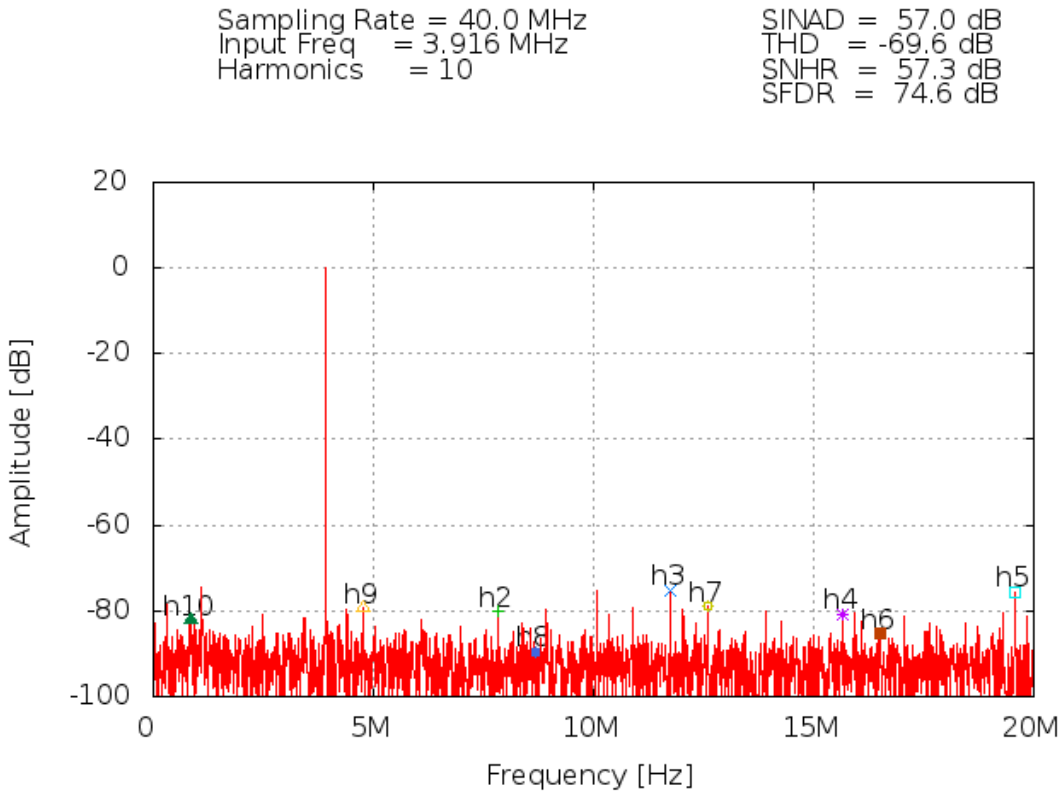


INL/DNL measurements



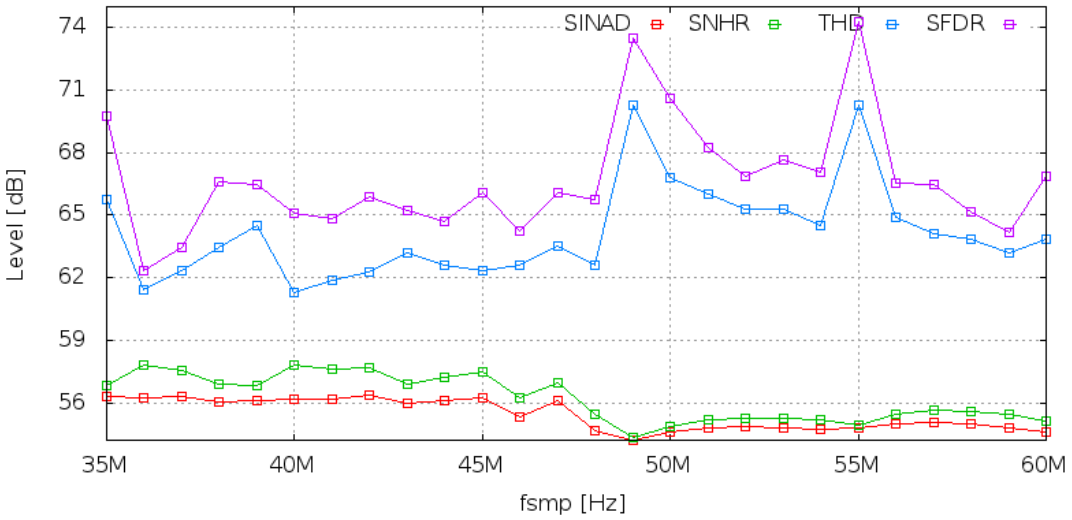
- ADC is alive and works in the whole input signal range
- There are some codes with worse linearity (to be investigated...)

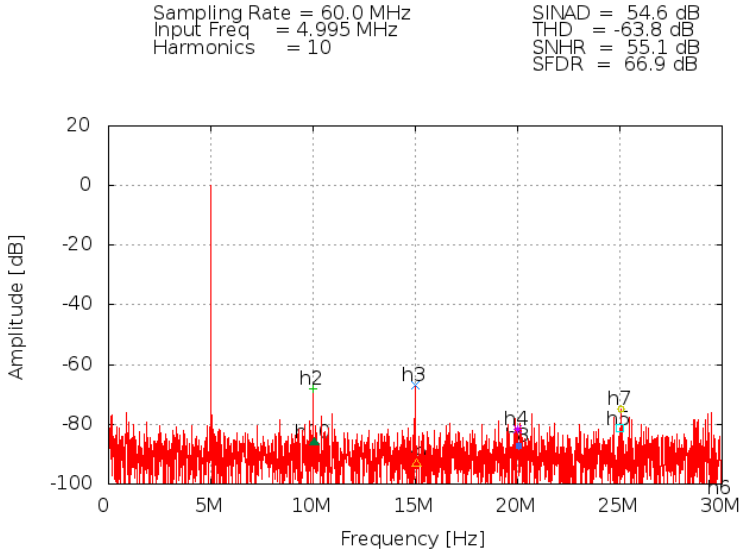
Preliminary measurements of 10-bit SAR ADC Dynamic measurement at 40Ms/S



- First dynamic measurements show that ADC is fully functional and gives reasonable resolution results
- Quantitative measurements in progress...

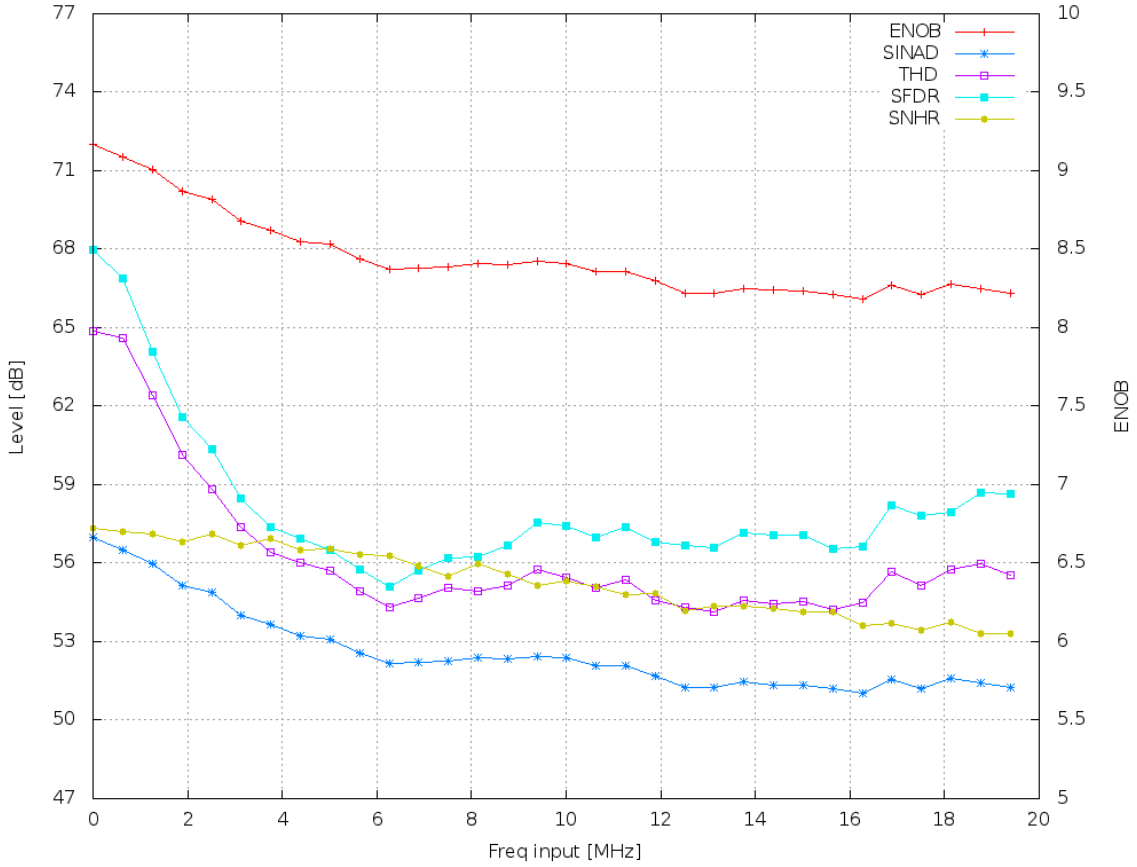
Preliminary measurements of 10-bit SAR ADC
Maximum sampling frequency

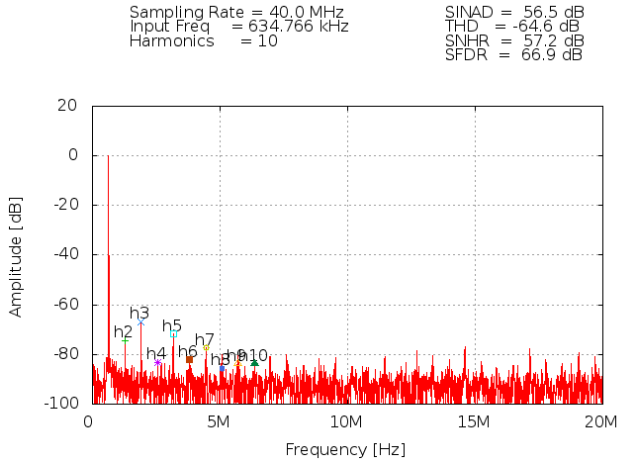


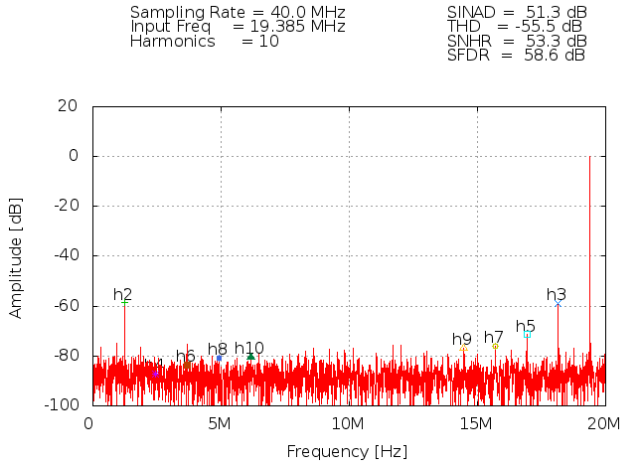


- It is suspected that measured ENOB is limited by the setup

Preliminary measurements of 10-bit SAR ADC
Dynamic measurements – f_{in} scan

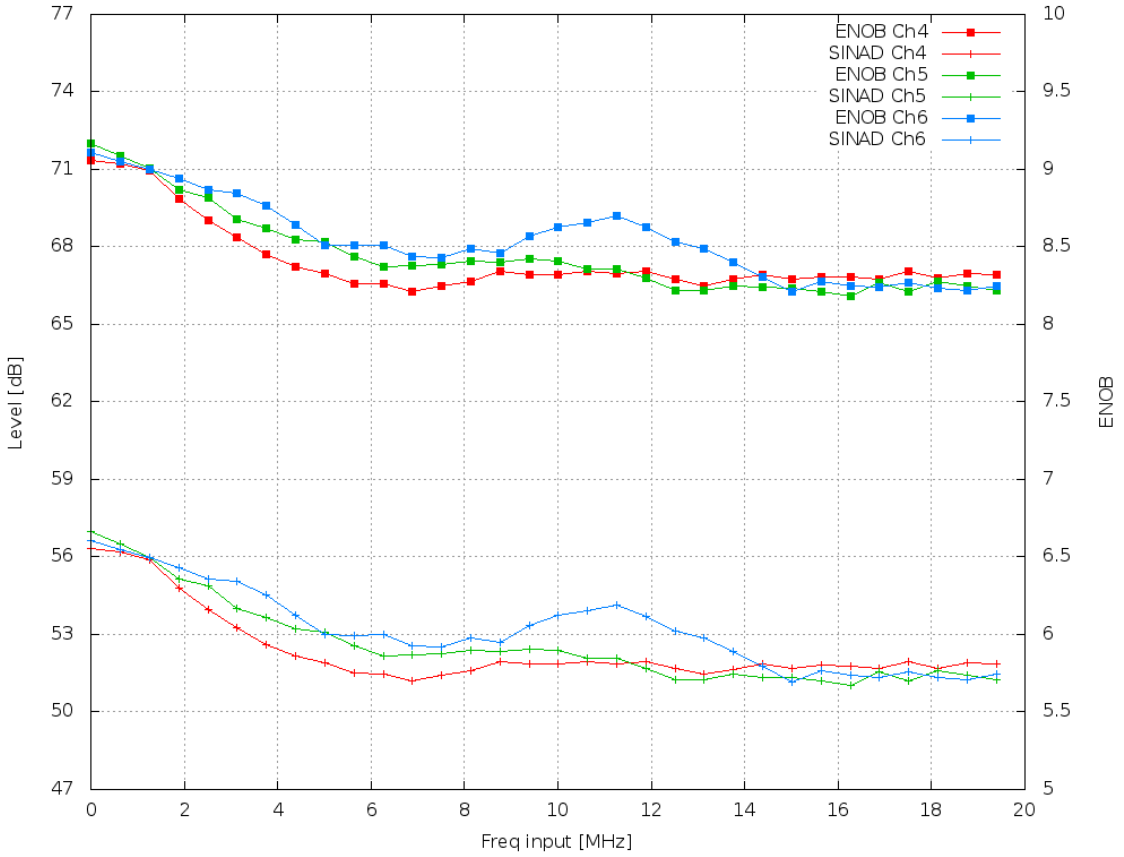






- For low f_{in} ENOB of >= 9.2 was measured
- It is suspected that ENOB decrease with f_{in} is partially/mainly due to setup

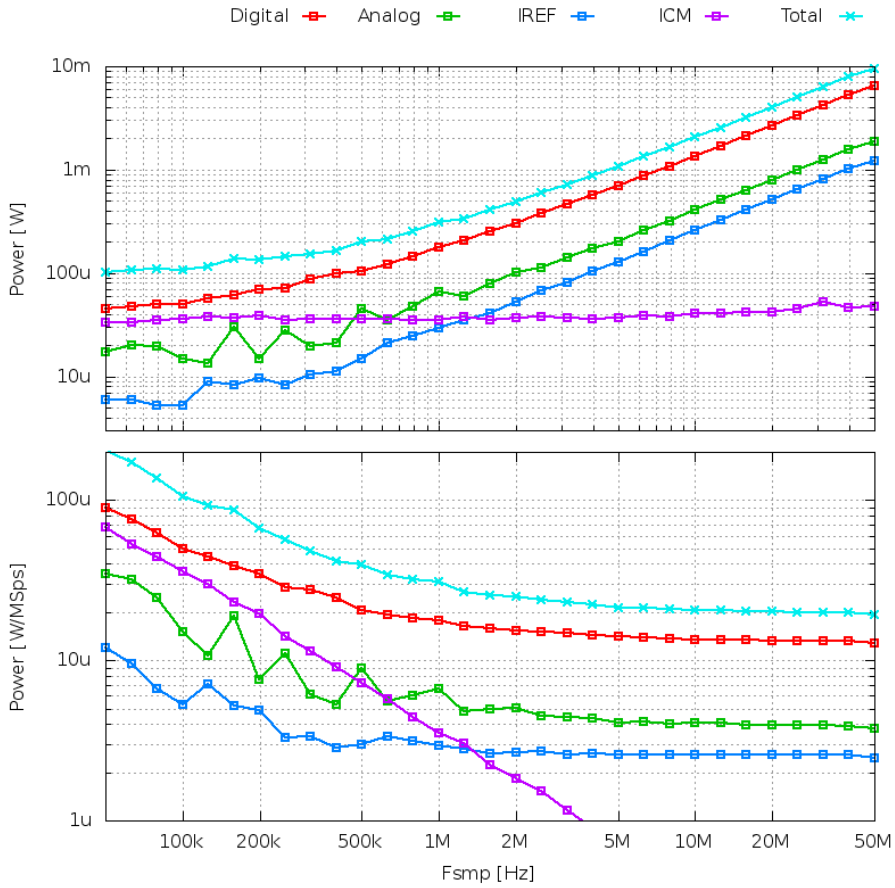
Preliminary measurements of 10-bit SAR ADC
Dynamic measurements – different channels



Results for different channels (only one channel ON during measurements) are similar

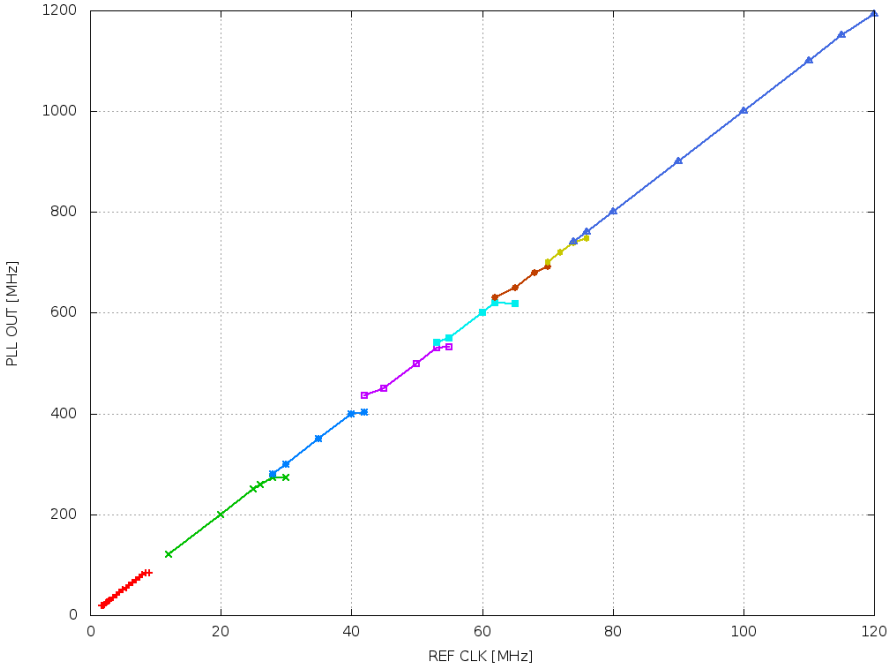
Preliminary measurements of 10-bit SAR ADC Power consumption vs sampling frequency

- Power measured for 8 ADC channels
- At 40MS/s power consumption is about 1 mW per channel – in agreement with simulations

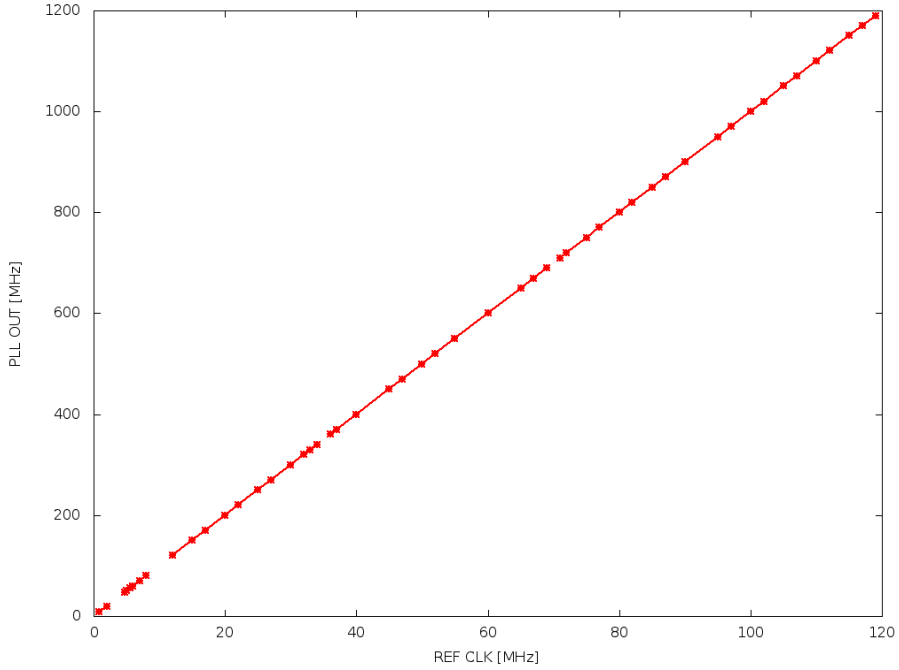


Preliminary measurements of PLL CLK out vs CLK ref

Manual mode setting

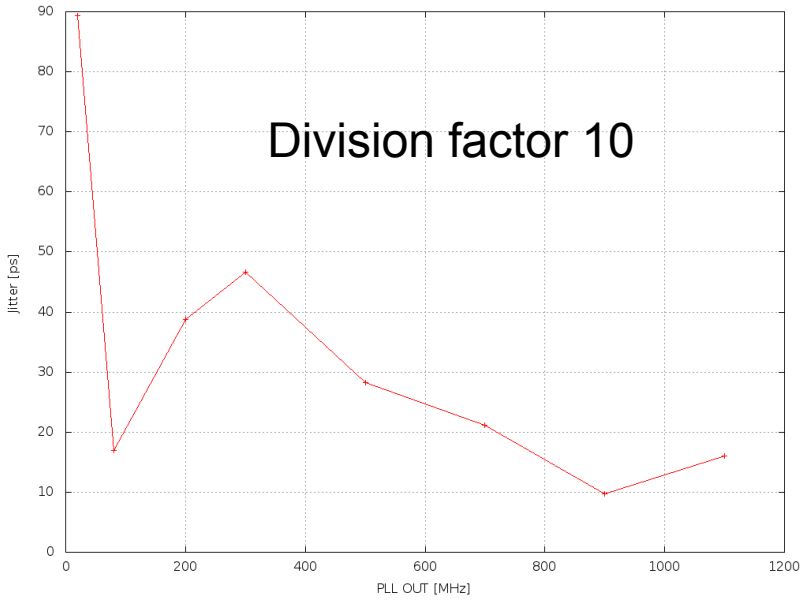


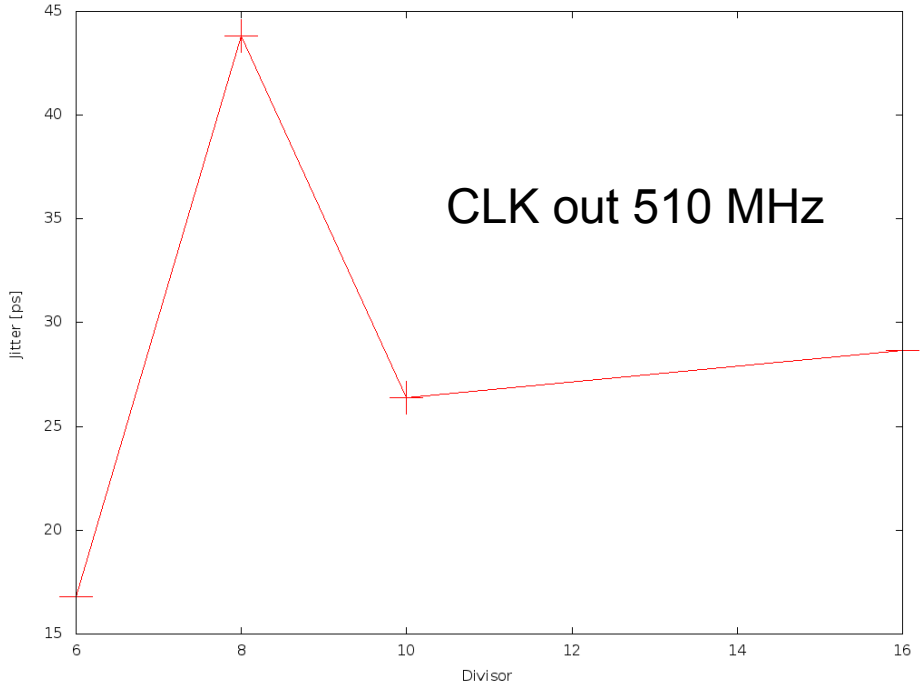
Automatic mode setting



- PLL measurements have just started (~ 2 days) and are in progress...
- PLL output CLK in frequency range 15MHz-1.2GHz already observed
- There are some gaps between frequency ranges...
- Automatic mode detection looks promising
- SLVS driver works at least up to 1.2 GHz (used for PLL output)

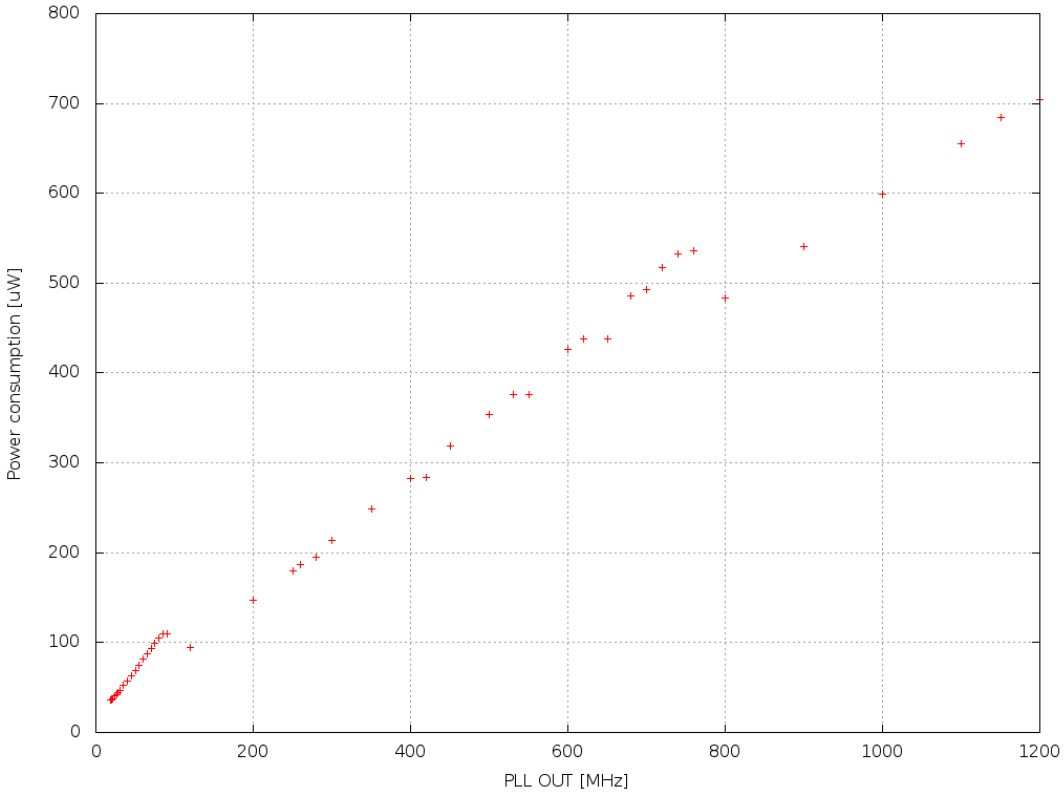
Preliminary measurements of PLL Jitter





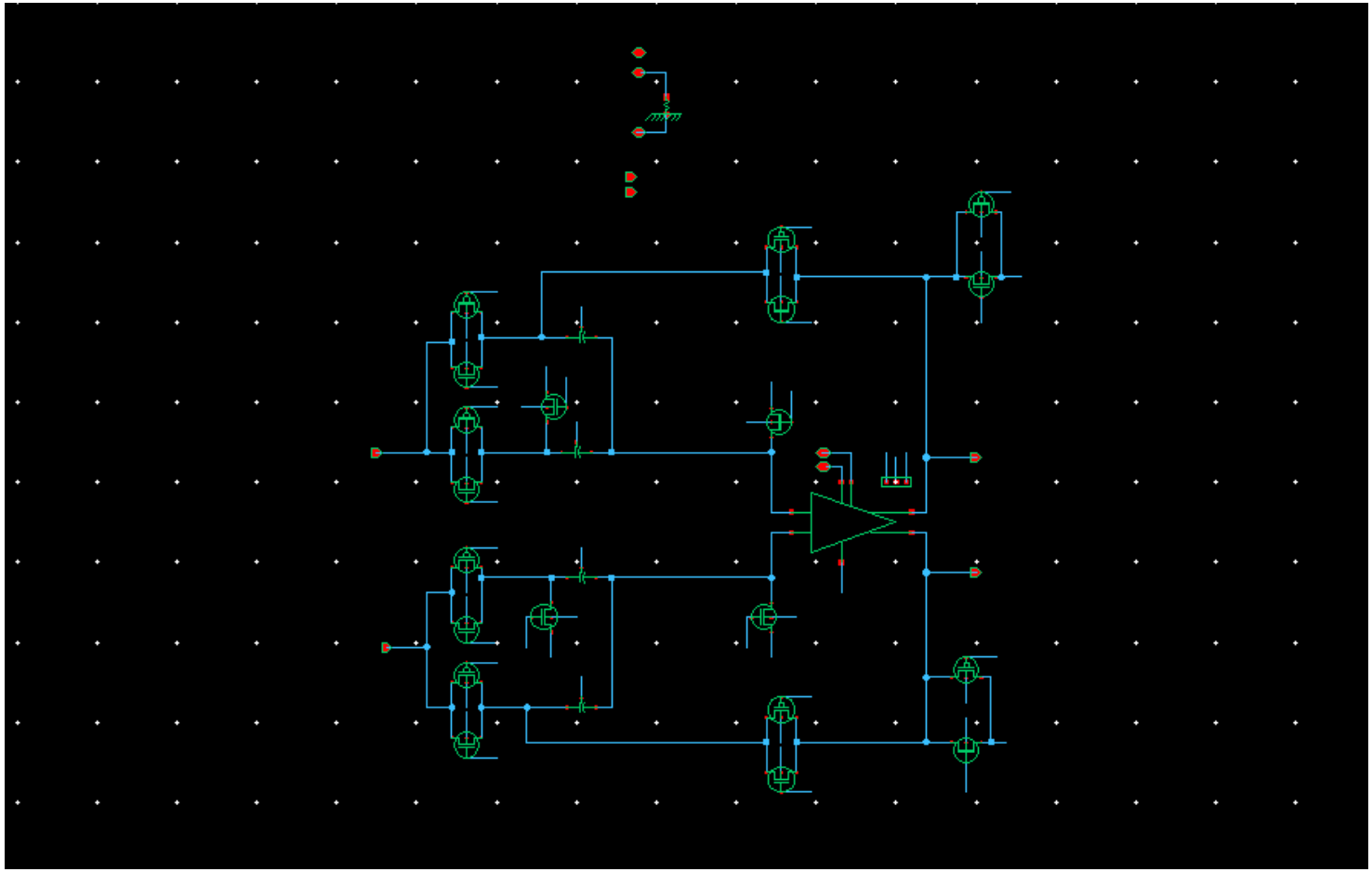
- Measured jitter at least few times higher than simulated (to be verified...)

Preliminary measurements of PLL Power consumption



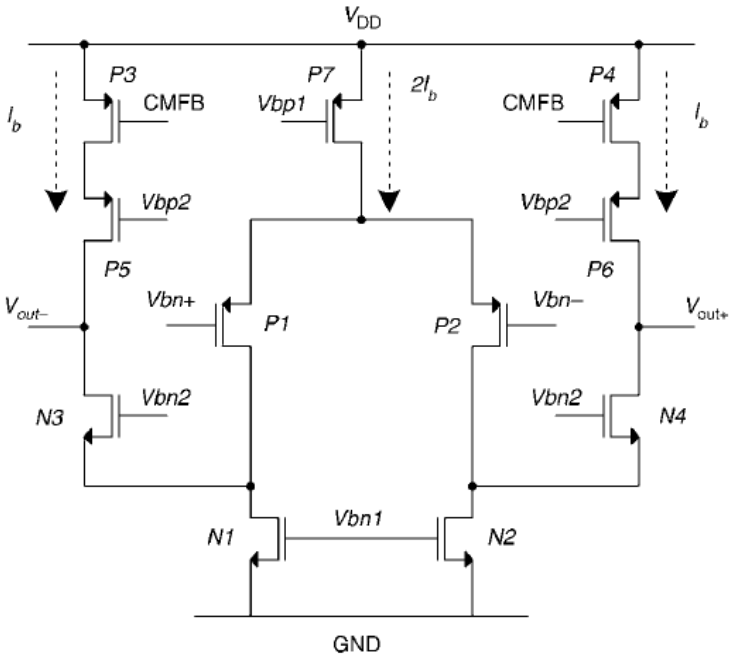
• Power consumption seems to be higher than simulated (to be verified...) but anyway very low

Front-end architecture
Single-to-Differential converter



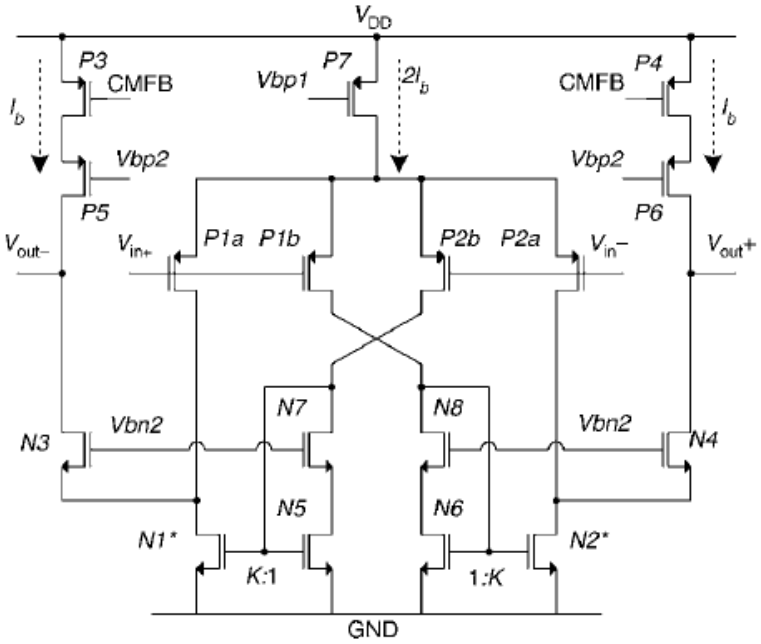
Converter has gain of 2, 100-250 uA for 6-bit

Sampling amplifier issues



Conventional folded cascode (FC)

$Gm_{FC}=gm_{P1}$, $SR_{FC}=2I_b/C_L$



Recycling folded cascode (RFC)

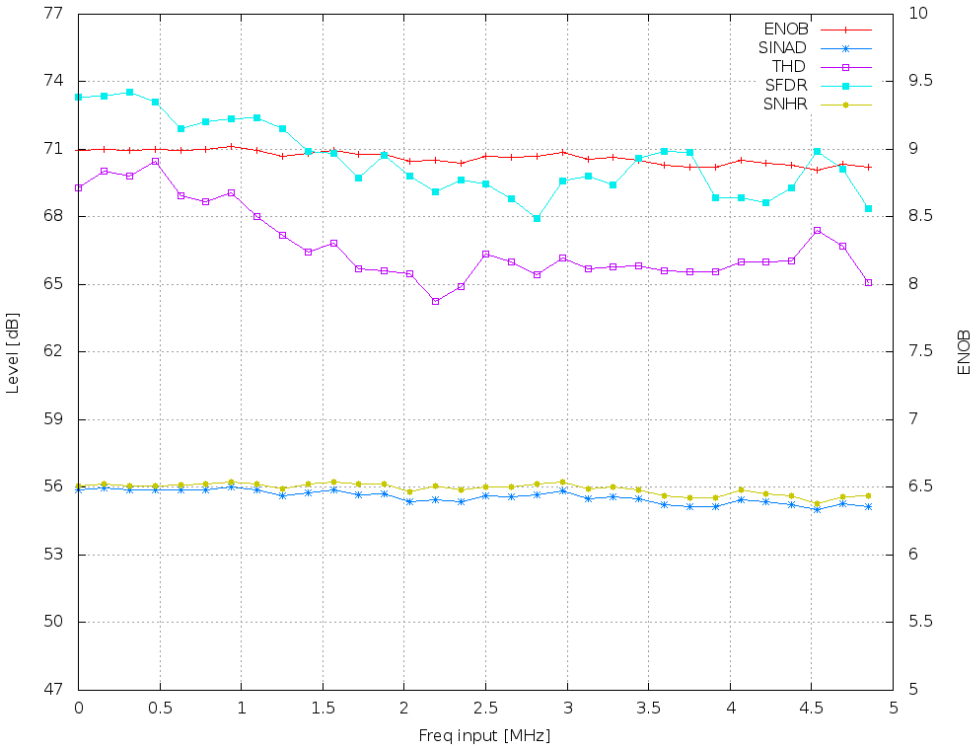
$Gm_{RFC}=gm_{P1}$ (1+K), $SR_{RFC}=2KI_b/C_L$

In 130nm a gain of few hundred may be achieved. For 10-bit accuracy a second stage or a gain boosting is needed

Summary

- Multichannel ADC in AMS 0.35um developed and working well in LumiCal detector module in test beams
- Two very low power multichannel SAR ADCs (10-bit, 6-bit) developed and fabricated in IBM 130 nm
- PLLs, SLVS, etc... developed as well
- First measurements of 10-bit SAR ADC showed that the blocks (ADC in particular) are functional
  - ENOB ~9 bits (preliminary and to be verified...)
  - Power consumption ~1mW@40MHz in agreement with simulations
- Tests of 6-bit ADC should start in May...
- PLL works and looks promising
- SLVS works well up to above 1GHz
- Quantitative tests in progress...

Preliminary measurements of 10-bit ADC
Dynamic measurements – fin scan



- ENOB ~ 9.2 was measured

Sampling pulse width