AGH University of Science and Technology

LumiCal readout
Future plans and developments

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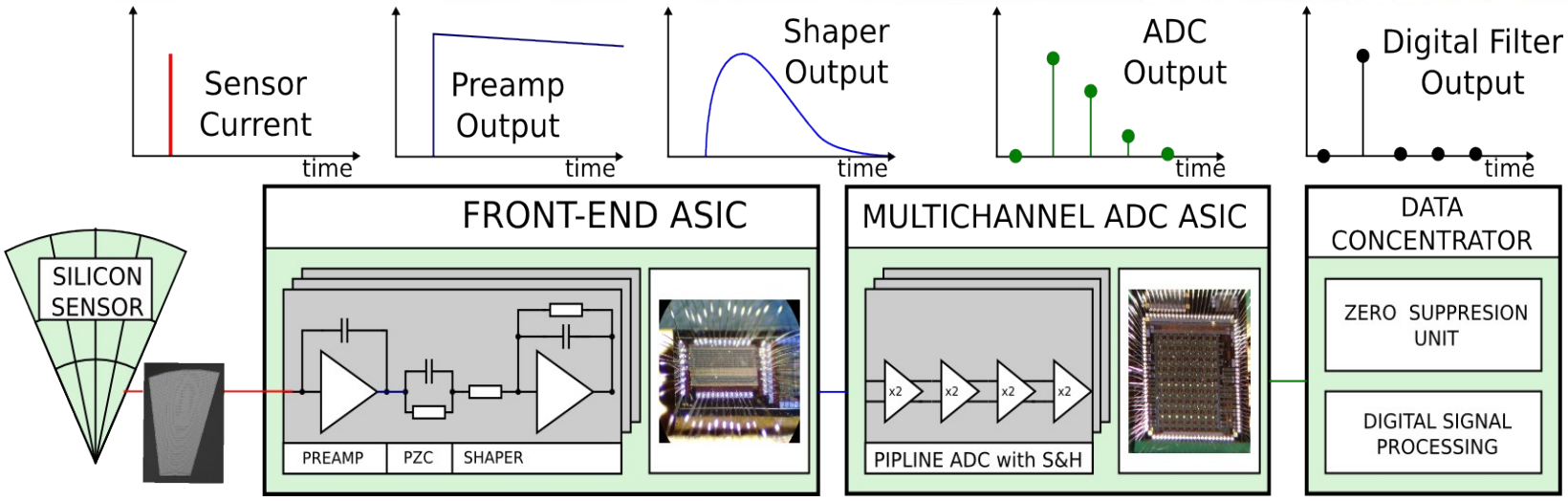
FCAL group at AGH-UST
people, infrastructure and activities

- People
  - staff: M. Idzik, K. Świentek,T. Fiutowski, Sz. Kulis will give only occasional contribution in next 2 years, phd students: J. Moroń, master students: ~1
- Dedicated labs for microelectronics and detectors:
  - Clean-room class ISO6
  - Equipment: probe-stations (e.g.semi-automatic Cascade), bonder (F&K Delvotec 5330), semiconductor parameter analyzers (Agilent B1500A x 2, HP4145A), spectrum/signal anylezers (Agilent 4395A, N9030A), scopes up to 40GS/s (e.g. Agilent 90804A), generators (e.g. Agilent 81150A, 81160A), semiconductor lasers (Picoquant PDL 800-D 660nm, 1060nm), radioactive sources, precise XYZ stages, High Voltage SMU (Keithley SMU237), RLC meters (e.g. Agilent E4980A)
  - Computer power and software for ASIC&FPGA design: 2 servers DELL MD710HD (24 cores)+disc array MD3200i, 5 x very fast PCs for fast complex analyses, personal workstations, ASIC design software (Cadence, Synopsis, Mentor Graphics), FPGA design (Xilinx), PCB design (Altium)
- Activities
  - Hardware: LumiCal Detector (ASICs, detector modules, tungsten plates, …)
  - Testbeams: preparation, running, data analysis

LumiCal detector readout chain
Status and plans



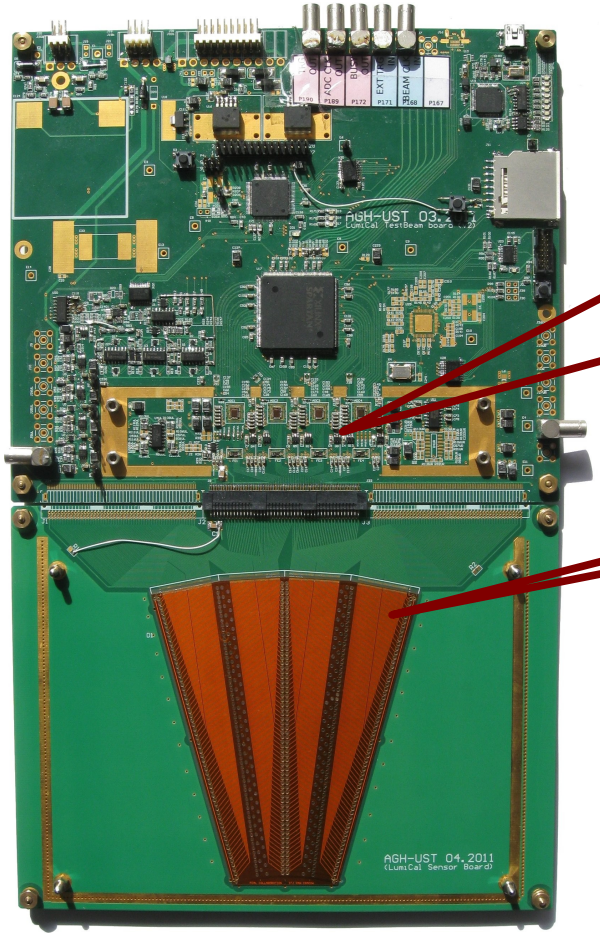
Existing LumiCal detector readout comprises:

- 8 channel front-end ASIC with preamp & CR-RC shaper Tpeak~60ns, ~9mW (**AMS 0.35um**)
- 8 channel pipeline ADC ASIC, Tsmp<=25MS/s, ~1.2mW/MHz (**AMS 0.35um**)
- FPGA based data concentrator and further readout

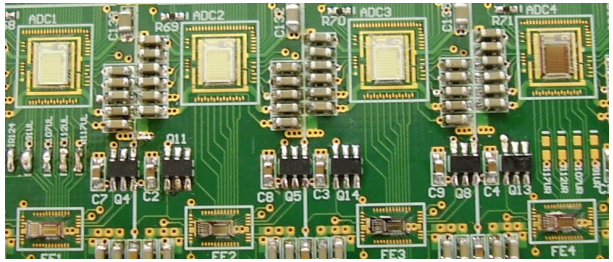
New developments for LumiCal detector readout:

- Prototype front-end ASIC **in IBM 130 nm under development…**
- Prototype SAR ADC ASIC **in IBM 130 nm under development…**

LumiCal detector – present status
Few existing detector modules



4 pairs of Front-end + ADC

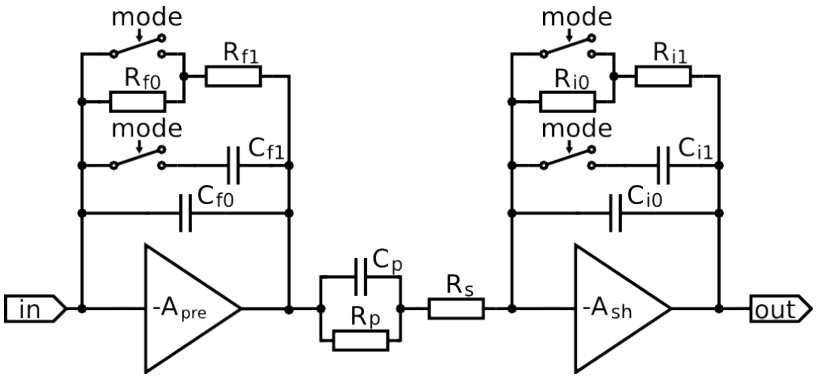


Sensor (IFJ PAN)

- LumiCal detector module with 32 fully equipped channels (Front-end +ADC ASICs) plus FPGA data concentrator is regularly used during FCAL Collaboration test-beams

Development of front-end in IBM 130nm Preamplifier & Shaper

Block diagram of existing ASIC (in AMS0.35um)

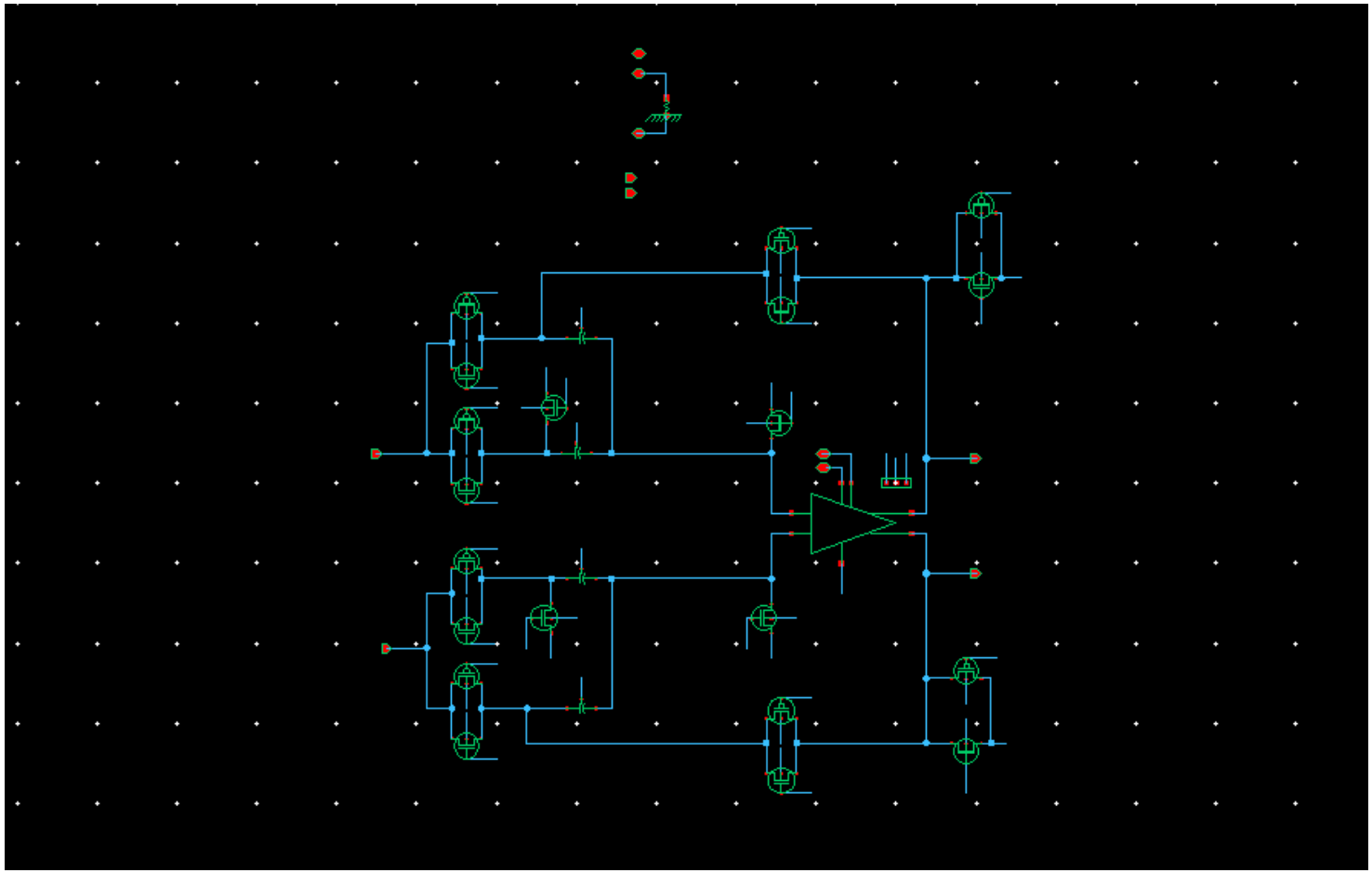


New front-end has very similar architecture ("mode" switch only in the preamplifier)

Design specs:

- 8 channels
- Cdet ≈ 5 ÷ 50pF
- 1st order shaper (Tpeak ≈ 50 ns)
- Variable gain:
  - calibration mode - MIP sensitivity
  - physics mode - input charge up to ~6 pC
- Power pulsing implemented
- Simulated power consumption ~1.5 mW/channel
- ***Design submitted in February 2013***

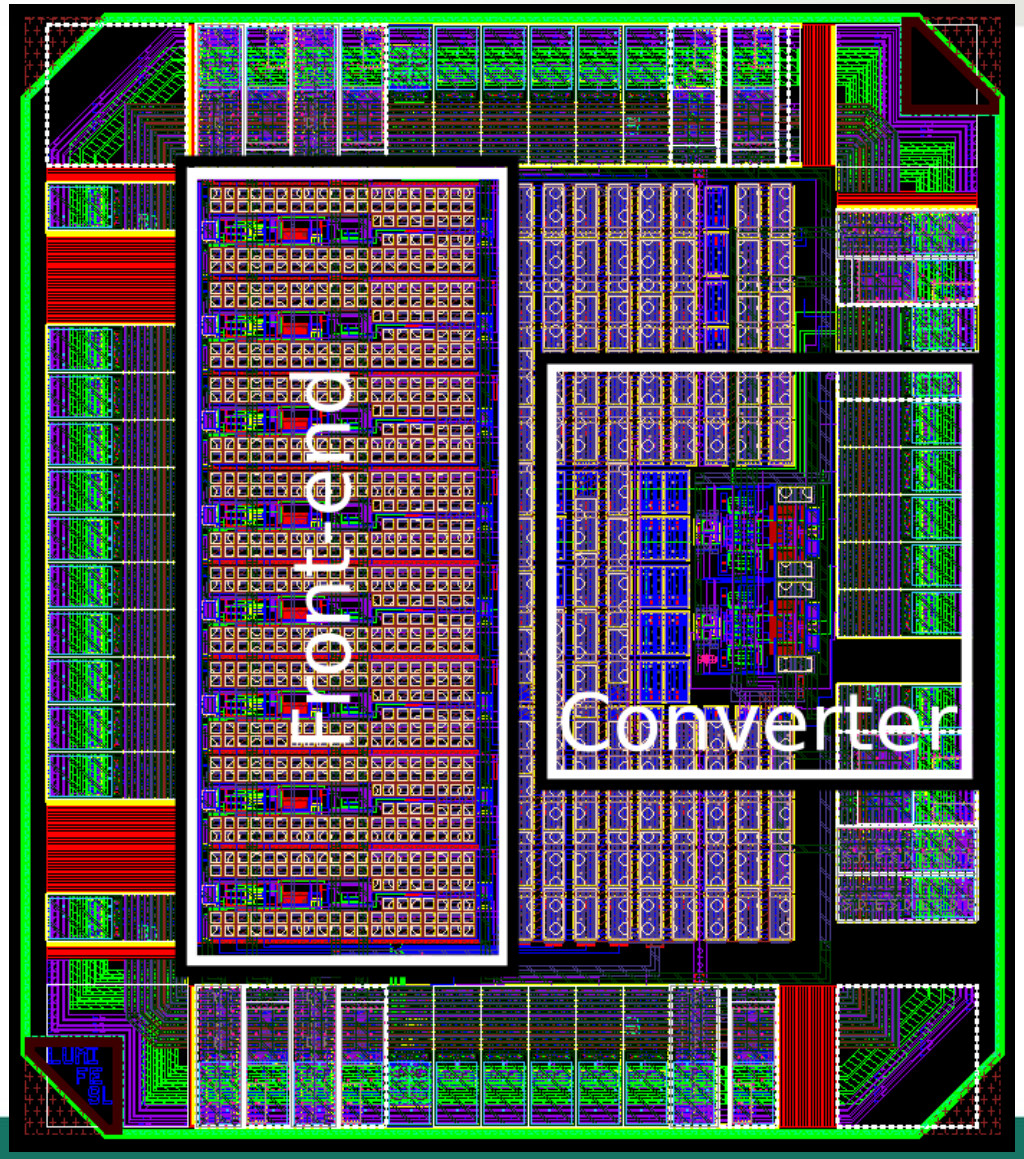
Development of front-end in IBM 130nm SingleEnded-to-Differential converter



Converter has gain of 2

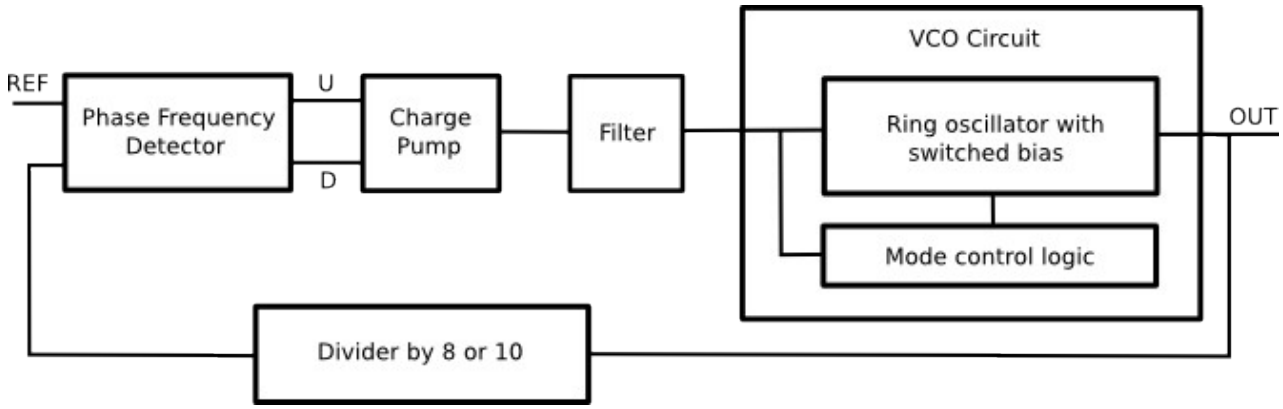
Design submitted February 2013

New front-end in IBM 130 nm



- Submitted February 2013
- 8 front-end channels
- 2 single-ended to differential converters

Design of PLL for data serialization in IBM 130nm



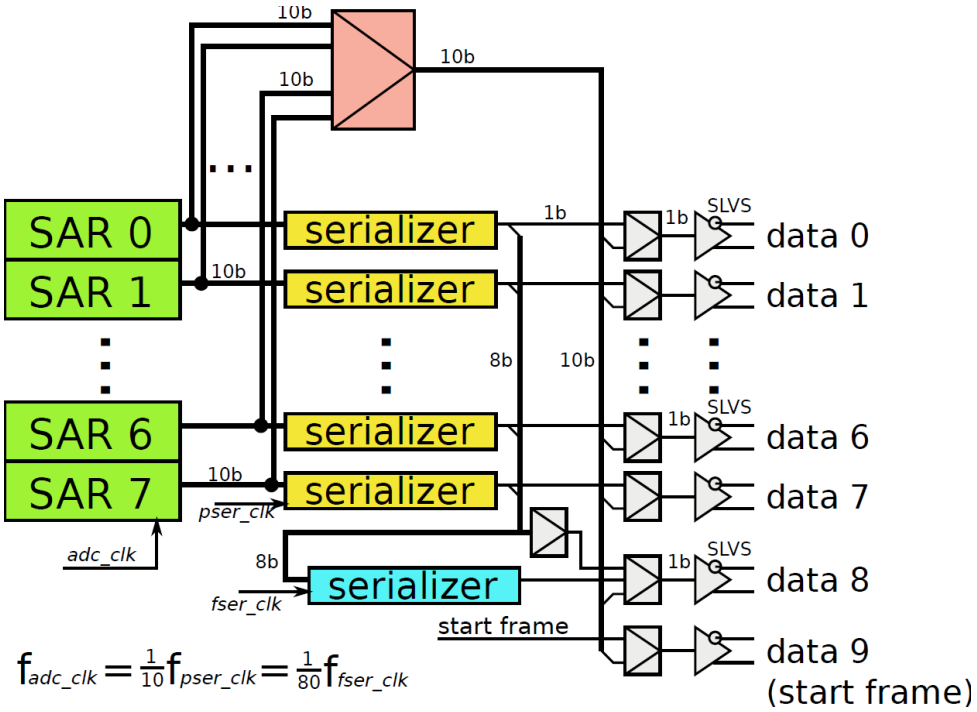
Design specs:

- Architecture: type II PLL with 2nd order filter
- Scalable frequency&power
- Automatically switched VCO freq. range
- VCO frequency range 8MHz – 3GHz,
- VCO frequency division by 6, 8, 10 or 16
- Power consumption <2mW at 3GHz
- ***Submitted and fabricated in 2012, the tests have just started…***

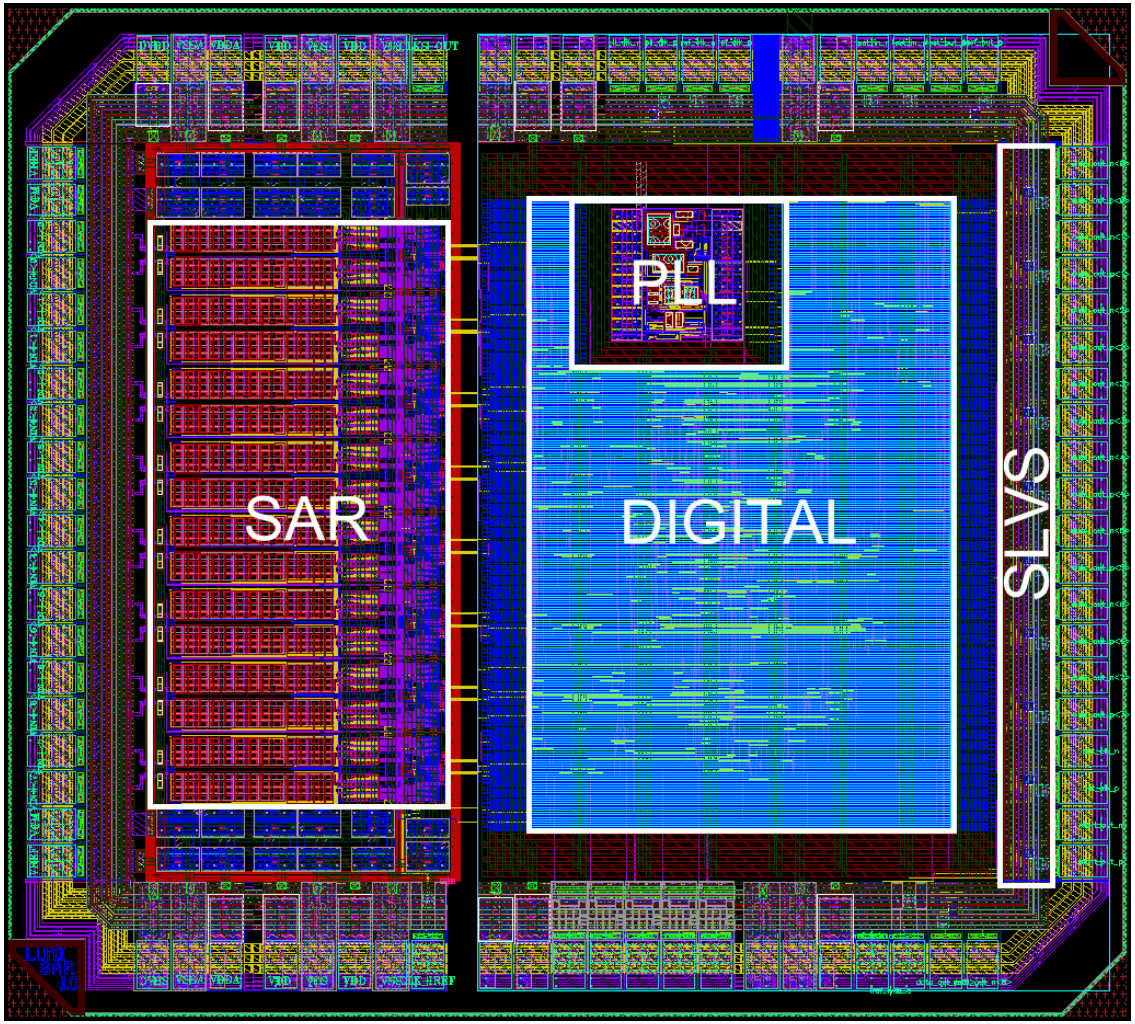
Development of multichannel SAR ADC in IBM 130 nm (K. Świentek talk)

Specifications :

- 8 channels of 10-bit (6-bit) SAR ADC
- Technology IBM 130 nm
- Layout with 146um (40um) ADC pitch
- Multimode digital multiplexer/serializer:
  - Serial mode: one data link per all channels (external clk division or PLL clk generation)
  - Parallel mode: one data link per channel (external clk division or PLL clk generation)
  - Test mode: single channnel output (max fsmp ~50 Msps)
- PLL for data serialization
- High speed SLVS interface (~1GHz)
- Power pulsing



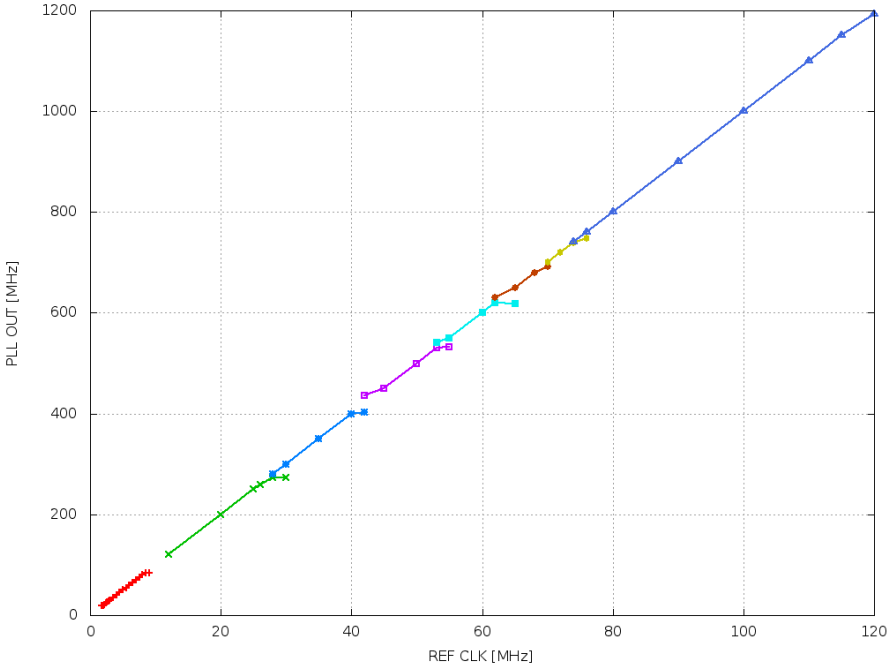
Layout of 8 channel 10-bit SAR ADC in IBM 130 nm (T. Fiutowski talk)



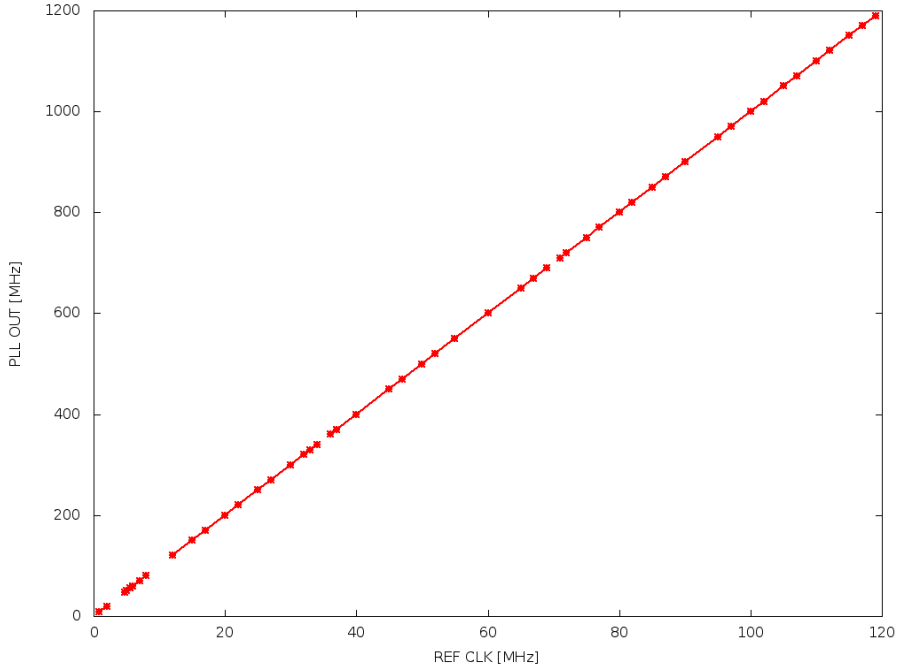
2200um x 2000um

Preliminary measurements of PLL CLK out vs CLK ref

Manual mode setting

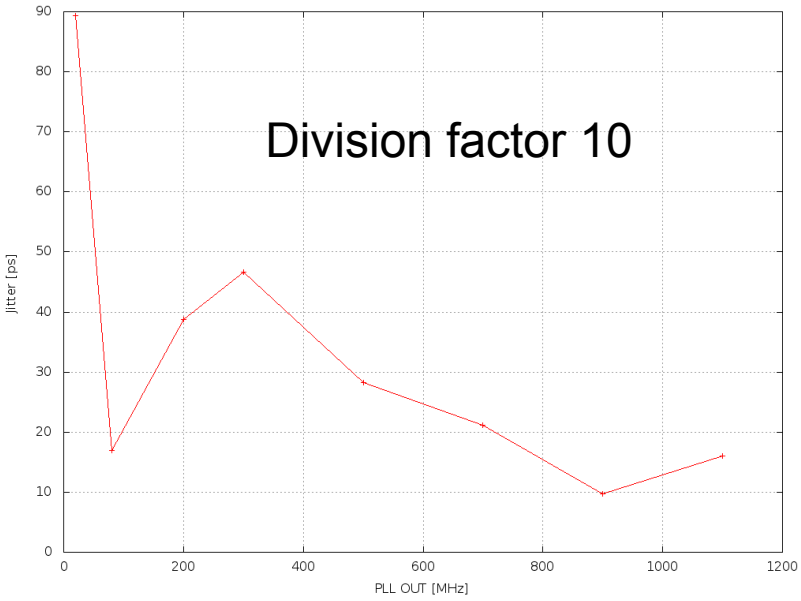


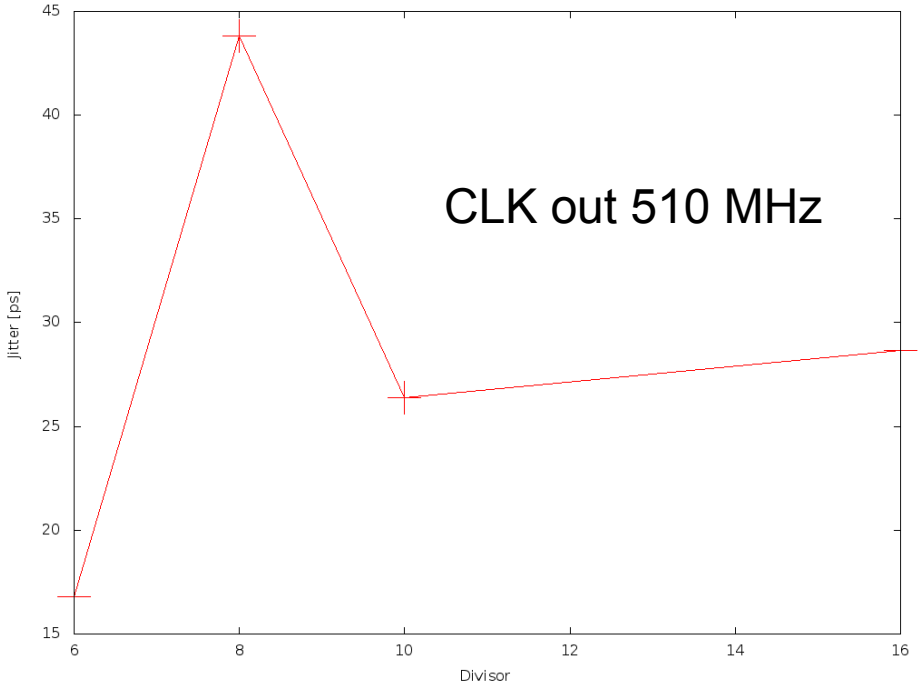
Automatic mode setting



- PLL measurements have just started (~ 2 days) and are in progress...
- PLL output CLK in frequency range 15MHz-1.2GHz already observed
- There are some gaps between frequency ranges...
- Automatic mode detection looks promising
- SLVS driver works at least up to 1.2 GHz (used for PLL output)

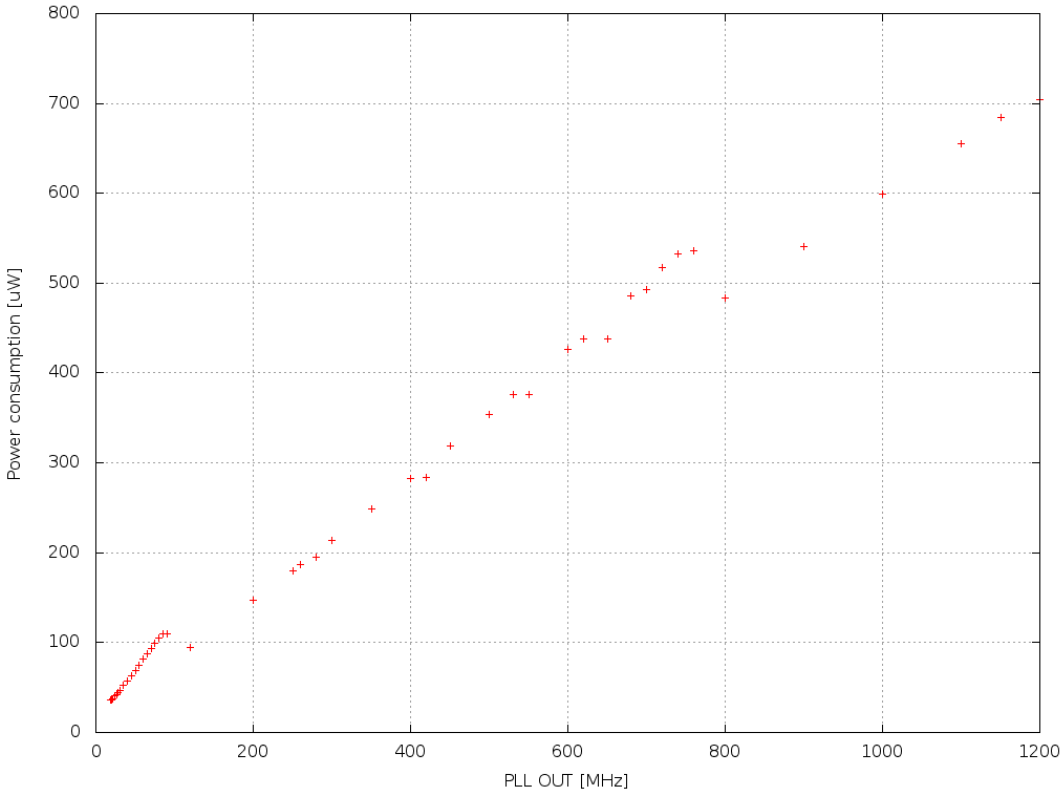
Preliminary measurements of PLL Jitter





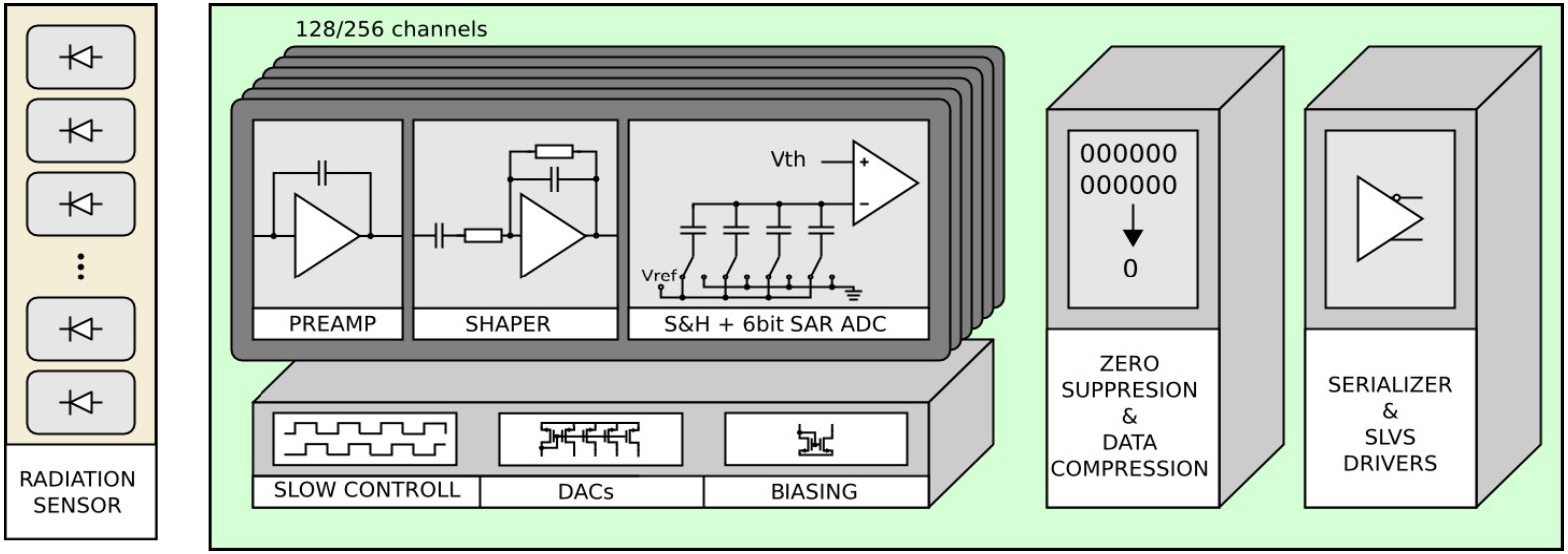
- Measured jitter at least few times higher than simulated (to be verified...)

Preliminary measurements of PLL Power consumption



- Power consumption seems to be higher than simulated (to be verified...) but anyway very low

For DSP we may gain from other project Multichannel readout ASIC for LHCb strip tracker



- Complex 128 channel ASIC
- CMOS IBM 130 nm technology
- DSP will contain:
  - Pedestal subtraction, mean common mode suppression, zero suppression

Summary and Plans

- Presently FCAL uses in test-beams the readout modules based on developed at AGH-UST front-end ASICs and FPGA base DAQ
- New ASICs of LumiCal readout in IBM 130 nm under development...
- First prototype of front-end electronics submitted and should be available in May/June 2013
- First prototypes of 10-bit SAR ADC, PLL, SLVS already produced and presently under test:
  - 10-bit SAR ADC: first results show its functionality, the effective resolution seems to be less than simulated - quantitative measurements are still progoress
  - PLL tests are just starting
  - SLVS interface works well
- Depending on test progress and results we plan next submission at the turn of 2013/2014