AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

SAR ADC Architecture and Status

Krzysztof Świentek AGH-UST
Presented works done by:
M.Firlej, T. Fiutowski, M. Idzik, Sz. Kulis, J. Moroń

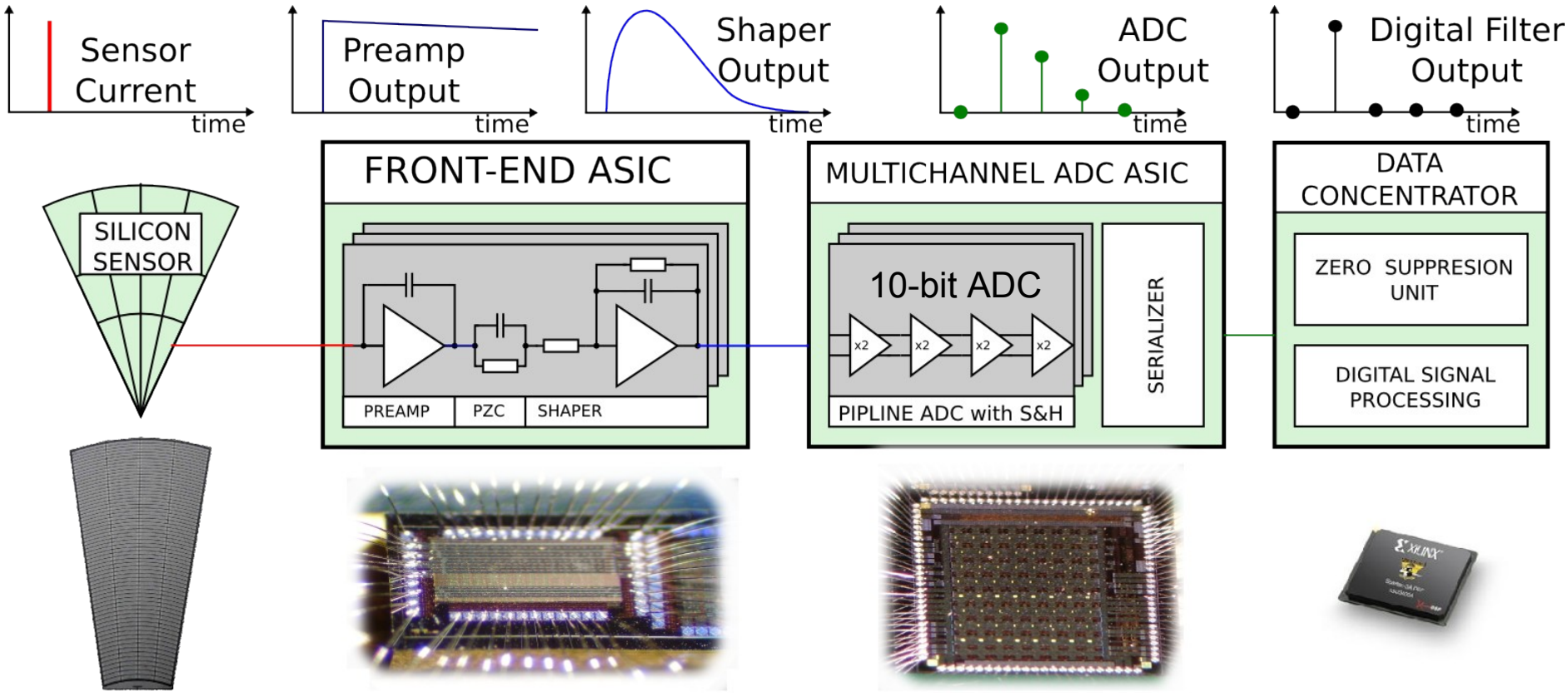
Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

26 April 2013, CERN

Outline

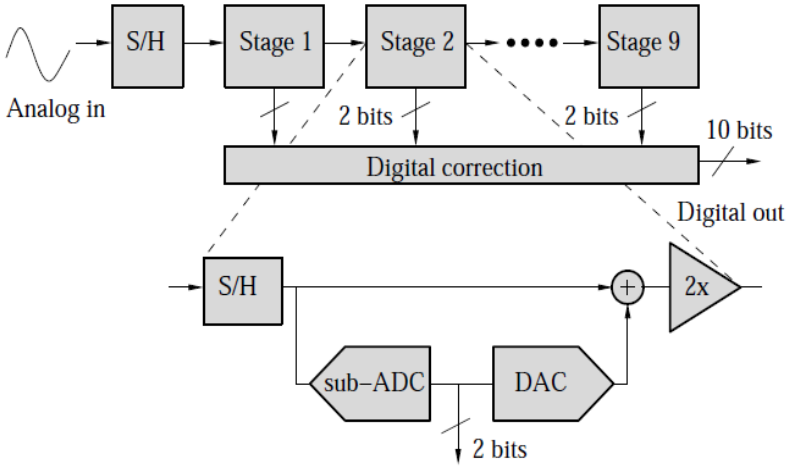
- Motivation
- Multichannel digitizer in AMS 0.35 um
- Multichannel SAR ADC in IBM 130 nm
  - SAR architecture considerations
  - Design of 10-bit SAR ADC
  - Preliminary tests
- Summary

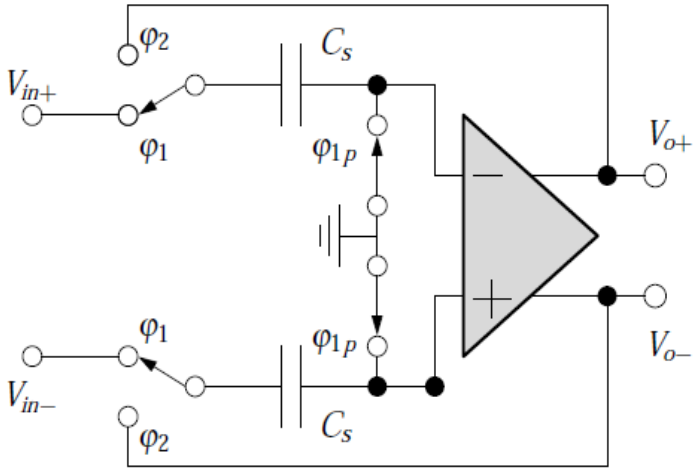
Motivation
LumiCal detector readout electronics



- Present readout ASICs developed in CMOS AMS 0.35 um
- Development of new readout in CMOS IBM 130 nm in progress...

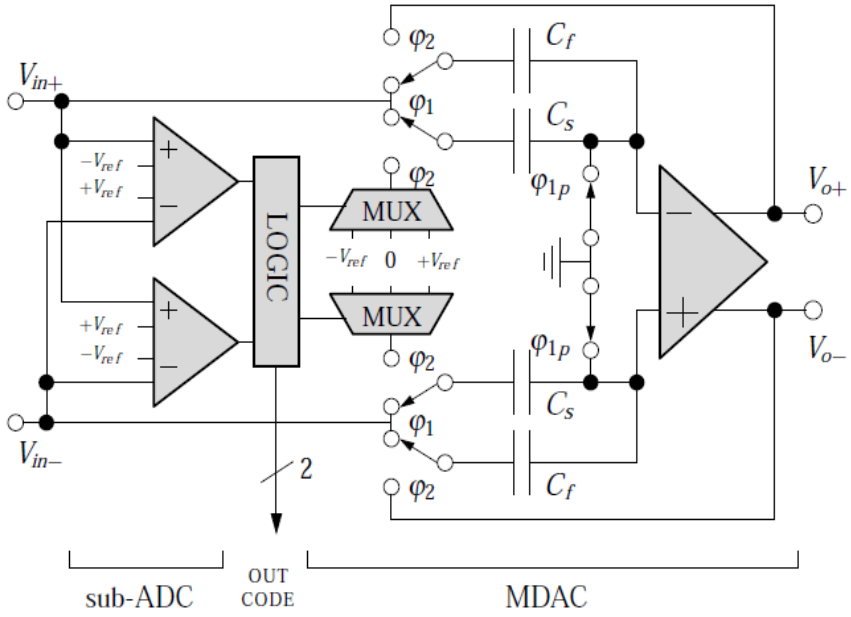
Previous work – multichannel digitizer
10-bit pipeline ADC





S/H stage

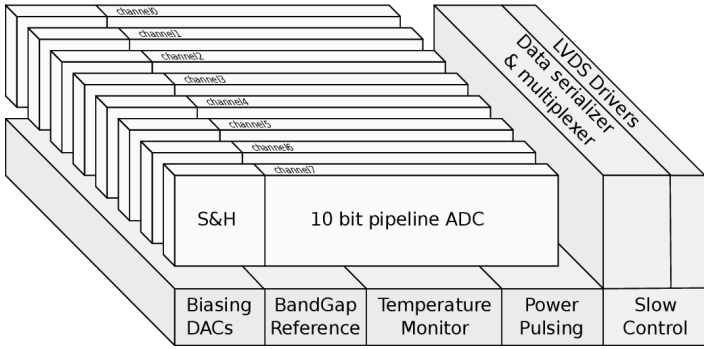
- High throughput - conversion rate = clock rate
- 1.5 bit per stage - redundancy reduces comparator requirements
- Fully differential architecture

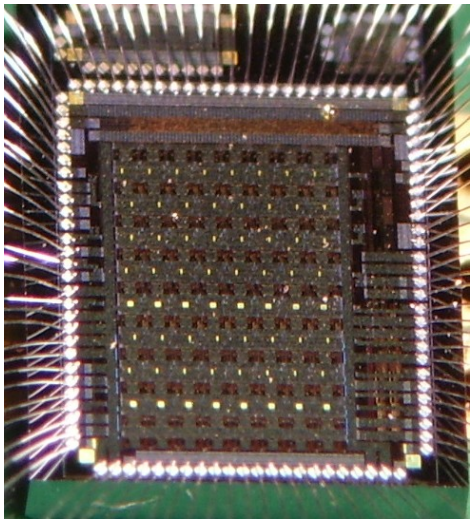


1.5 bit pipeline stage

Multichannel digitizer Architecture

- Specs & impleentation issues:
  - 8 channels of 10-bit pipeline ADC
  - Technology AMS 0.35um
  - Fully differential ADC
  - Layout with 200um ADC pitch
  - Multimode digital multiplexer/serializer:
    - Serial mode (~250MHz): one data link per all channels (max fsmp ~ 3 MSps)
    - Parallel mode (~250MHz): one data link per channel (max fsmp ~ 25 MSps)
    - Test mode: single channnel output (max fsmp ~50 MSps)
  - High speed LVDS interface (~1GHz)
  - Bootstrapped S/H switches
  - Power pulsing
  - Low power DACs for internal settings
  - BandGap reference source
  - Temperature sensor

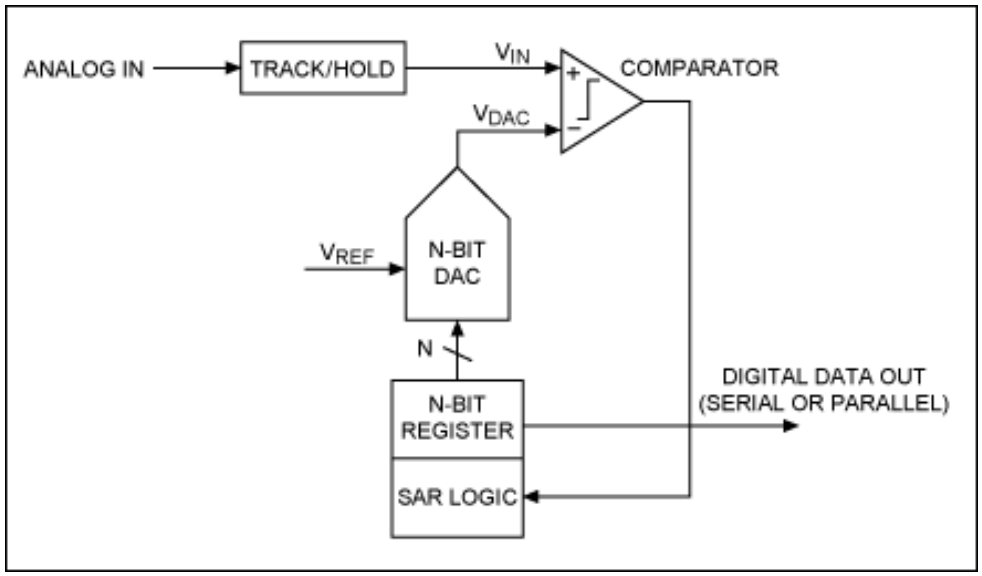


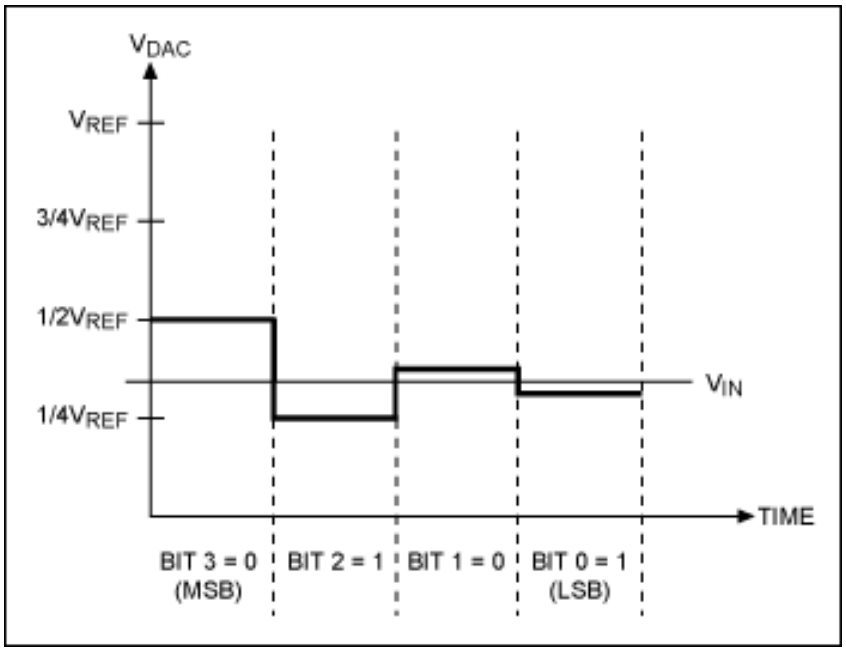


2.6mm x 3.2mm

Three submissions were done (two to develop core ADC) to get final chip

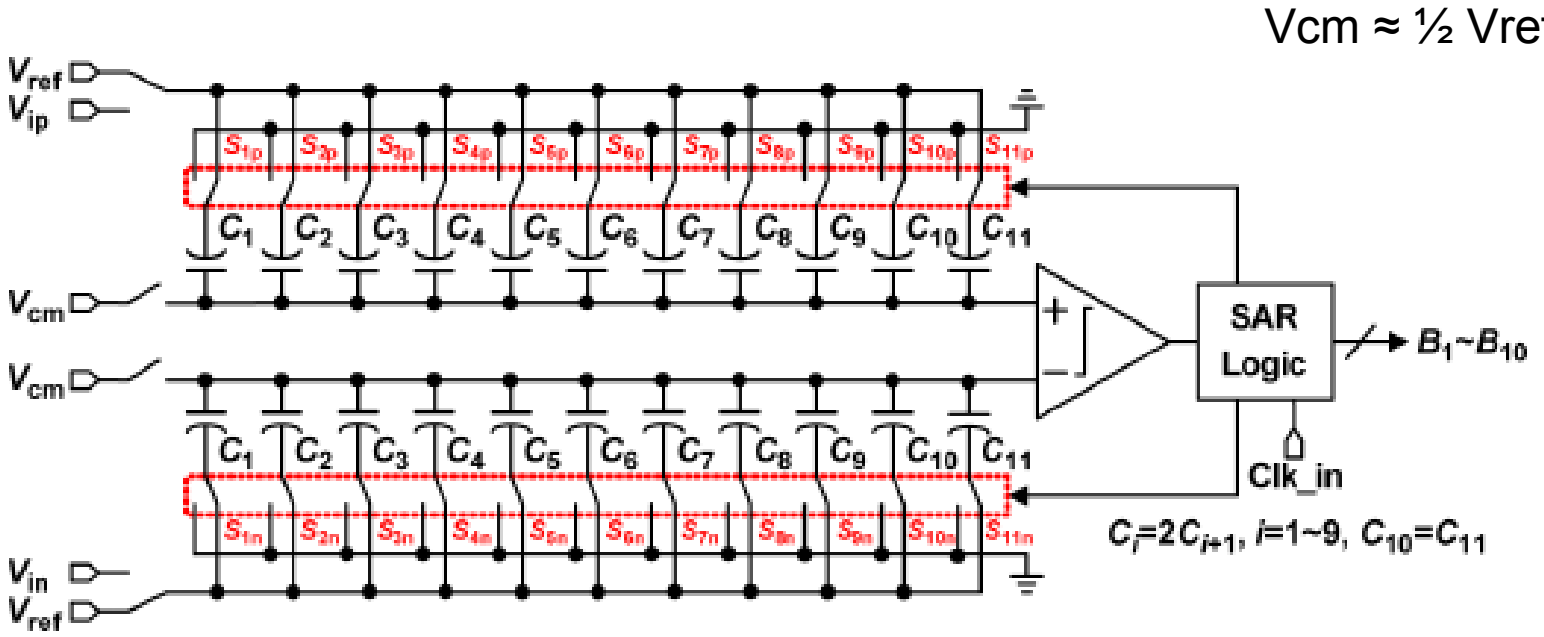
Idea of Successive-Approximation-Register (SAR) ADC





- Conversion done in a loop utilizing single comparator and DAC
- Simpler and more energy efficient comparing to pipeline ADC

Conventional differential SAR ADC



- In first sampling step – sampling – comparator is connected to Vcm
- 10 bit ADC but 11 capacitors and 11 steps

SAR ADC properties

• Power and area-efficient architecture – the same circuitry is used N-times (for N-bit ADC) to approximate the input voltage

• Only one comparator, two DACs and SAR logic needed – fits well to modern digital CMOS

• Limited sampling rates - but with modern CMOS technology (~100nm) up to ~100MSps 10-bit ADCs were reported

- next conversion cannot be started before completion of previous one
- sampling time adds to conversion time (not like in pipeline)

•Comparator – the only analog block

• DAC network serves as sampling capacitance

• Simple digital logic

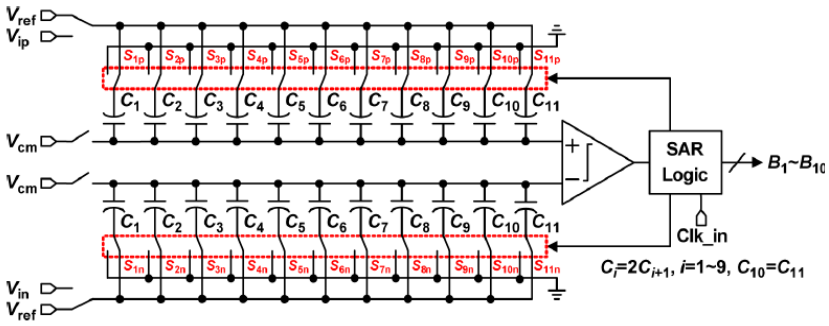
• Fully differential implementation increases the resistance to disturbances

Power consumption in SAR depends mainly on switching scheme

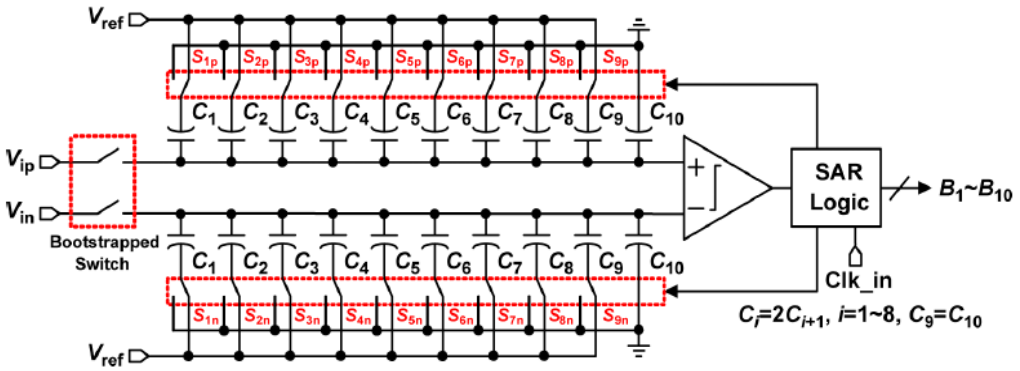
- With CMOS technology scaling digital power consumption is decreasing rapidly – so minimizing analog power (DAC, comparator) is of main interest
- Huge progress has been obtained in the last ~10 years in optimizing capacitive DAC configurations and their switching schemes
- Various DAC switching configurations were proposed
  - Conventional (100% power consumption)
  - 2 step switching (~10% power saving)
  - Charge sharing (~24% power saving)
  - Split capacitor (~37% power saving)
  - Energy saving (~56% power saving)
  - Set and down (~81% power saving)
  - Vcm-based (~87% power saving)
  - Merge Capacitor Switching (MCS) (~93% power saving)
  - Last half year some new were proposed (up to ~98% power saving)

Switching energy – more efficient configurations
Set and down vs conventional

Conventional 10-bit SAR

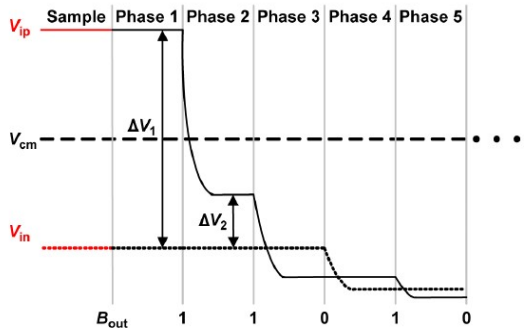


Set and down 10-bit SAR



Set and down SAR ADC:

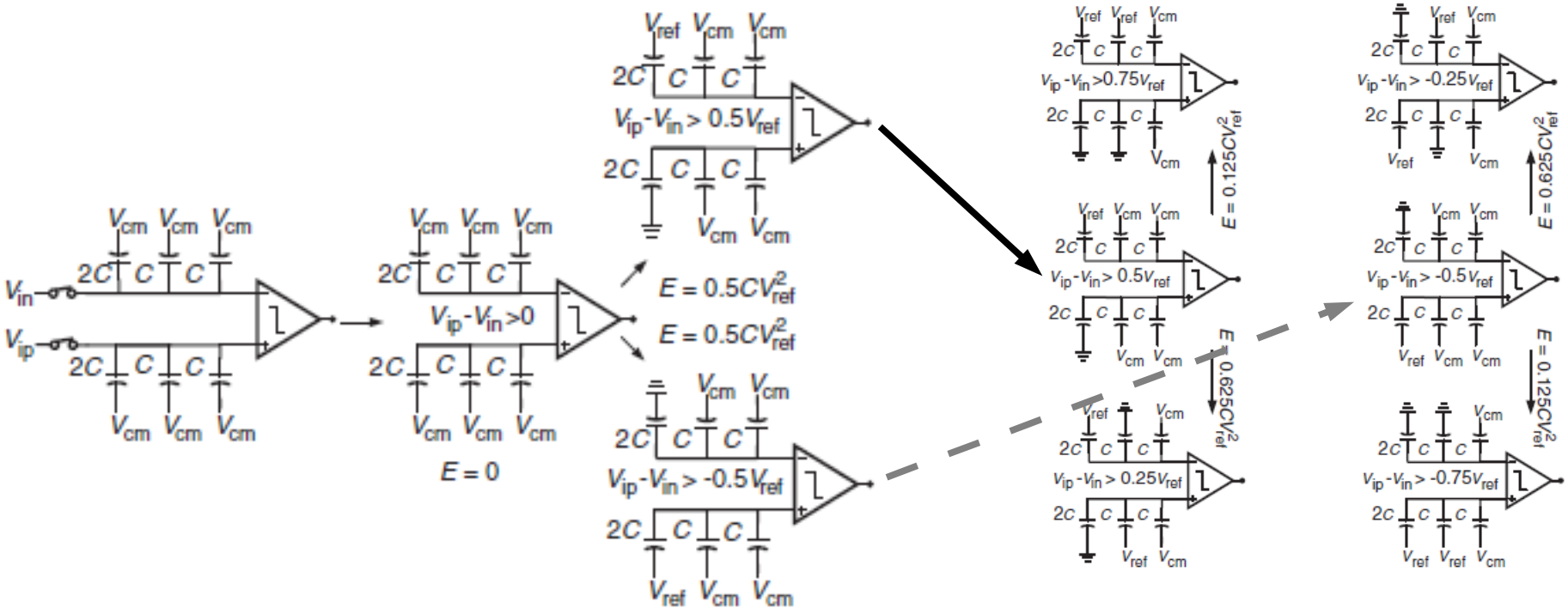
- 1st comparsion done before any switching
- 2 switching less (last capacitor to ground)
- pair of MSB capacitors smaller
- V_{in} sampled on top plate



Variable common mode...

Ch. Ch. Liu, S-J. Chang, G-Y.Huang, Y-Z. Lin "A 10-bit 50MS/s SAR ADC with a monotonic capacitor switching procedure", IEEE Journal of Solid-State Circuits v.45 pp. 731-740, April 2010

Switching energy – more efficient configurations
Merge Capacitor Switching (MCS) SAR ADC

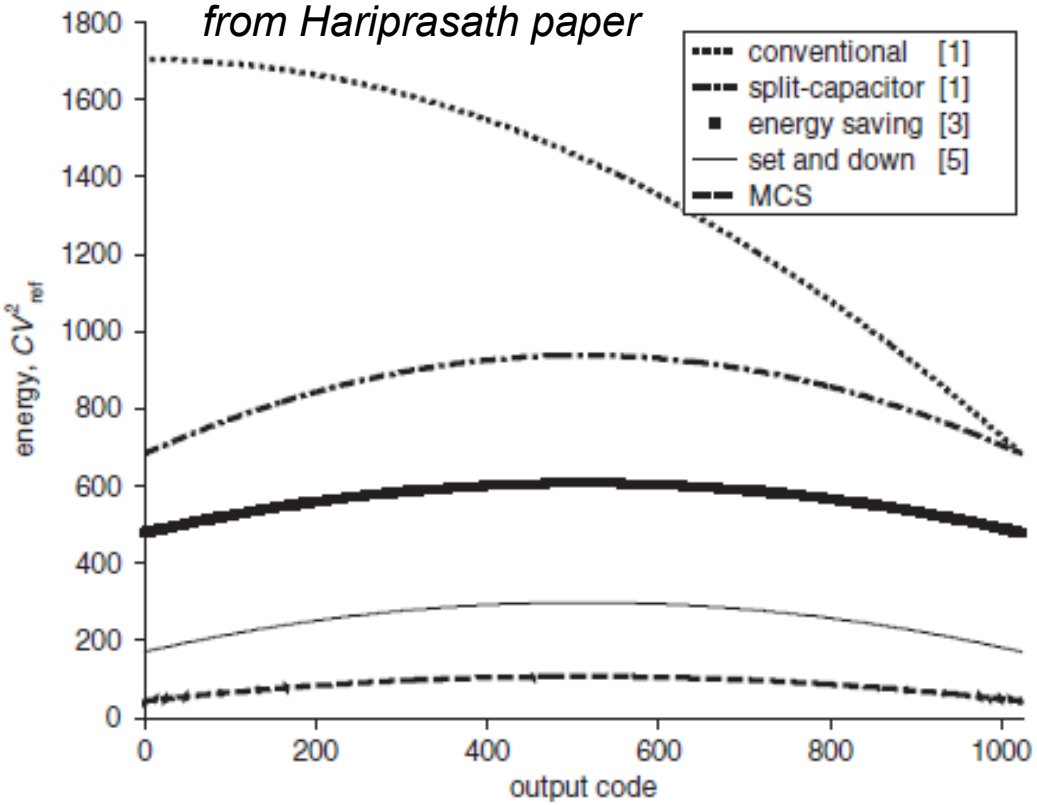


Switching energy ~93% less than conventional SAR ADC

Such switching scheme is used in our present design

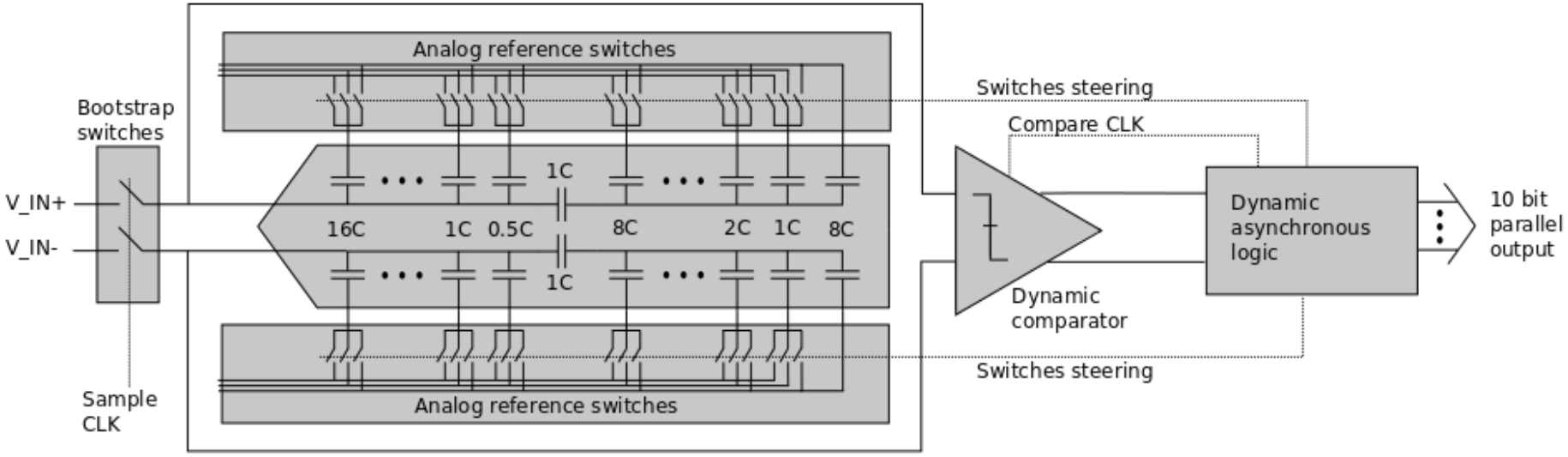
V. Hariprasath, J. Guerber, S-H. Lee, U-K. Moon "Merged capacitor switching based SAR ADC with highest switching energy-efficiency", Electronics Letterss v.46 No.9 April 2010

SAR switching energy
Merge Capacitor Switching (MCS)...



Within last ~half year new papers with even more efficient schemes were published...

Split DAC Architecture (our 10 bit ADC)

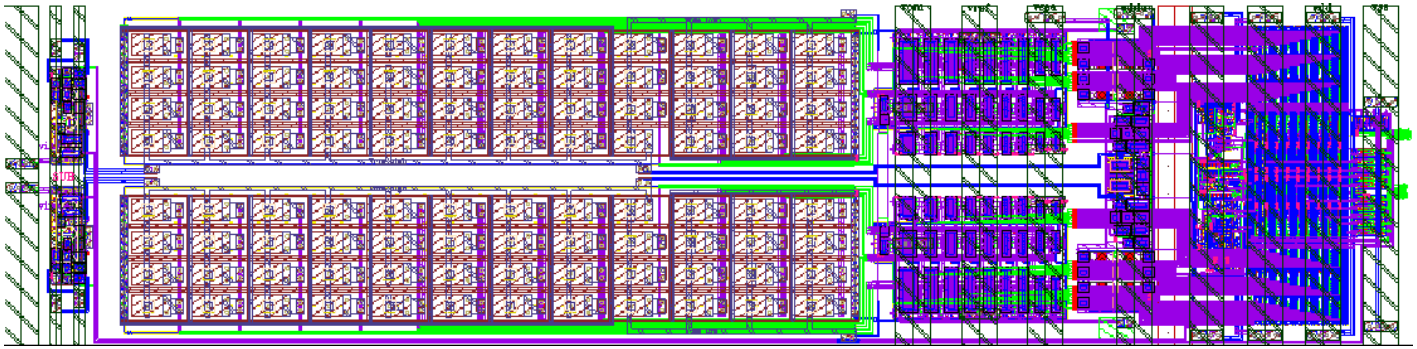


- Additional capacitor in the middle of DAC
- $C_{tot} \approx 56C_{min} < 2^6 C_{min}$; set and down $C_{tot} \approx 2^8 C_{min}$; conventional $C_{tot} \approx 2^9 C_{min}$;

Design of SAR ADC
Implementation issues

- Split DAC architecture
  - allows using higher unit capacitance for the given total DAC capacitance. It helps to bypass the problem of relatively high C_{min} available in CMOS technologies – allows to decrease the effective "LSB capacitance" and so power consumption
- Asynchronous logic
  - no fast clock needed for bit cycling
  - only sampling pulse needed for digital control
  - sampling pulse (trigger) does not need to be periodic
- Dynamic comparator
  - allows to obtain zero static power consumption and so "power pulsing" is given for free
- Bootstrapped sampling switch
  - improves ADC linearity

Design of 10-bit SAR in IBM 130nm



SAR DAC channel 600um x 146um

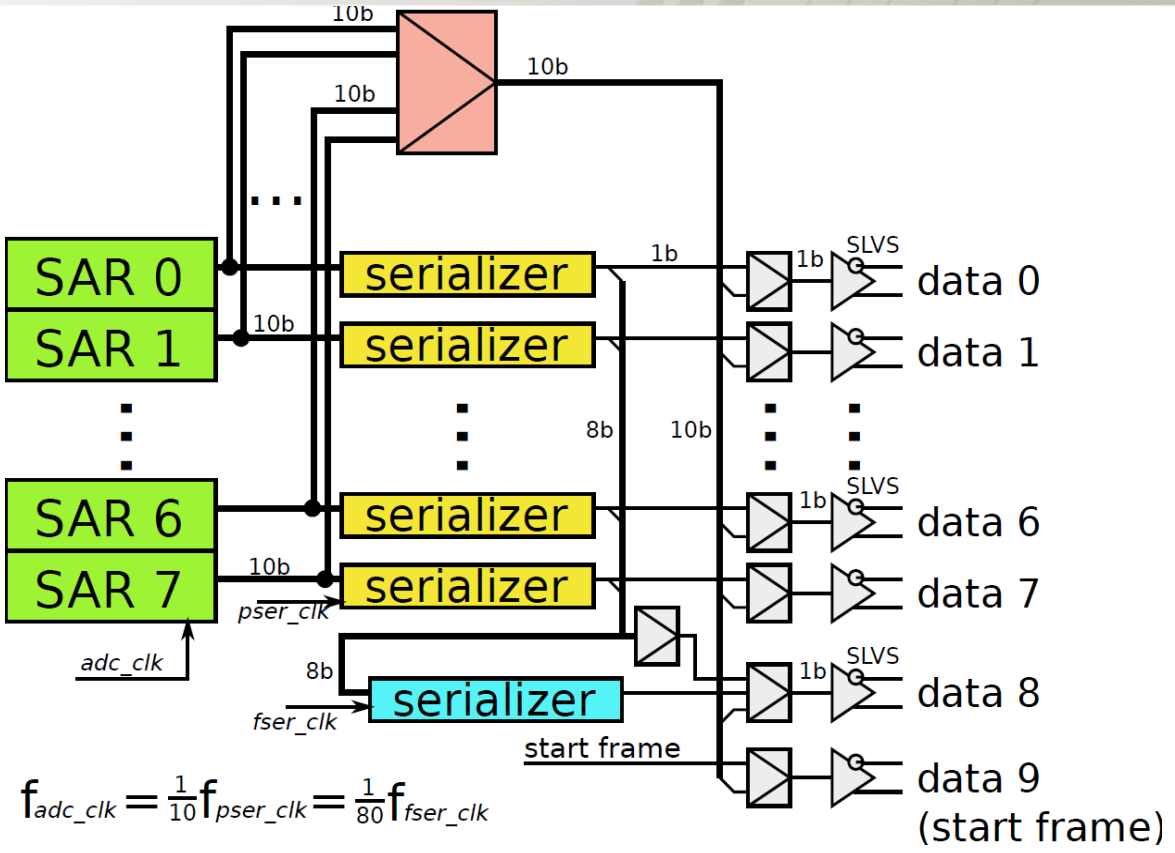
Two slightly different designs in IBM 130 nm submitted

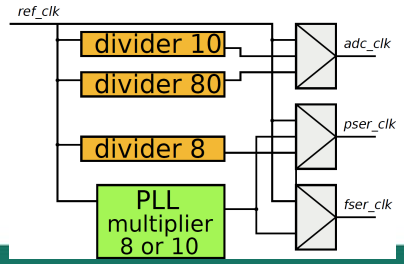
- Simulated ENOB ≈ 9.5-9.7 bits
- Maximum sampling rate ~50 MS/s
- Power consumption ≈ 1-1.4mW @ 40 MS/s
- Slightly different DAC capacitance splitting in 2 prototypes
- Fabricated in 2012
- Measurements in progress

Design of SAR multichannel ADC

Specifications & implementation issues:

- 8 channels of 10-bit SAR ADC
- Multimode digital multiplexer/serializer:
  - Serial mode: one data link per all channels (external clk division or PLL clk generation)
  - Parallel mode: one data link per channel (external clk division or PLL clk generation)
  - Test mode: single channnel output (max fsmp ~50 Msps)
- PLL for data serialization
- High speed SLVS interface (~1GHz)
- Power pulsing





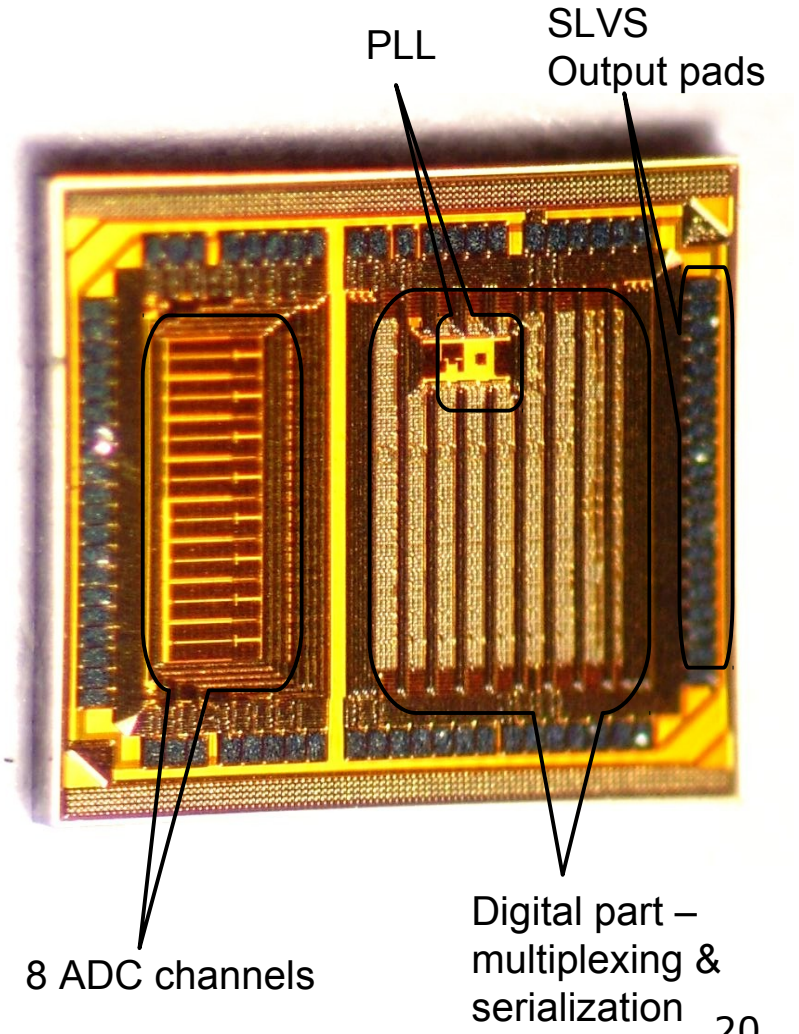
Prototypes in IBM 130nm under tests… 10-bit ADC, PLL, SLVS

Prototype of 10-bit ADC

- SAR ADC with segmented DAC
- Scalable frequency (up to ~50 MS/s) and power consumption
- Simulated power consumption 1-2mW at 40MS/s
- 146um pitch
- 2200 x 2000 um die

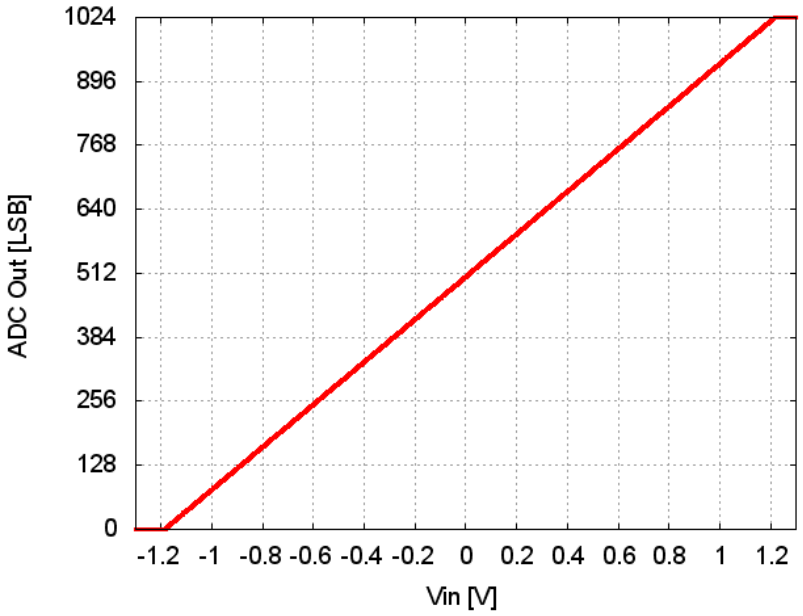
Prototype of PLL

- Type II PLL with 2nd order filter
- Scalable frequency & power
- Automatically switched VCO frequency range 8MHz – 3GHz
- VCO frequency division by 6, 8, 10 or 16
- Simulated power consumption ~1mW at 3GHz

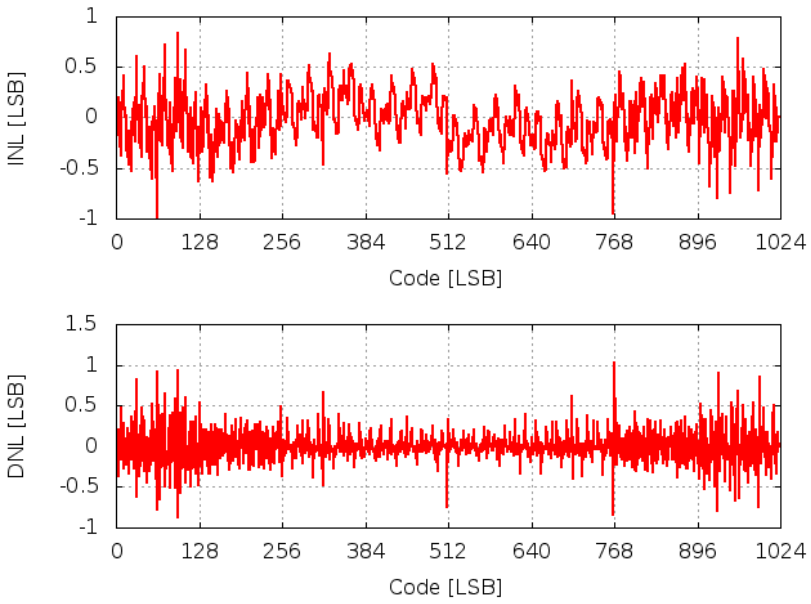


Preliminary measurements of 10-bit SAR ADC
Static measurements

Transfer function

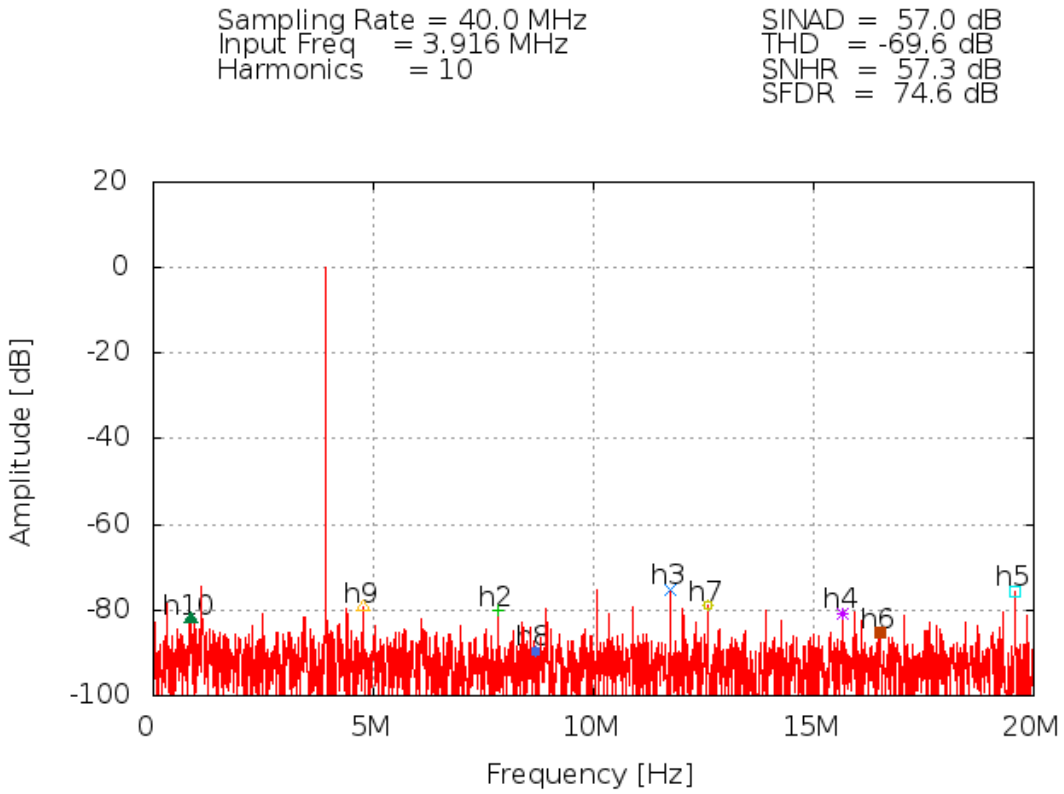


INL/DNL measurements



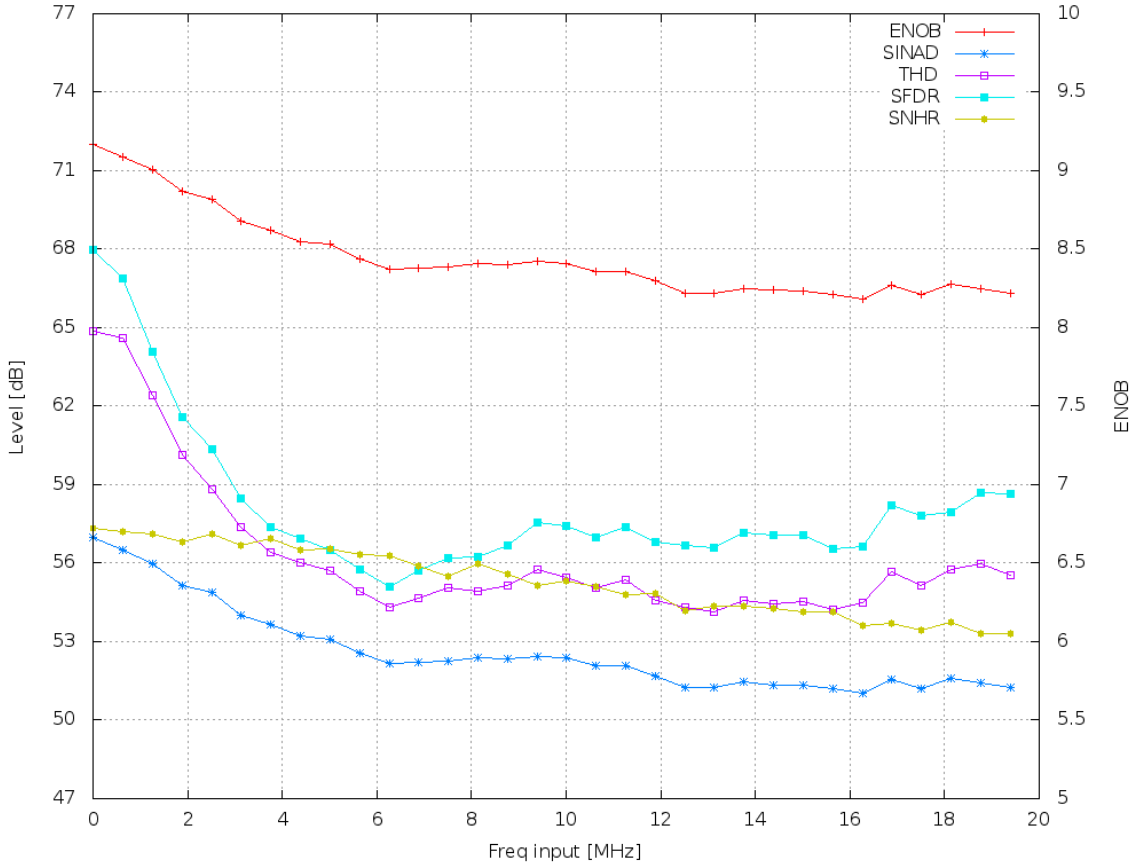
- ADC is alive and works in the whole input signal range
- There are some codes with worse linearity (to be investigated...)

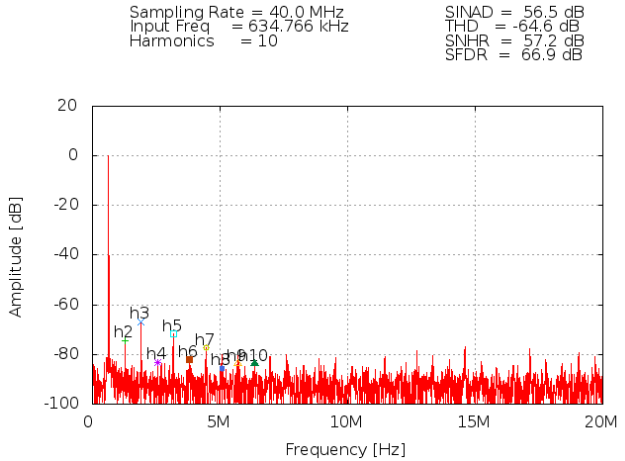
Preliminary measurements of 10-bit SAR ADC Dynamic measurement at 40Ms/S

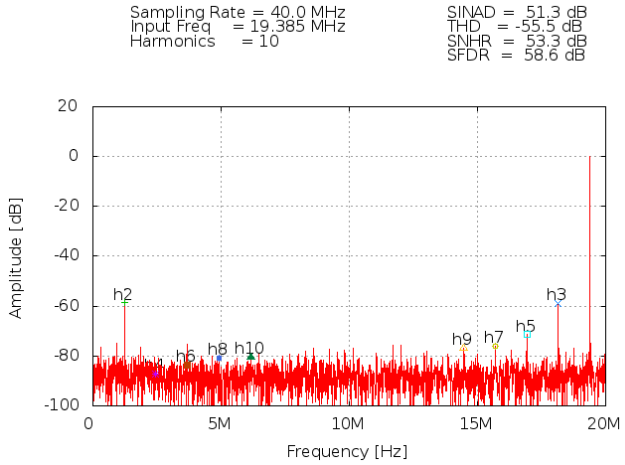


- First dynamic measurements show that ADC is fully functional and gives reasonable resolution results
- Quantitative measurements in progress...

Preliminary measurements of 10-bit SAR ADC
Dynamic measurements – f_{in} scan



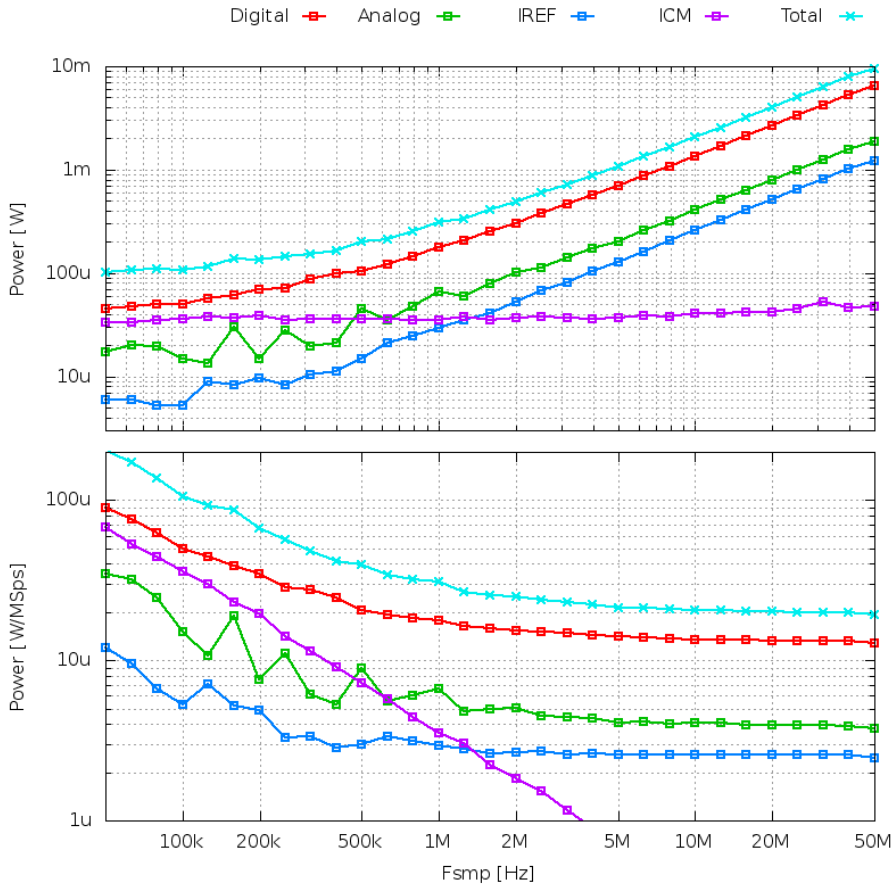




- For low f_{in} ENOB of >= 9.2 was measured
- It is suspected that ENOB decrease with f_{in} is partially/mainly due to setup

Preliminary measurements of 10-bit SAR ADC
Power consumption vs sampling frequency

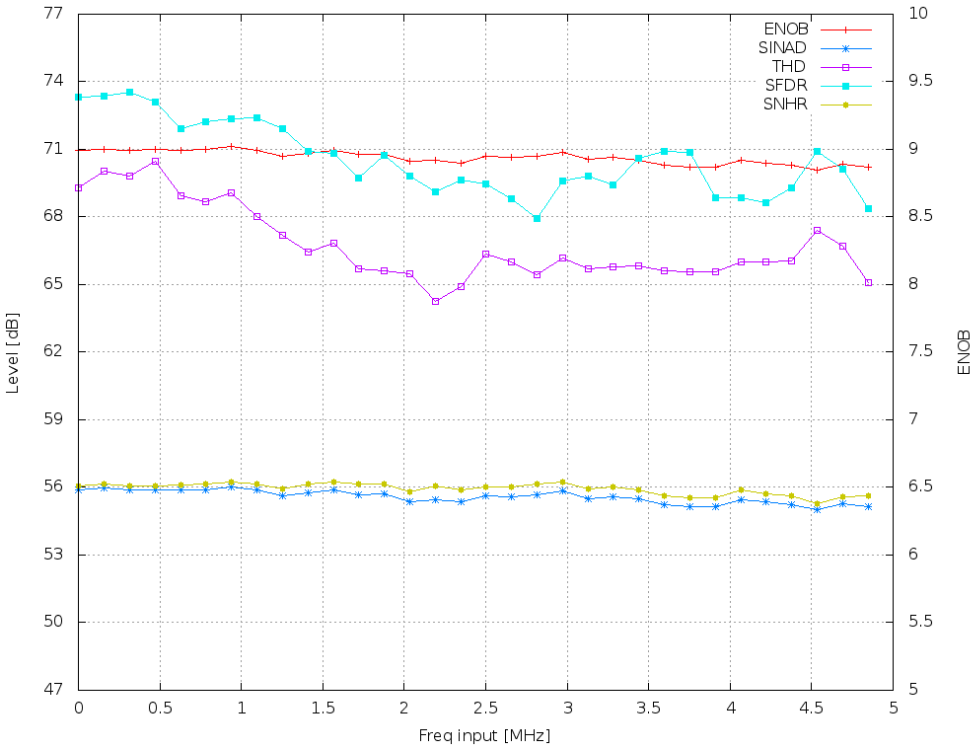
- Power measured for 8 ADC channels
- At 40MS/s power consumption is about 1 mW per channel – in agreement with simulations



Summary

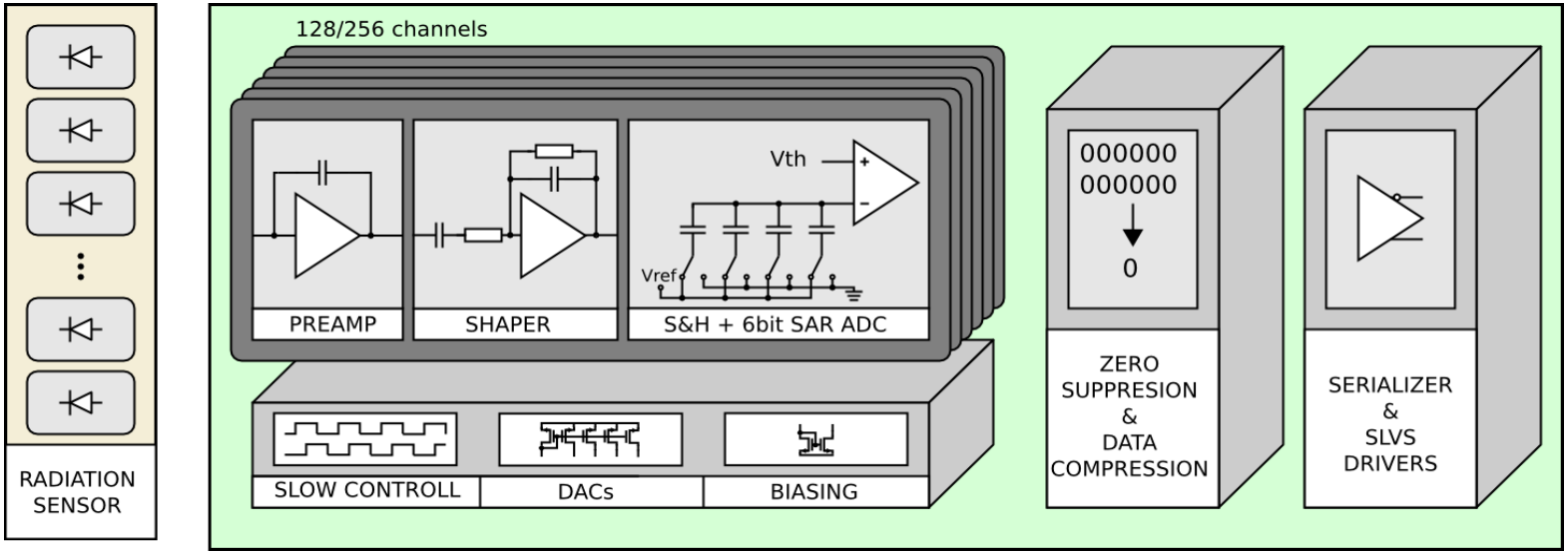
- Multichannel ADC in AMS 0.35um developed and working well in LumiCal detector module in test beams
- Very low power multichannel SAR ADCs (10-bit) developed and fabricated in IBM 130 nm
- PLLs, SLVS, etc... developed as well
- First measurements of 10-bit SAR ADC showed that the blocks (ADC in particular) are functional
  - ENOB ~9 bits (preliminary and to be verified...)
  - Power consumption ~1mW@40MHz in agreement with simulations
- PLL works and looks promising
- SLVS works well up to above 1GHz
- Quantitative tests in progress ...

Preliminary measurements of 10-bit ADC
Dynamic measurements – fin scan



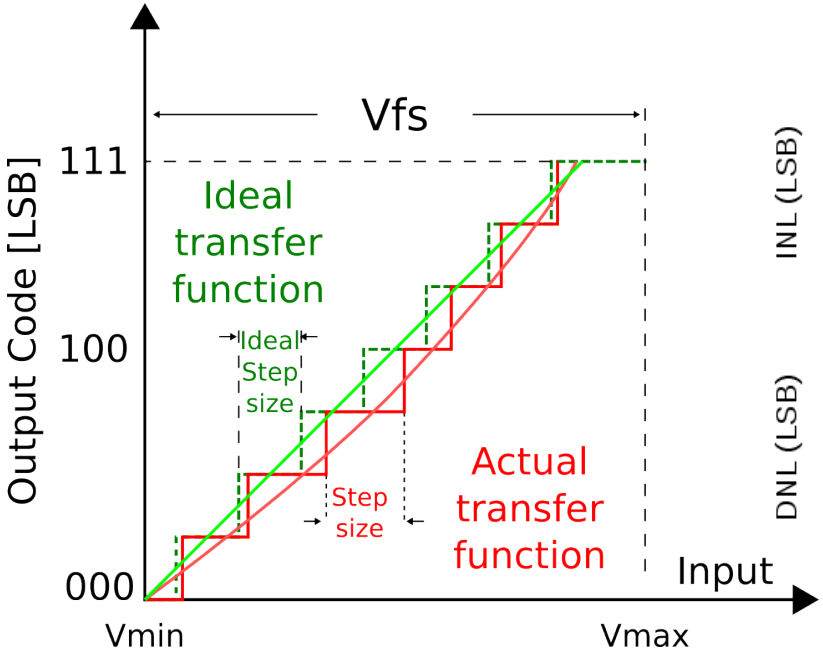
- ENOB ~ 9.2 was measured

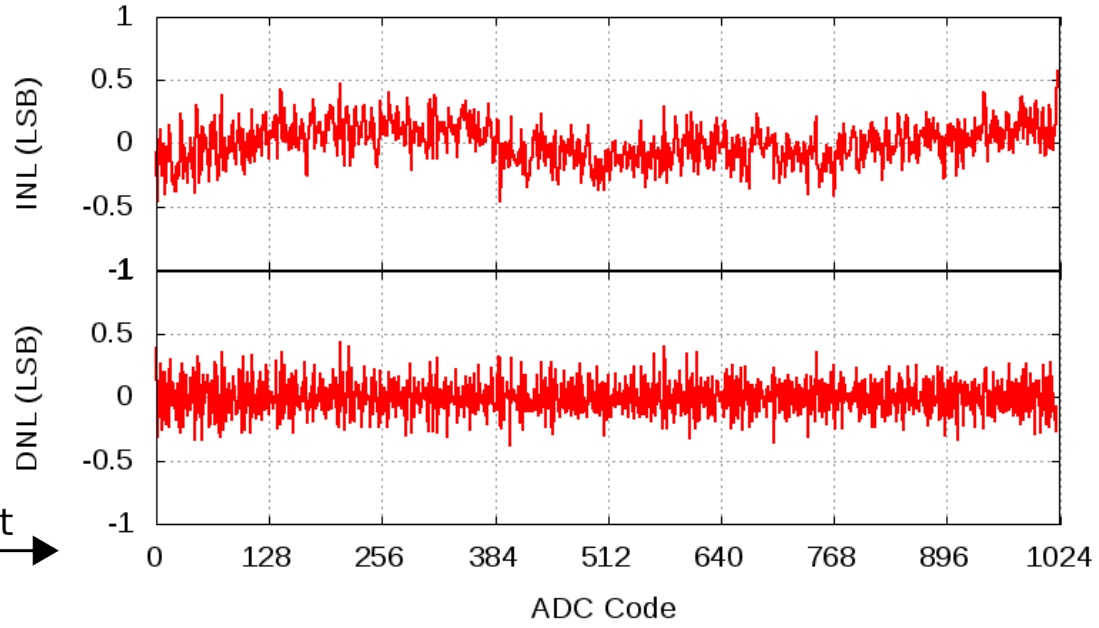
Motivation…
Multichannel readout ASIC for LHCb strip tracker



- Complex 128 channel ASIC
  - Preamplifier-shaper, 6-bit ADC, zero supp., serialization
  - Pitch ~40um
- CMOS IBM 130 nm technology
- Application in various detectors
  - TT tracker, VELO strip, IT tracker ?

ADC testing
Static measurements



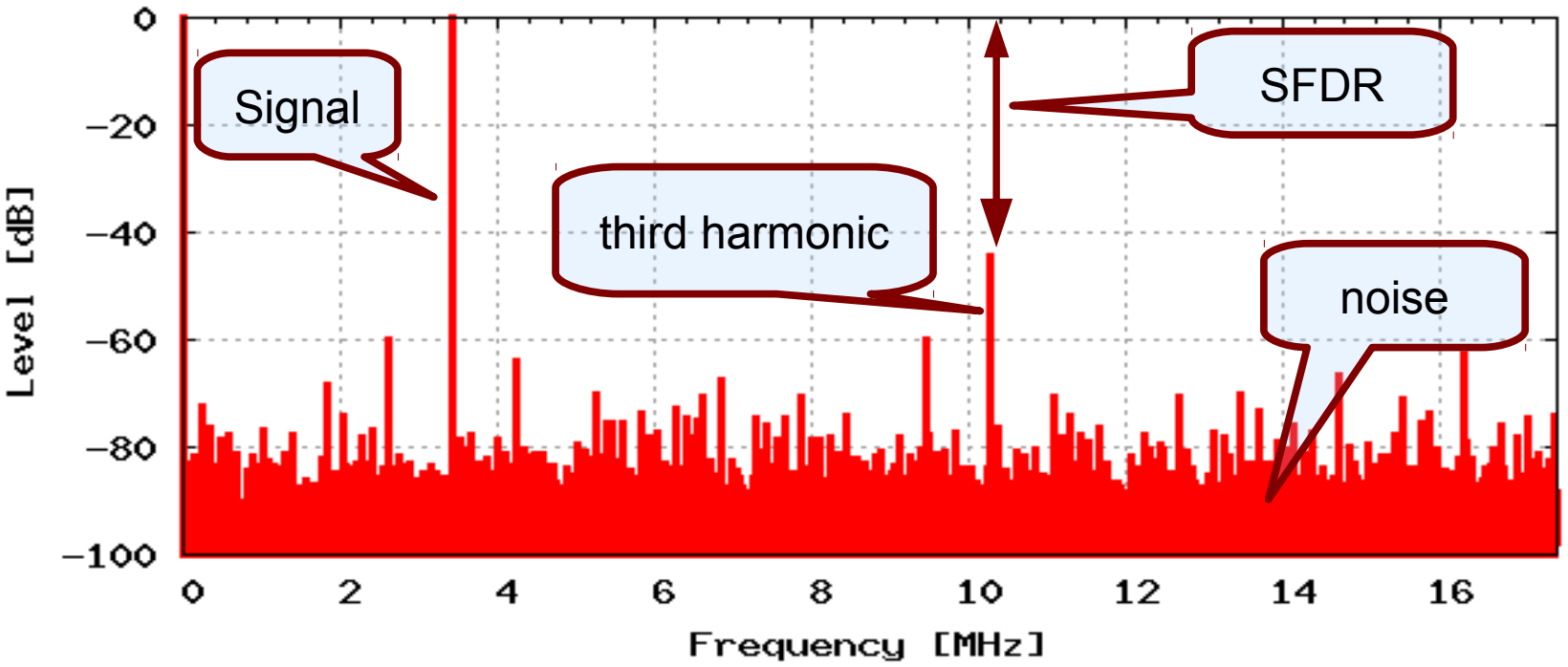


- **DNL** - Differential NonLinearity - the difference between an actual step width and the ideal step width
- **INL** - Integral NonLinearity - deviation of an actual transfer function from a straight line (integrated DNL)

ADC testing
Dynamic measurements

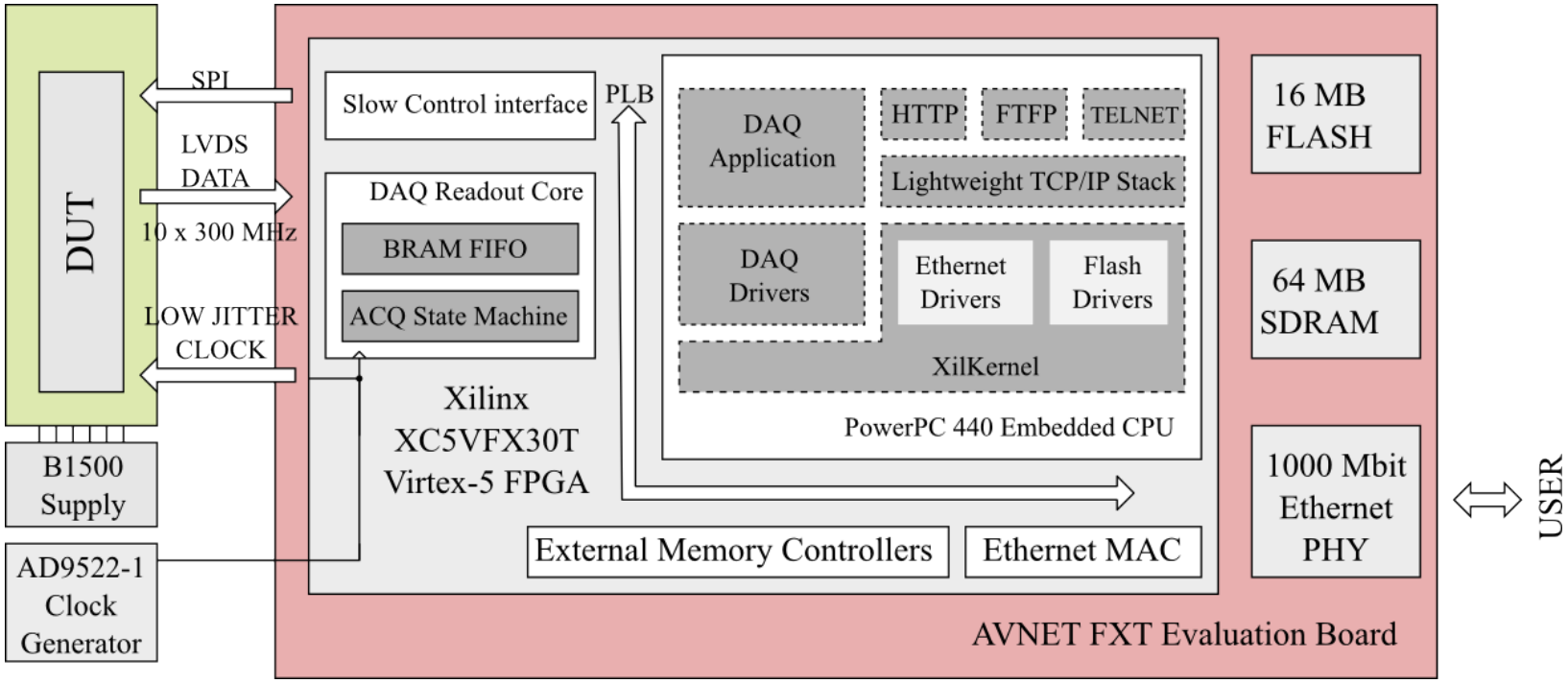
$$ENOB = \frac{SINAD[dB] - 1.76}{6.02}$$

- Single tone, full scale sine wave applied to input of the ADC
- Fourier Transform computed from the collected digital samples



- **SINAD** – Signal to Noise And Distortions
- **THD** – Total Harmonic Distortions
- **SFDR** – Spourious Free Dynamic Range
- **SNHR** – Signal to Non Harmonic Ratio

ADC testing
FPGA based test setup



- Capturing data from ADC up to 300 MHz in LVDS standard
- AD9522 external PLL used to provide low jitter sampling clock (<10ps required !)
- Other instruments (power supplies- Agilent B1500A, signal generators- Agilent 81160A) controlled via GPIB/Etherhet by the supervising PC
- Fully automatic ASIC testing