



AGH UNIVERSITY OF SCIENCE  
AND TECHNOLOGY

# SAR ADC layout consideration

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Faculty of Physics and Applied Computer Science

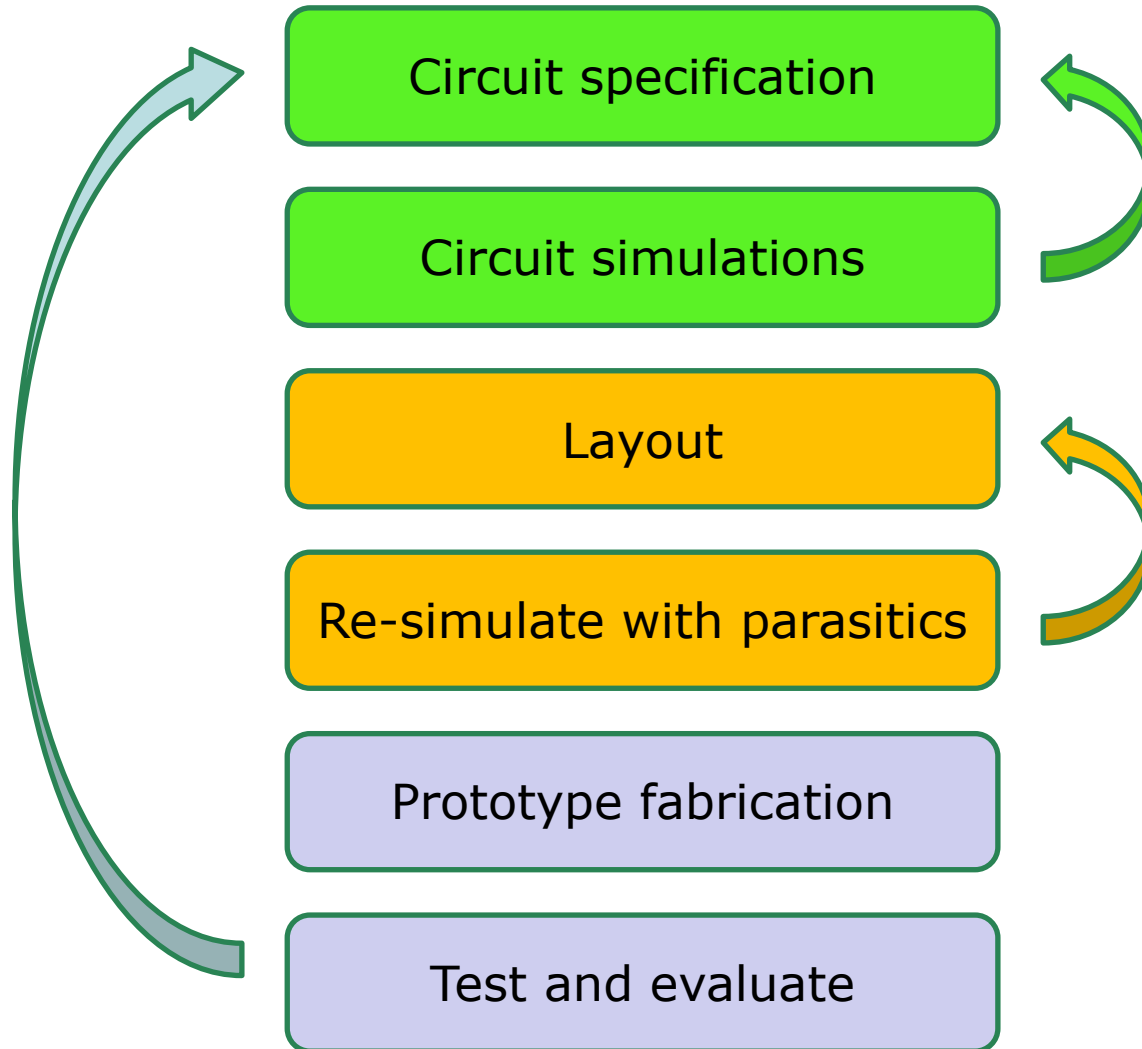
22<sup>nd</sup> FCAL Worksop , 29-30 April 2013, Kraków



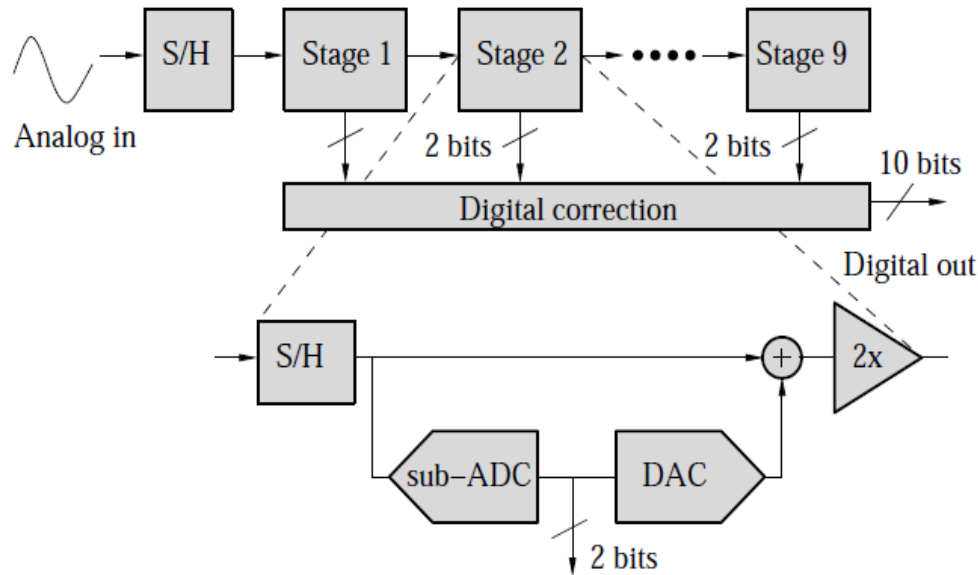
# Outline

- **CMOS IC design flow**
- **Lessons from the pipeline ADC**
- **SAR ADC layout consideration**

# Simplified flowchart for the CMOS IC design process

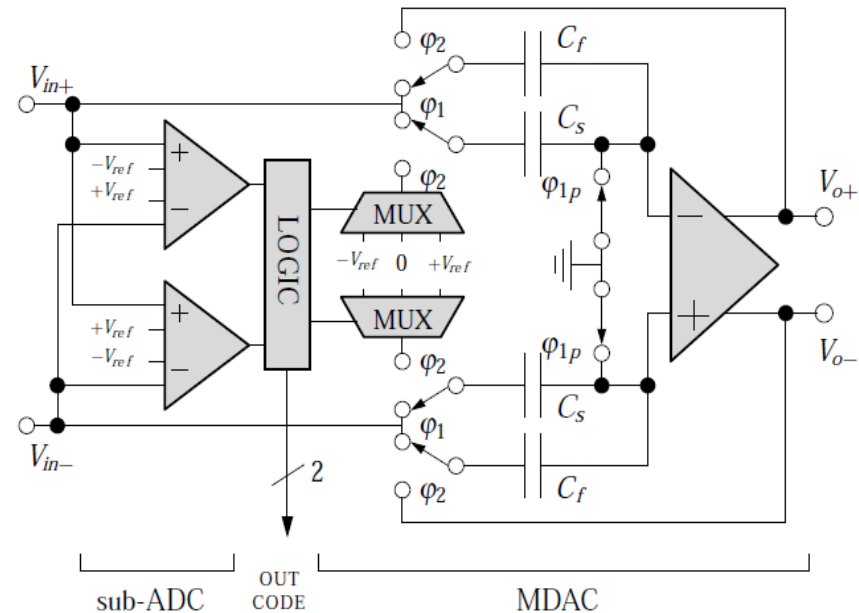


# Single channel 10-bit pipeline ADC



- Maximum sampling rate 25 Ms/s
- Scalable power consumption
- Fully differential
- Power switching OFF/ON

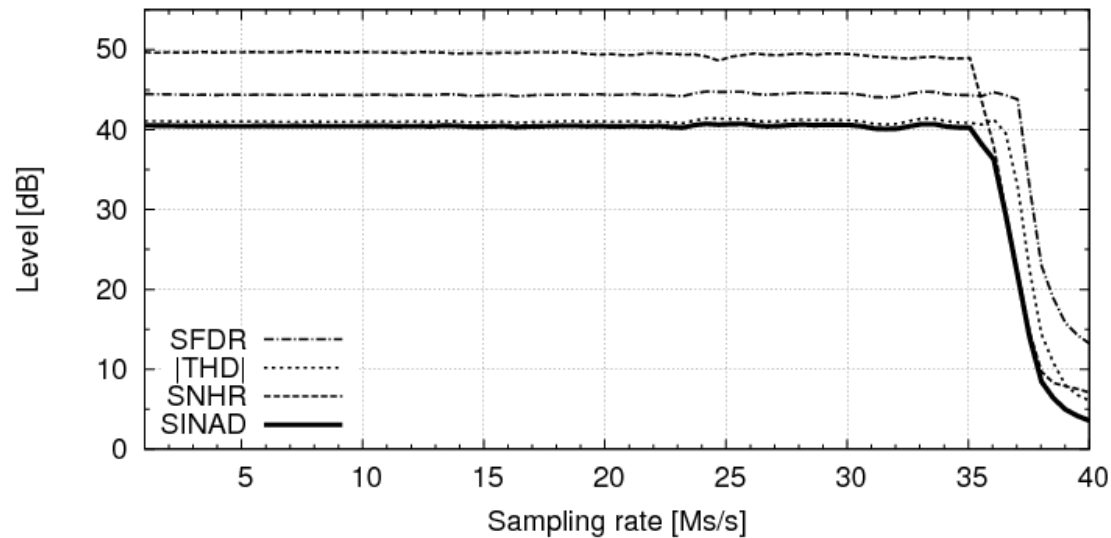
- S/H stage + 9 pipeline stages
- 1.5 bit per stage architecture



**Three submissions were done to get final chip !!!**

# Progress on pipeline ADC parameters

2009

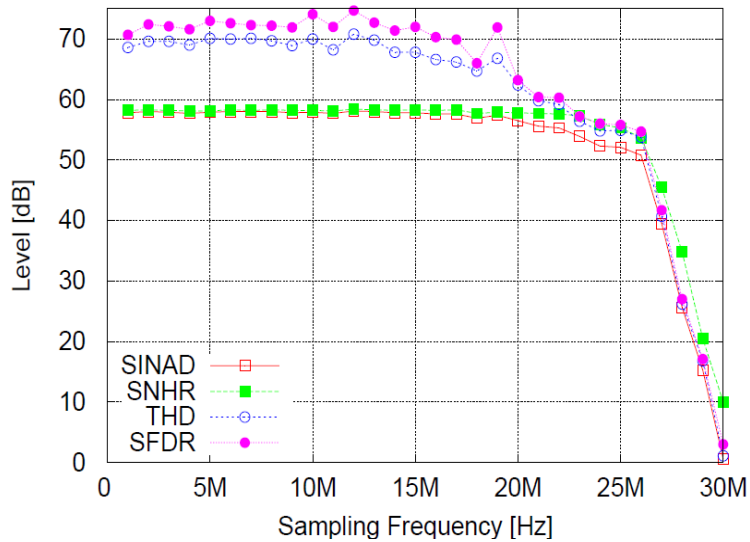


Dynamic parameters:

- SINAD = 40.4 dB
- ENOB = 6.4

# Progress on pipeline ADC parameters

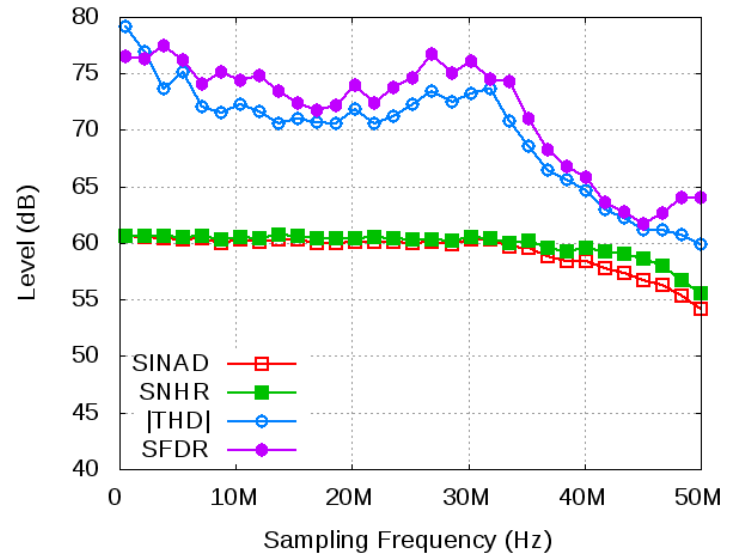
2010



Dynamic parameters:

- SINAD = 57.7 dB
- ENOB = 9.3

2011



Dynamic parameters:

- SINAD = 60 dB
- ENOB = 9.7

## Impact of the layout on pipeline ADC parameters

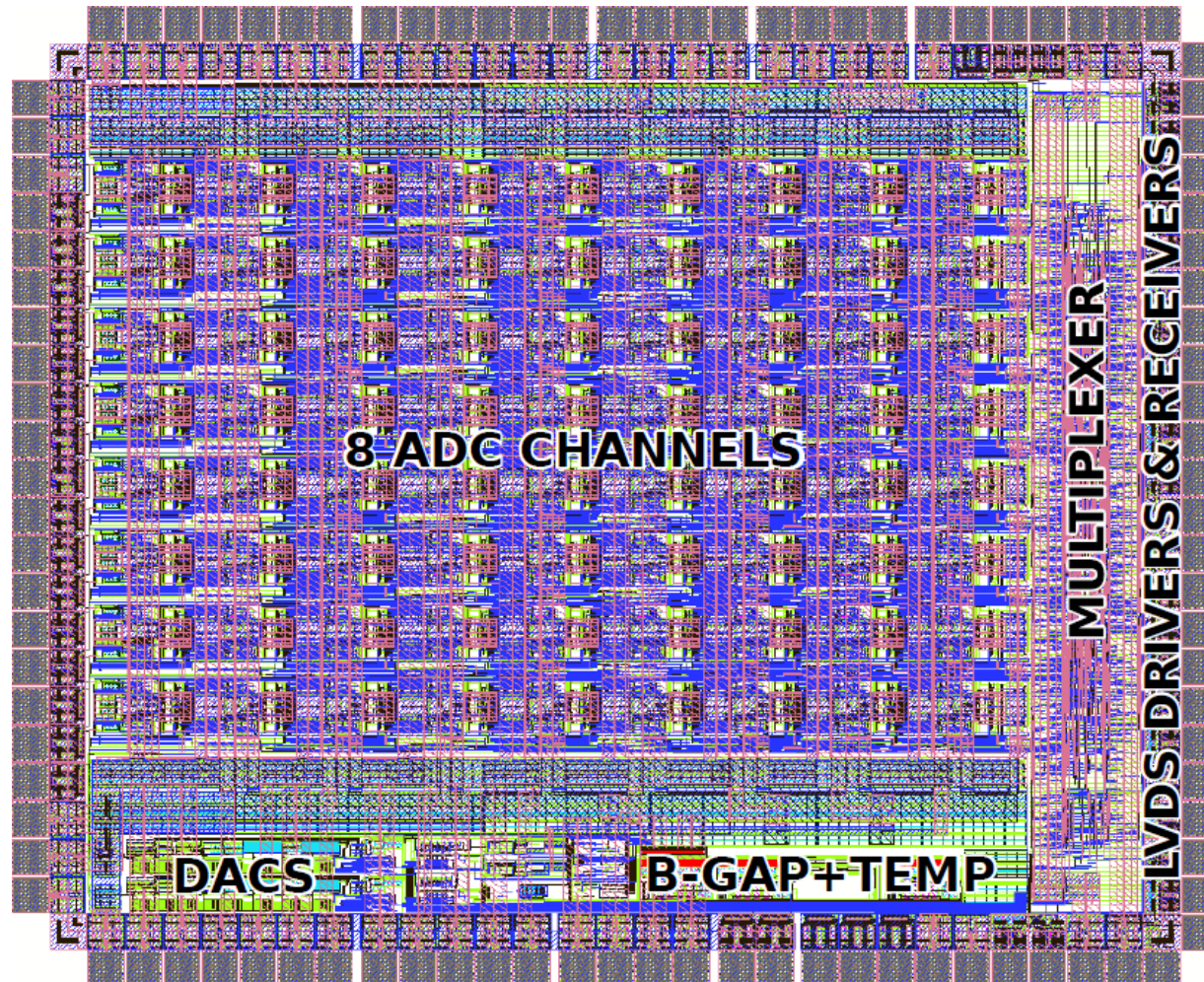
*Knowing that the performance of pipeline ADC depends in great part on the precision of multiplying by two amplifier, the most important layout issue was the matching between the sampling and feedback capacitors (including parasitics) in this amplifier. Since these capacitances are of about 500 fF, even very small parasitics (less than 1 fF) resulting from metal-to-metal path capacitance may seriously deteriorate the performance of 10-bit ADC. For this reason particular attention was given to good matching of these capacitances and elimination of their parasitics. In practice, the layout of the multiplying stage was adjusted in an iterative procedure. For each layout version, the extracted schematic diagram was generated and the post-layout simulations of ADC performance were done.*

*M. Idzik, K. Świentek, T. Fiutowski, S. Kulis, D. Przyborowski*

**A 10-bit Multichannel Digitizer ASIC for Detectors in Particle Physics Experiments.**

IEEE Transaction on Nuclear Science, vol. 59, no 2, pp. 294-302, 2012

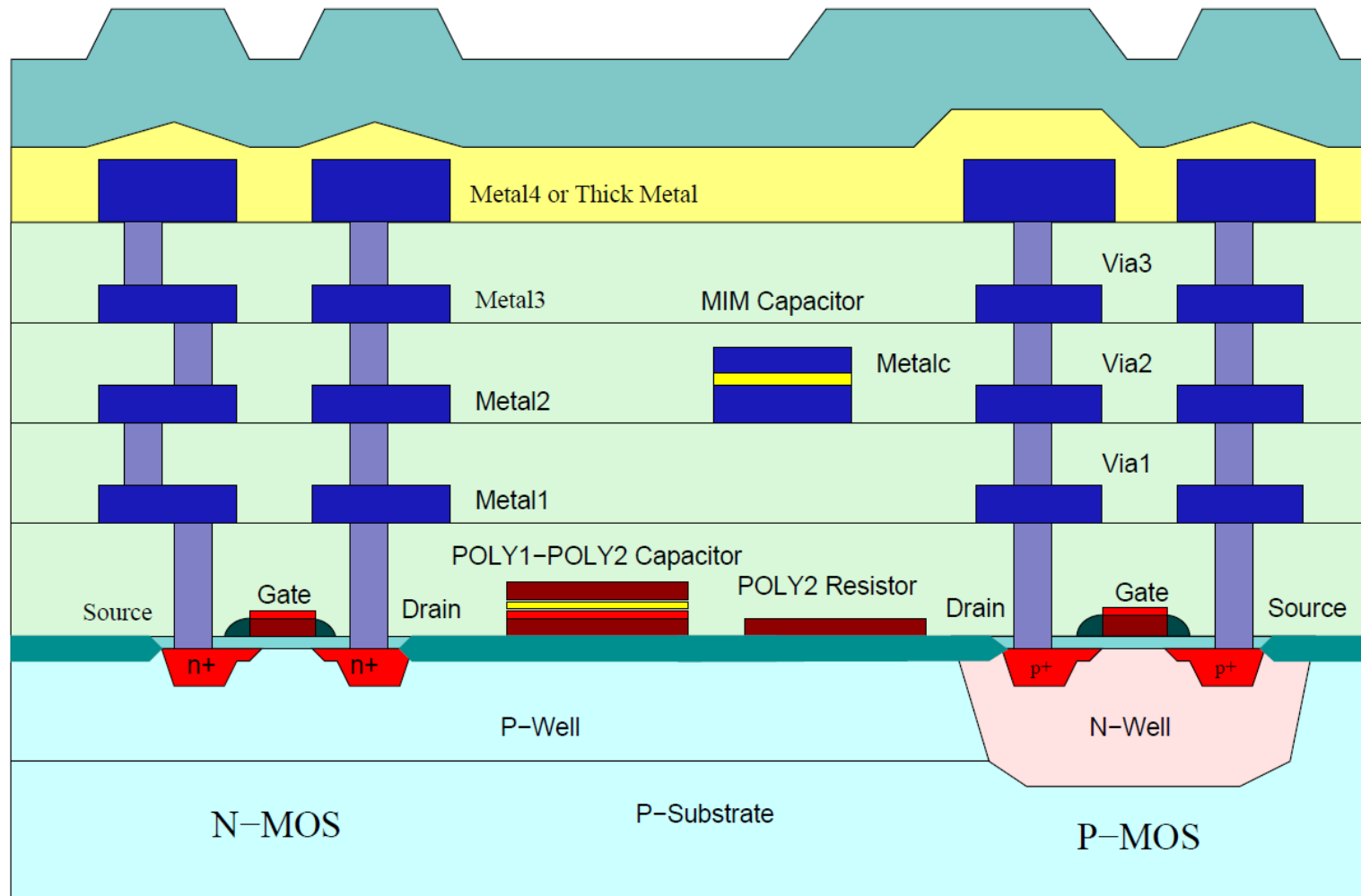
# 10-bit Multichannel Digitizer ASIC in AMS



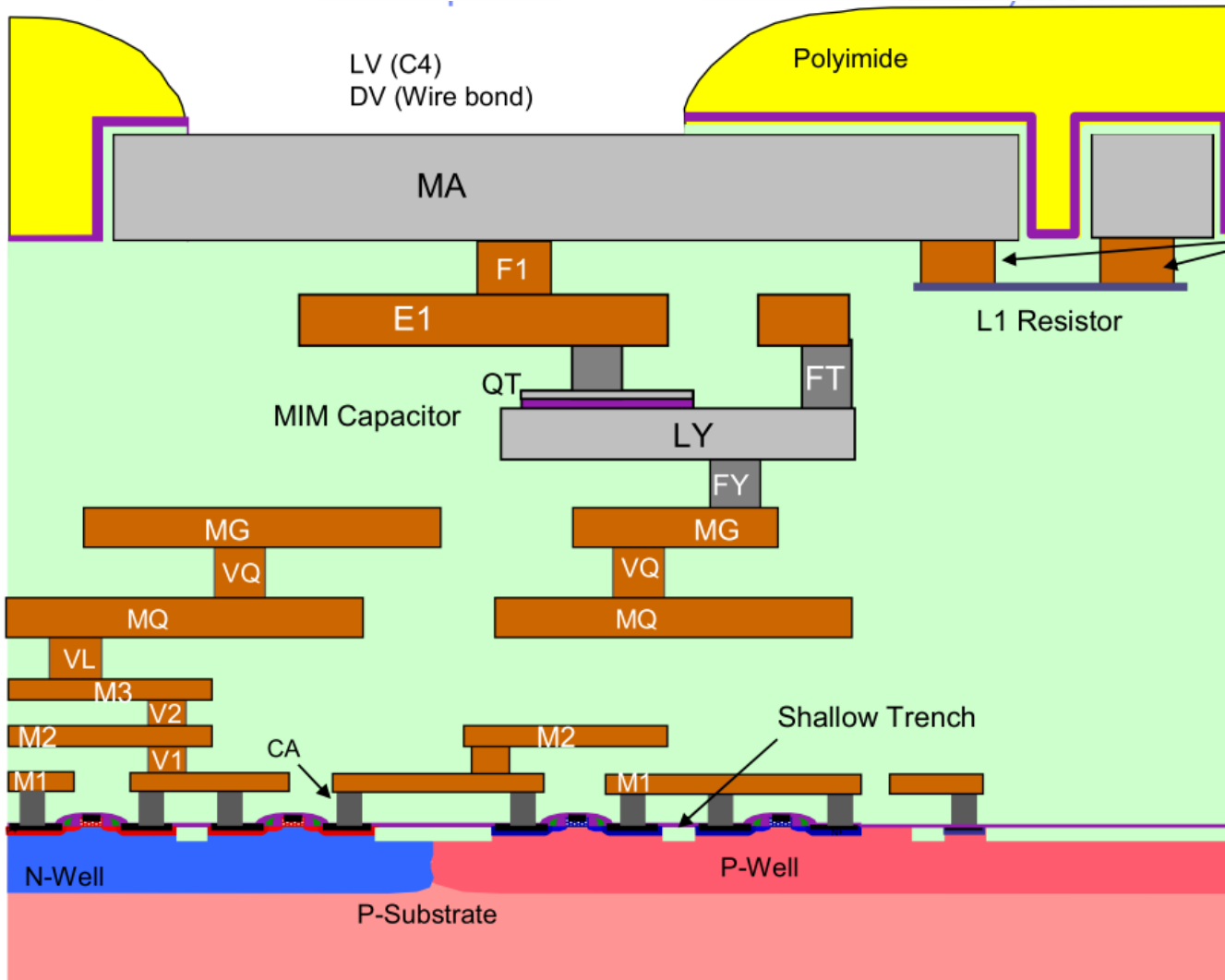
3.2mm × 2.6mm



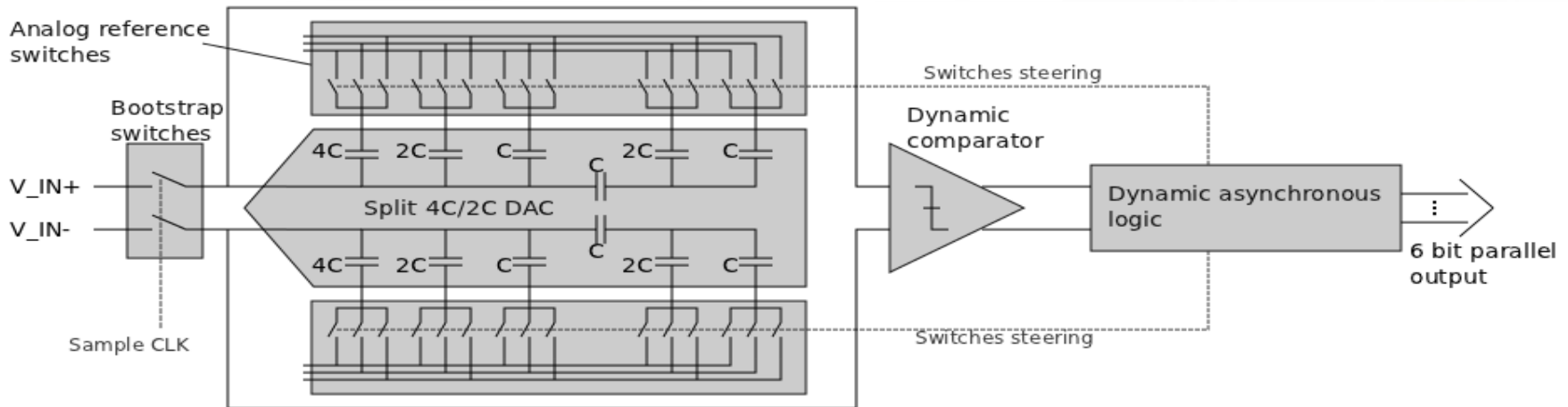
# Process Cross-Section AMS C35B4C3



# Process Cross-Section IBM CMOS8RF DM



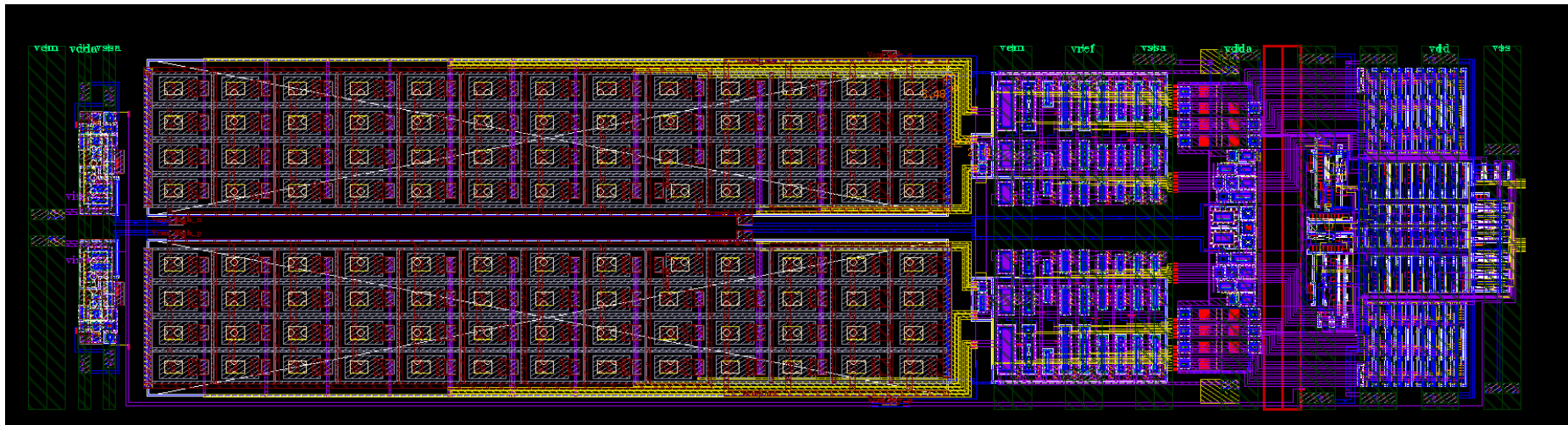
# SAR (successive approximation register) architecture (6-bit example)



- Power and area-efficient architecture – the same circuitry is used n-times (for n-bit ADC) to approximate the input voltage
- Asynchronous logic – no fast clock needed for bit cycling, only sampling signal needed
- Only one comparator per channel – small layout area
- Split DAC architecture – lower area and power consumption
- Not for ultra-high sampling rate – next conversion cannot be started before the current one is completed

# 10-bit SAR ADC in 130nm IBM

Two ADCs designed in 130nm IBM  
 Both: channel area  $\approx 0.09 \text{ mm}^2$  (146 $\mu\text{m}$  x 600 $\mu\text{m}$ )



Sampling  
switches

DACs

DACs reference switches  
& Dynamic comparator

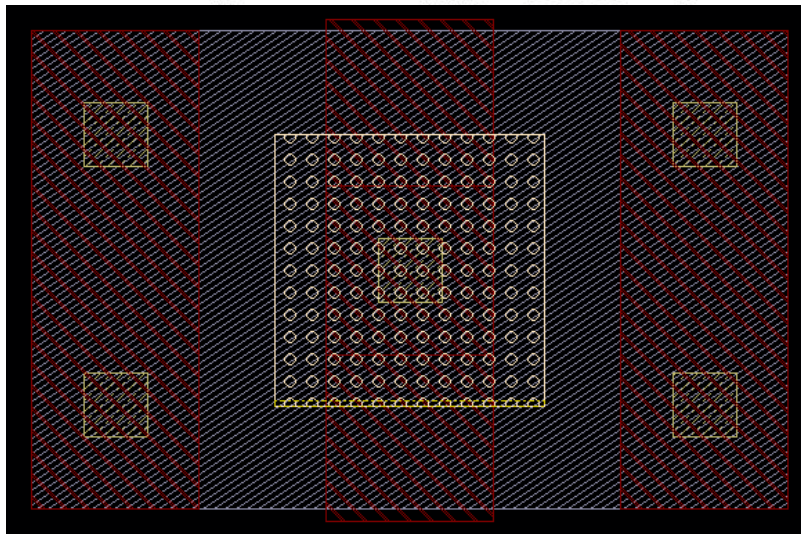
ADC logic (SAR)

- Simulated ENOB  $\approx 9.5$ -9.7 bits
- Maximum sampling rate  $\sim 50 \text{ MS/s}$
- Power consumption  $\approx 1$ -1.4mW @ 40 MS/s
- Slightly different DAC capacitance splitting in 2 prototypes
- No dummy capacitors in DAC network!

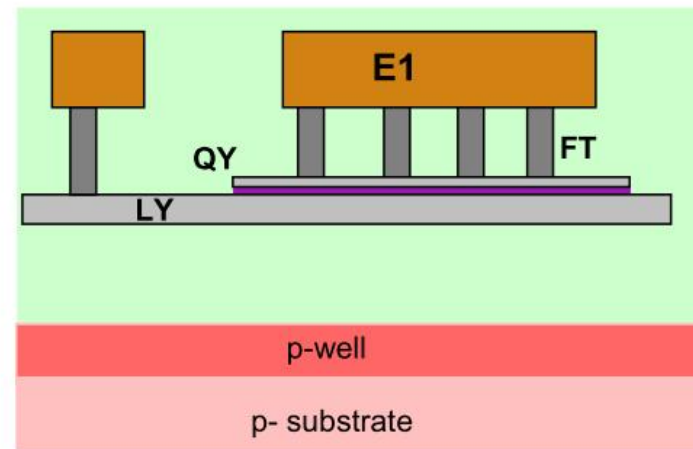
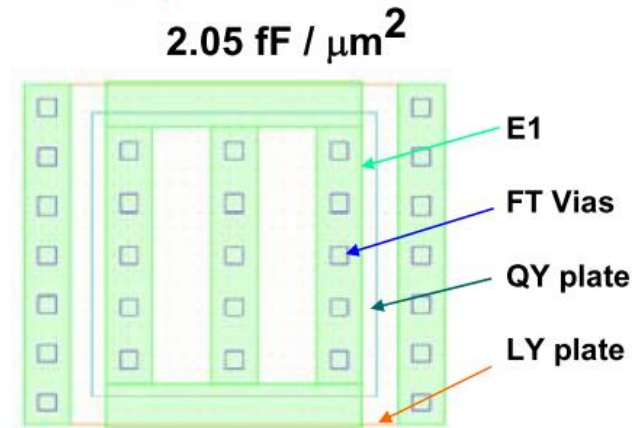
# Metal-insulator-metal capacitor

## Single HP MIM capacitor (mimcap)

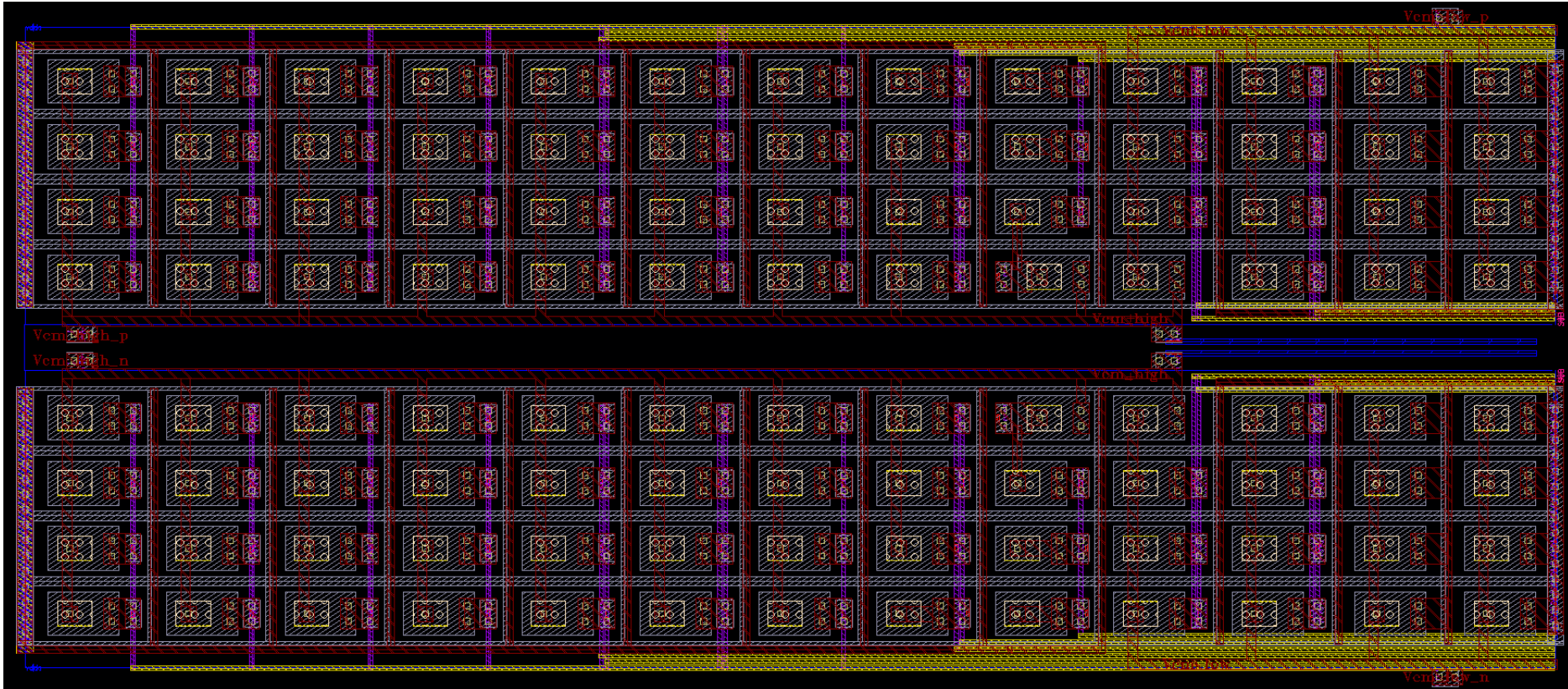
- Optional device for **DM** only
- BEOL device
  - **QY** mask
- Thin High Performance nitride dielectric with Al bottom electrode
- Aspect ratio:  $1/3 \leq W/L \leq 3$
- Min. size:  $5.24\mu\text{m} \times 5.24\mu\text{m}$



**60 fF standard P-cell**

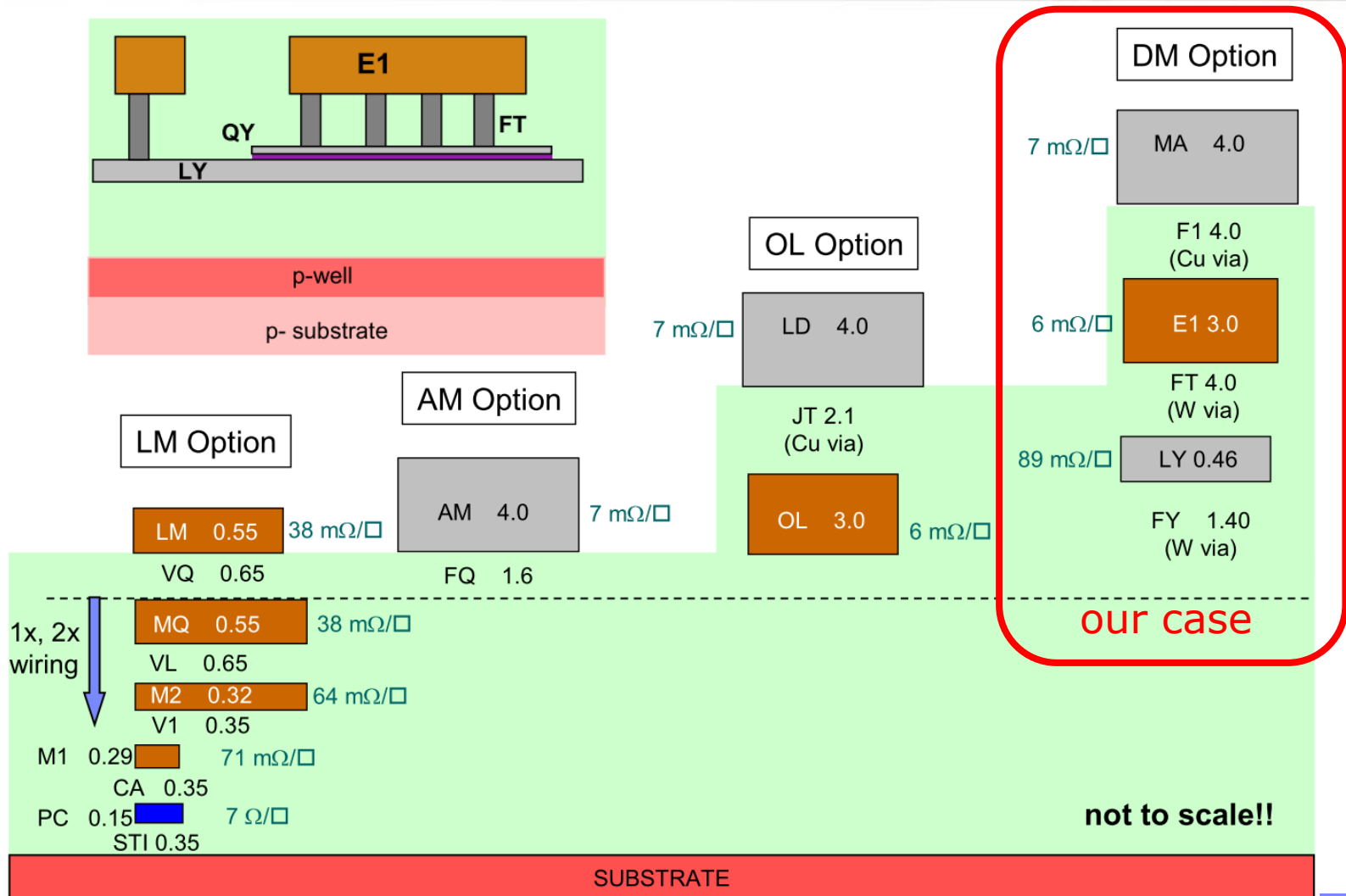


# DACs matrix

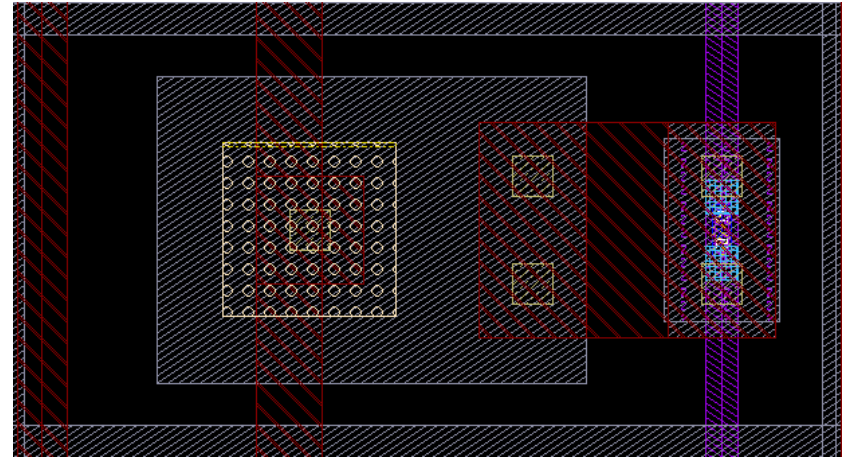
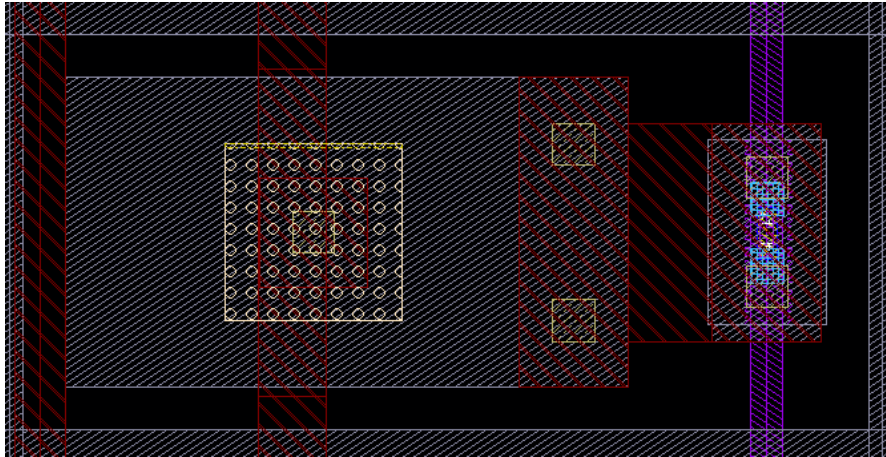


**Built of custom designed 80 fF elementary cells**

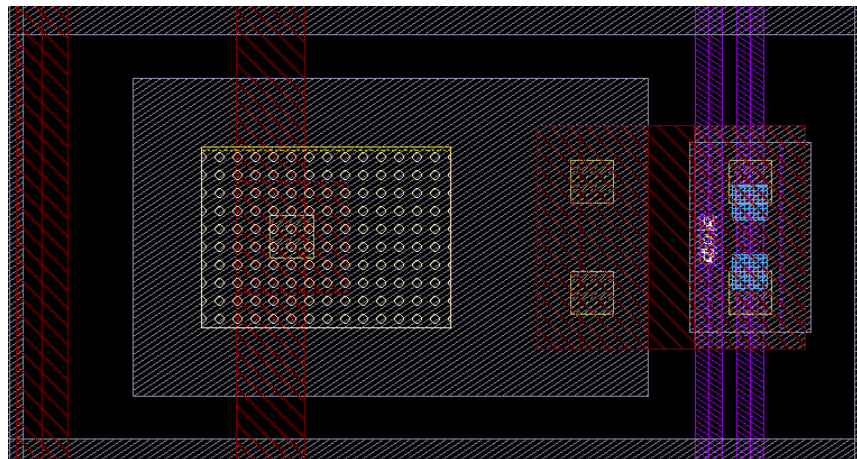
# Last metal options



# Standard vs. custom designed mimcap cell



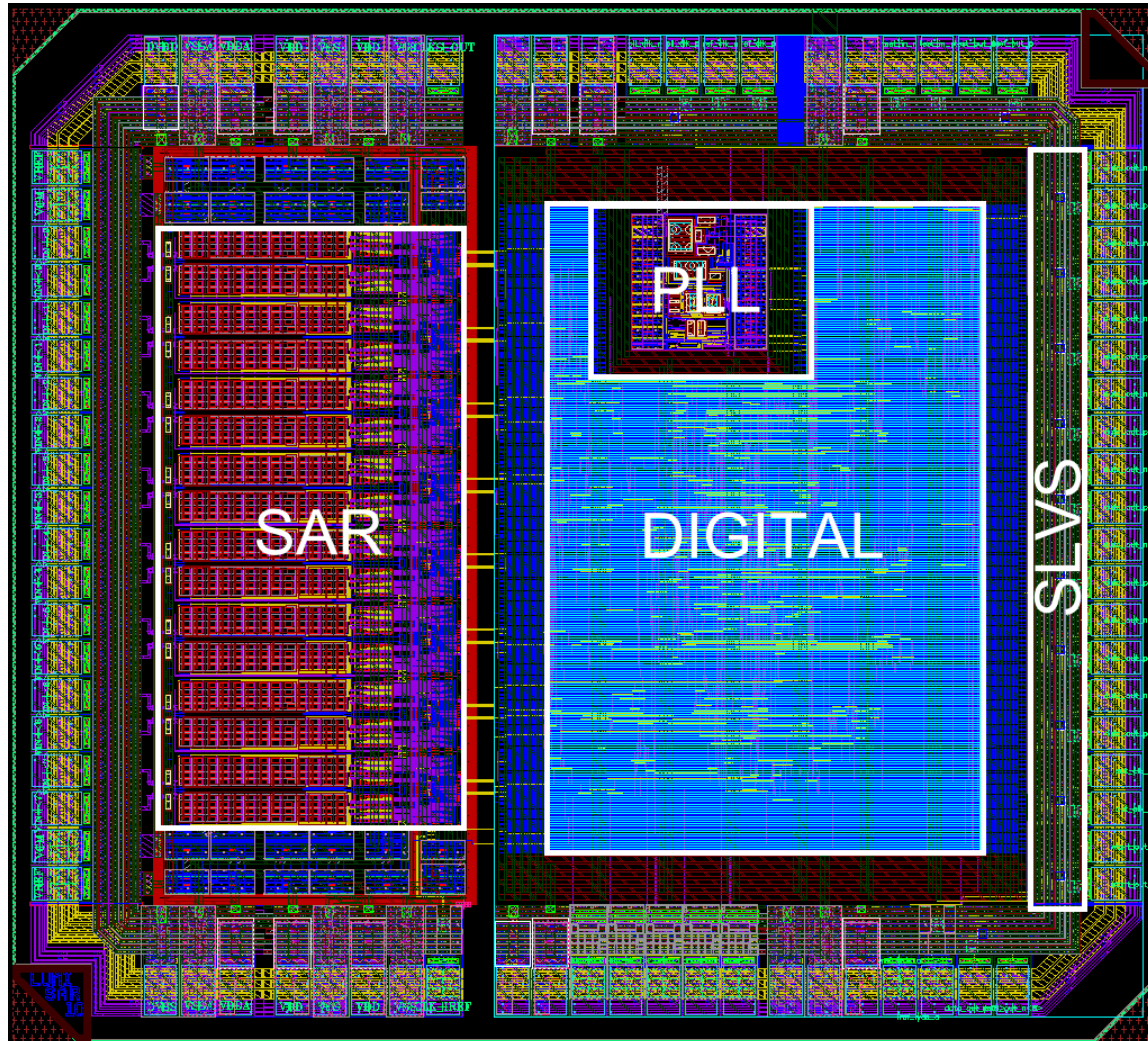
**1<sup>st</sup> prototype: two types of 60 fF cells**



**2<sup>nd</sup> prototype: 80 fF cell**



## 2<sup>nd</sup> prototype of 10-bit SAR ADC in IBM



2.2mm × 2mm

## Summary

- **ADC is fully functional and fulfils the requested specifications**
- **Preliminary measurements of the multichannel ADC are very promising**

# Process Cross-Section AMS C35B4C3

