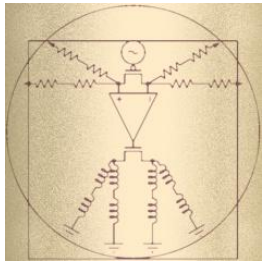

10-bit SAR ADC with configurable INL for non-linearity compensation

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FCAL Workshop 2013 – Cracow
April 29, 13:55

Outline

1. Context

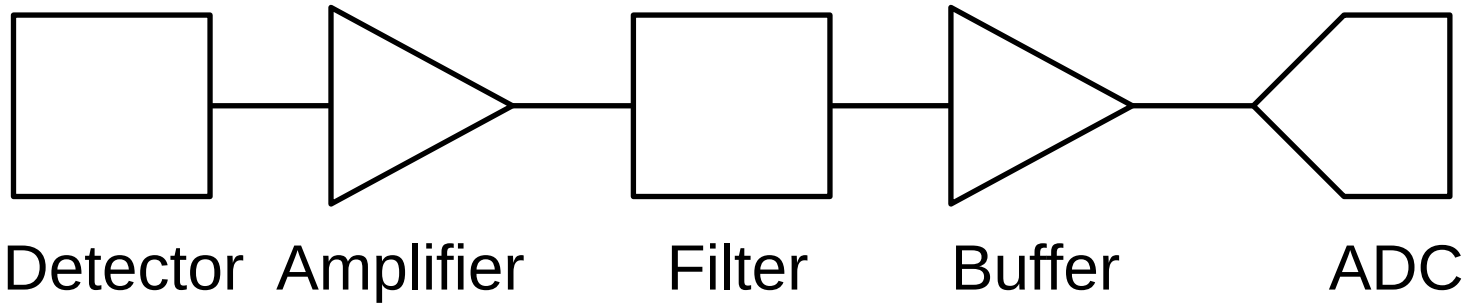
2. Advances:
   a. Front-end noise optimization guidelines
   b. Noise analysis for discrete-time filters

3. 10-bit SAR ADC with non-linearity compensation

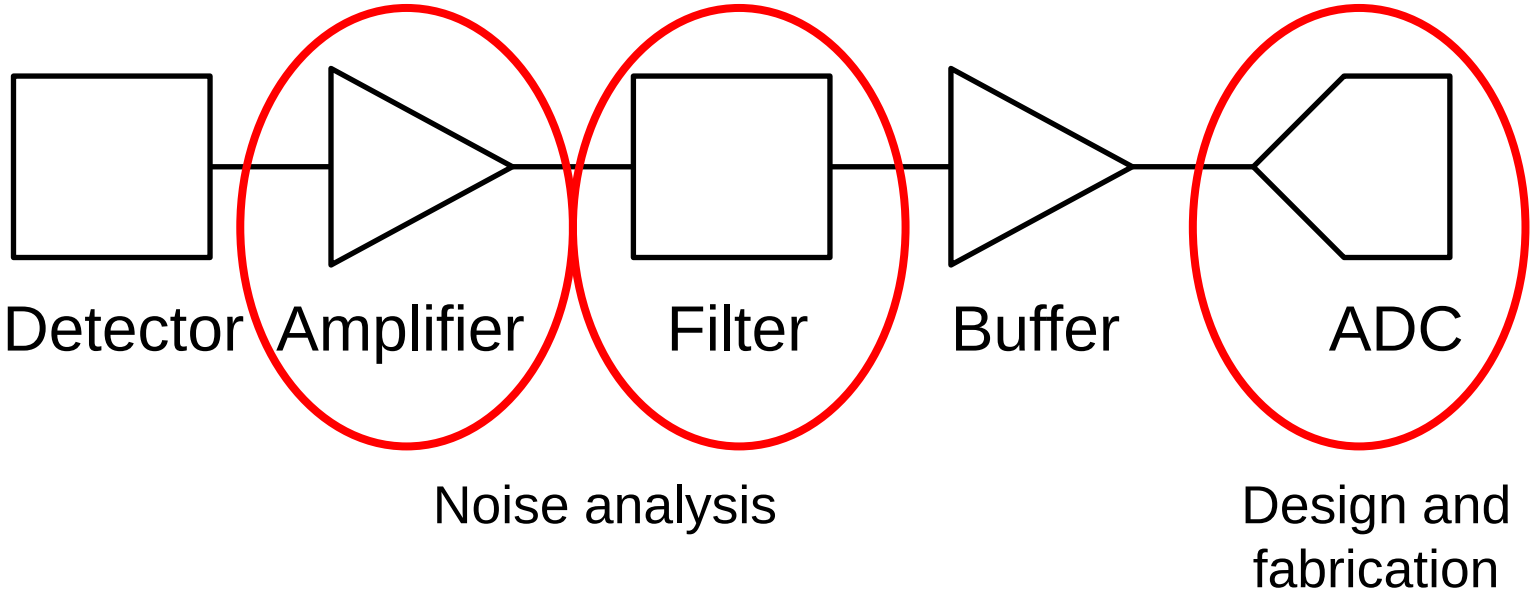
4. Current work

5. Planned work

1. Context: BeamCal instrumentation circuit

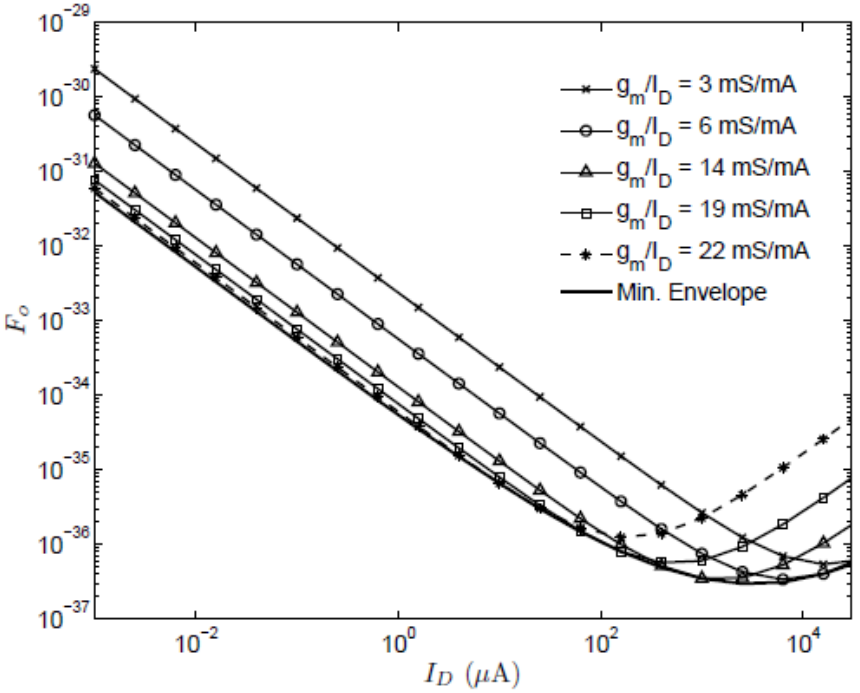


1. Context: BeamCal instrumentation circuit



2.a. Front-end noise optimization guidelines

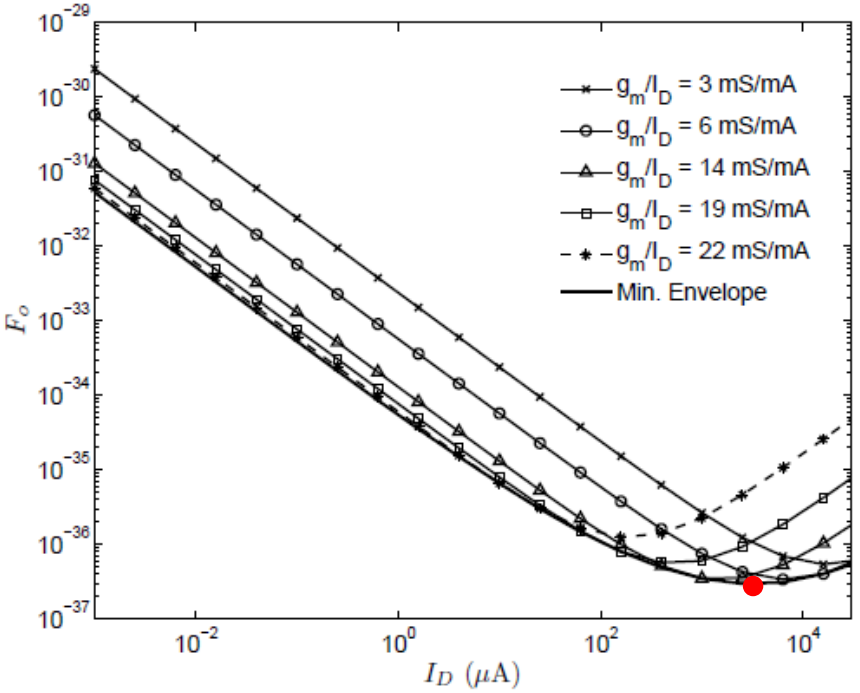
- Classic approach:
  - Minimum length input device
  - Optimal capacitive matching at the input node
  - Use the maximum power available



These conclusions, reached by analysis based on simple noise models, lead to sub-optimal results

2.a. Front-end noise optimization guidelines

- Minimum input device length is not necessarily the optimal
- *Flicker noise* is responsible for the non-monotonic noise versus current function



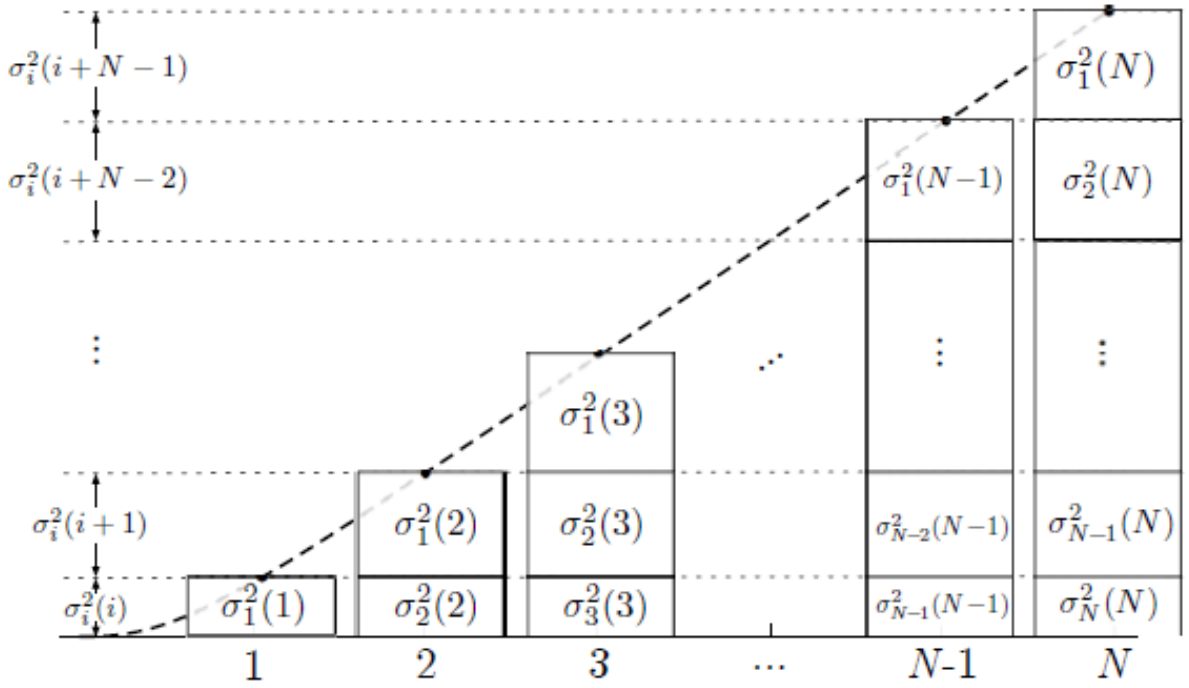
- The results were published:

E. Álvarez and A. Abusleme. *Noise power normalisation: extension of gm/ID technique for noise analysis*. IET Electronics Letters, Vol. 48, No. 8, April 2012.

E. Álvarez, D. Ávila, H. Campillo, A. Dragone and A. Abusleme. *Noise in Charge Amplifiers—A gm/ID Approach*. IEEE Transactions on Nuclear Science, vol.59, no.5, Oct. 2012

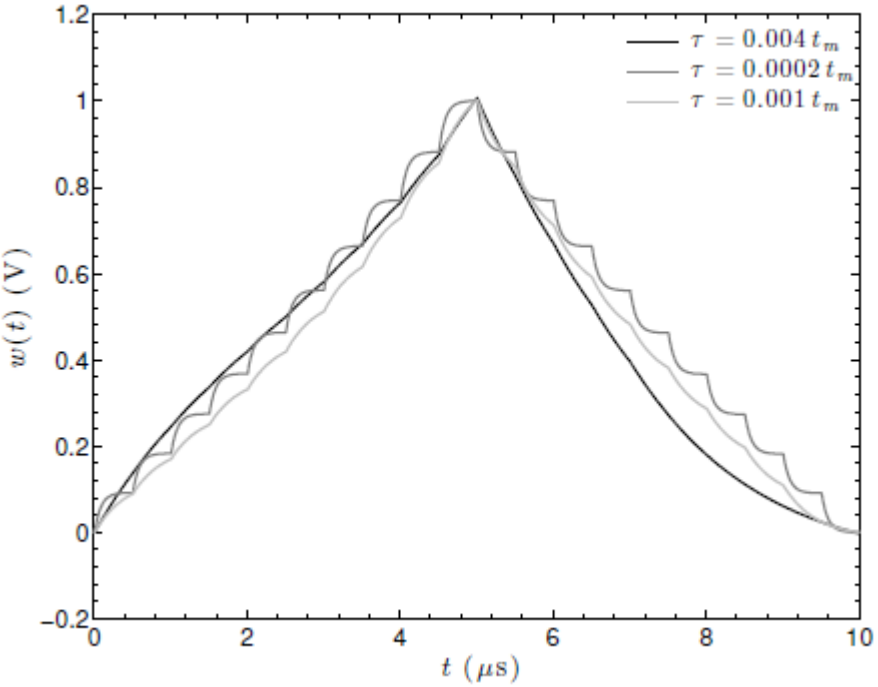
2.b. Noise analysis for discrete-time filters

- New mathematical framework:



2.b. Noise analysis for discrete-time filters

- Allows to obtain a closed-form expression for the front-end noise, suitable for computer automatic evaluation and filter optimization procedures

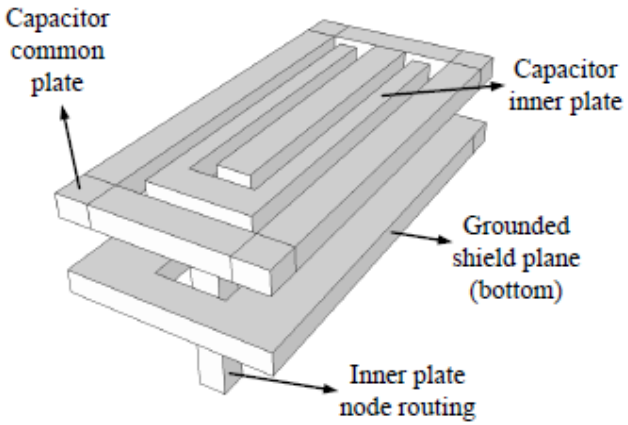


- Under review:

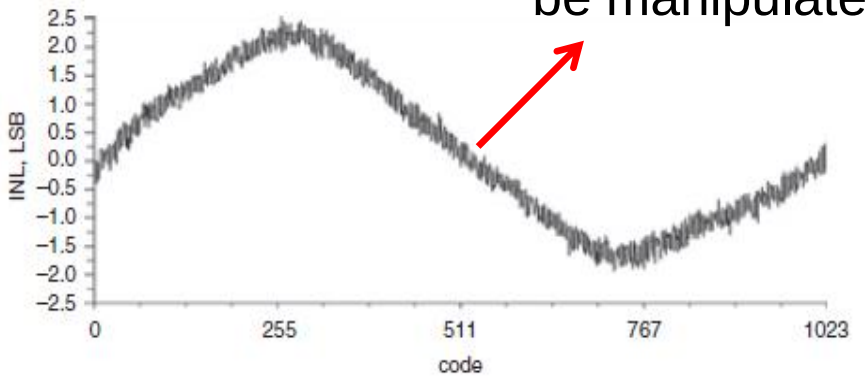
  D. Ávila, E. Álvarez and A. Abusleme. *Noise Analysis in Pulse-Processing Discrete-Time Filters*. IEEE Transactions on Nuclear Science

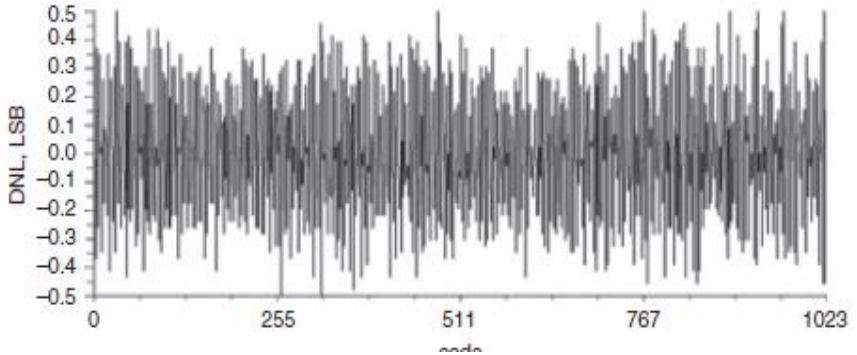
3. 10-bit SAR ADC with non-linearity compensation: previous results

- 2-fF unit capacitors
- Mismatch below 10%
- Low power consumption



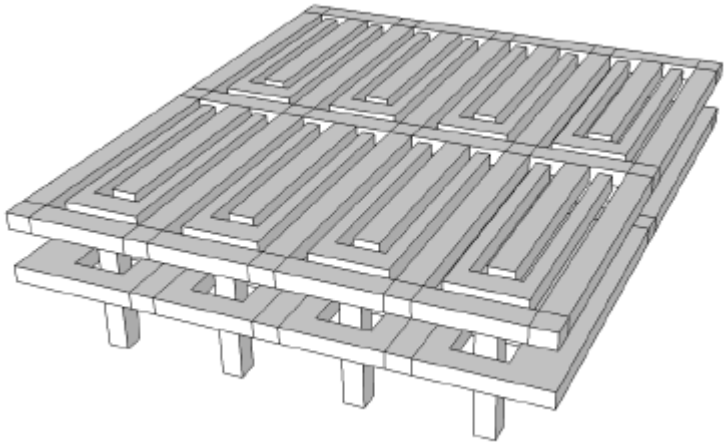
This shape can be manipulated!





3. 10-bit SAR ADC with non-linearity compensation

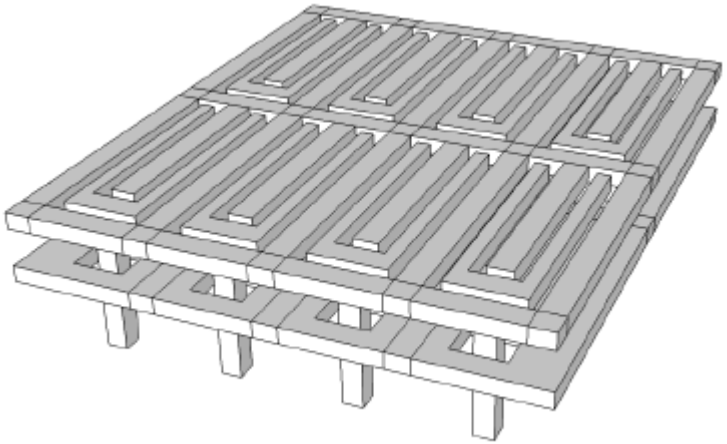
- Common-centroid fashion capacitor array
- The capacitors that are closest to the edges are larger than the capacitors at the center (due to CMP)

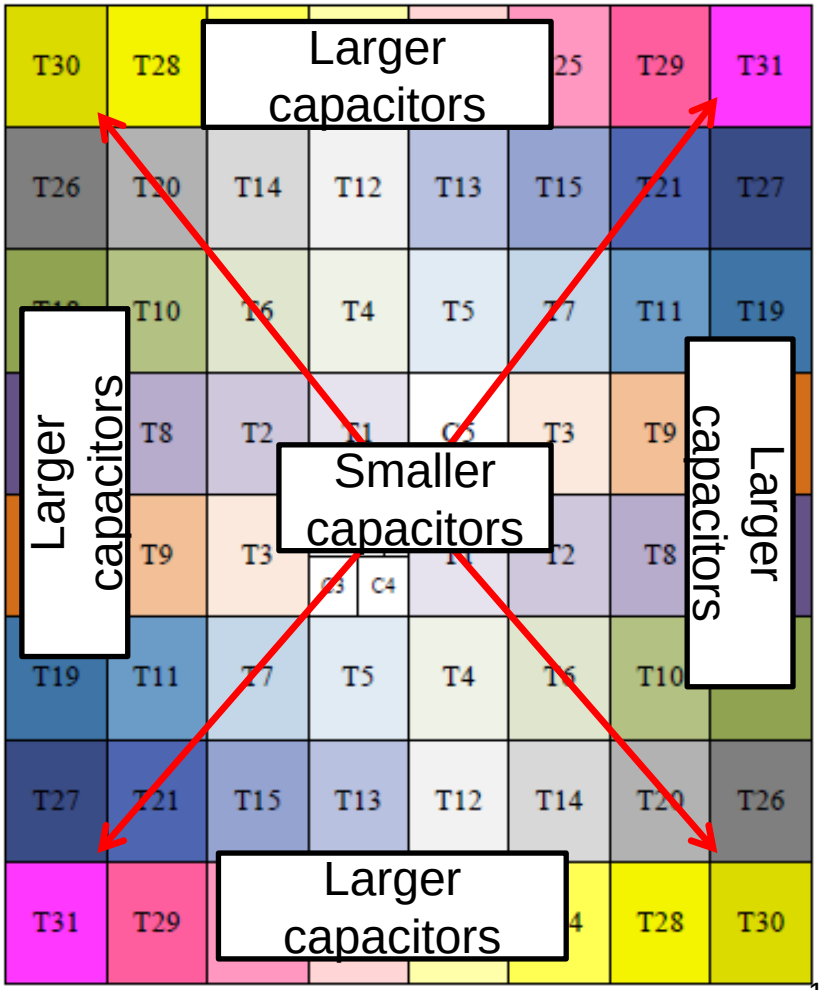


T30	T28	T24	T22	T23	T25	T29	T31
T26	T20	T14	T12	T13	T15	T21	T27
T18	T10	T6	T4	T5	T7	T11	T19
T16	T8	T2	T1	C5	T3	T9	T17
T17	T9	T3	C4 C2 Cx C1 C2 C3 C4	T1	T2	T8	T16
T19	T11	T7	T5	T4	T6	T10	T18
T27	T21	T15	T13	T12	T14	T20	T26
T31	T29	T25	T23	T22	T24	T28	T30

3. 10-bit SAR ADC with non-linearity compensation

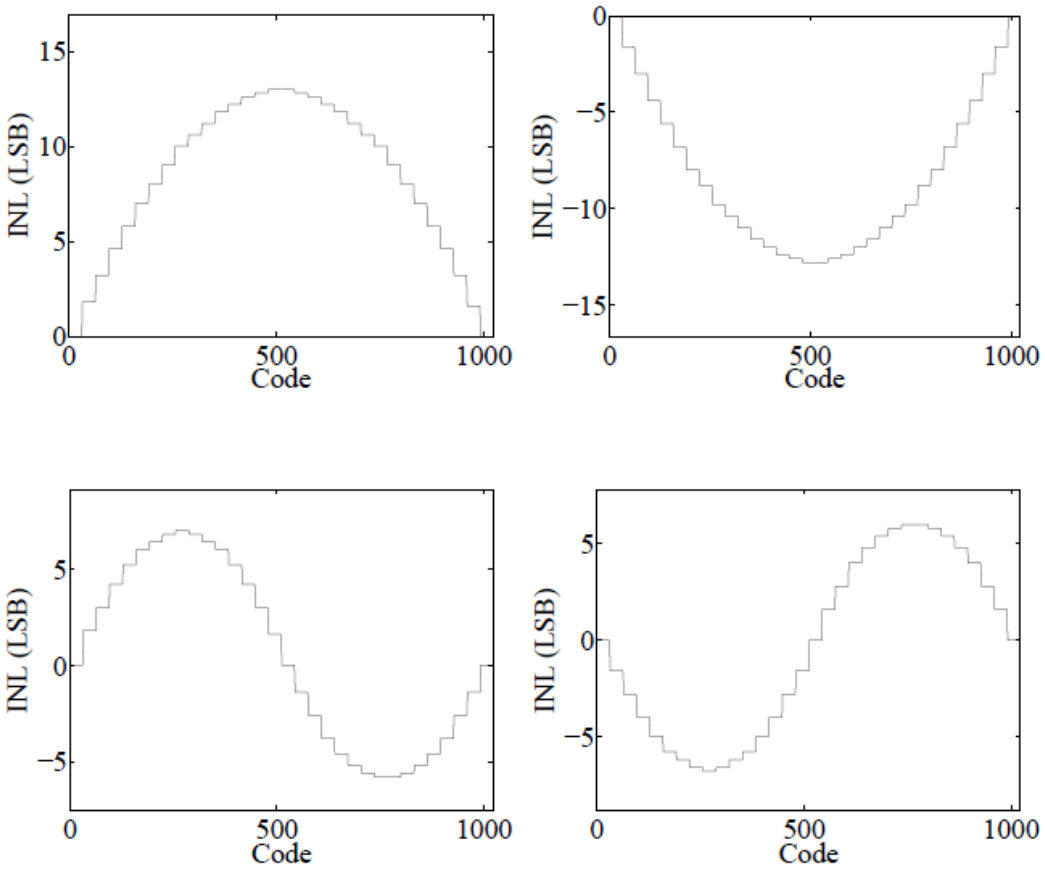
- The INL can be manipulated by changing the order in which the capacitors T1-T30 are connected





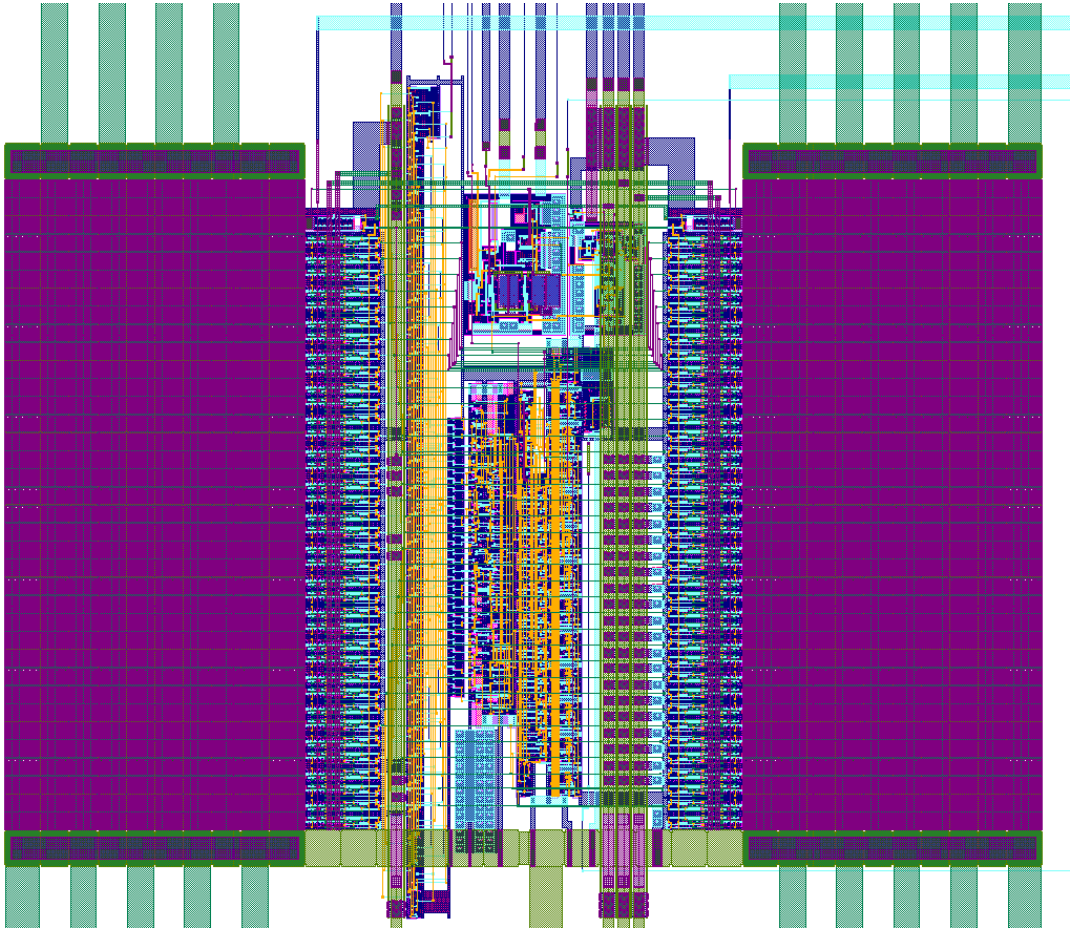
3. 10-bit SAR ADC with non-linearity compensation: simulation results

- The nonlinearity of the previous blocks in the signal path can be compensated!
- The circuit operation range can be extended!
  - Increasing the SNR



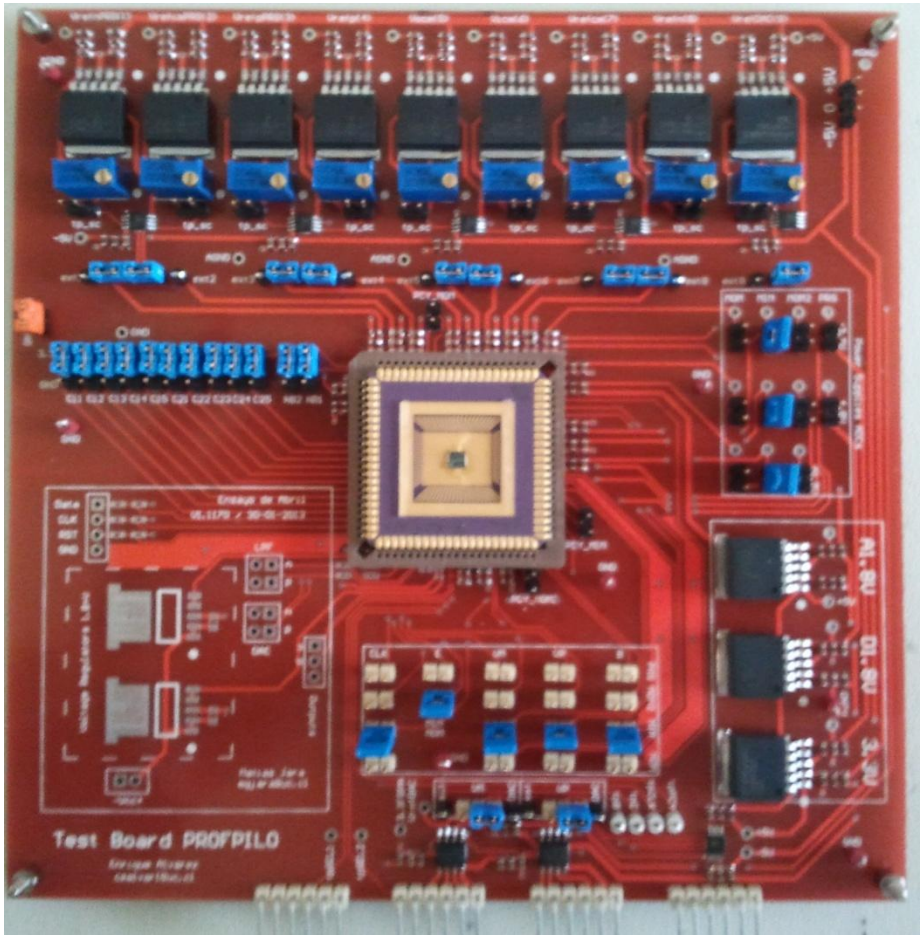
4. Current work: ADC tests

- 0.18 µm technology
- 300µm x 380µm
- Three versions of this ADC were fabricated, using different types of capacitors



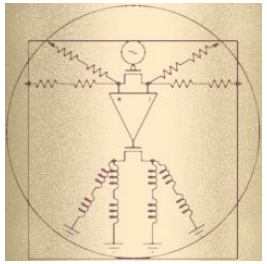
4. Current work: ADC tests

- The test board has been recently populated, and the tests start today…



5. Planned work

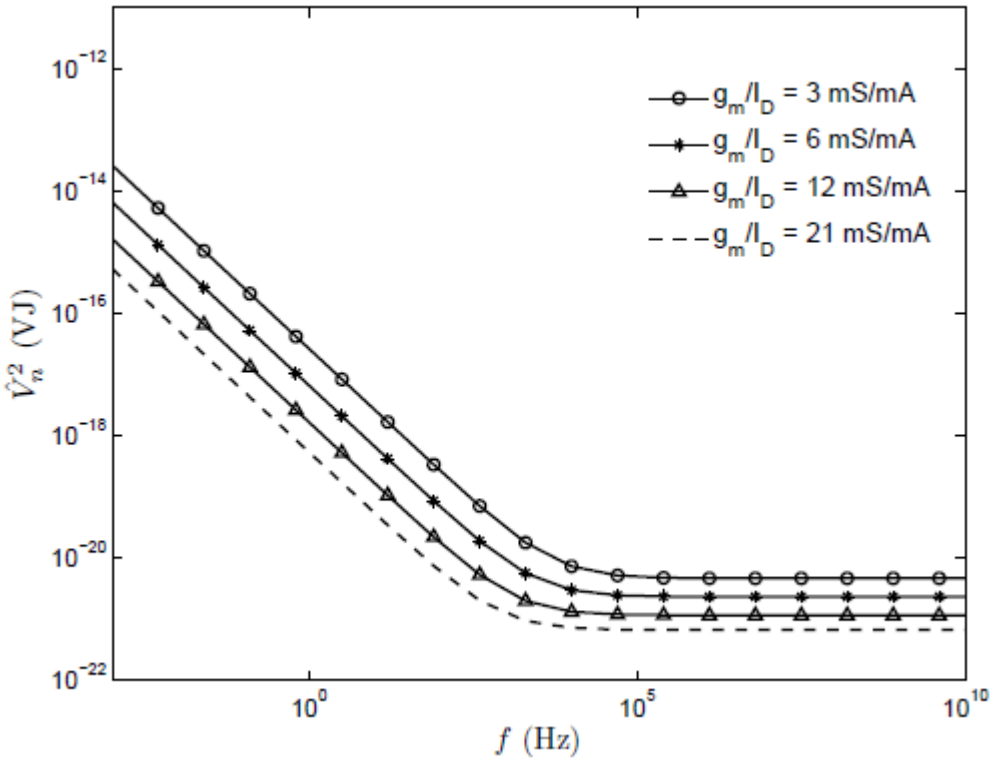
- This week: characterize the fabricated ADCs
- 2013: design and fabricate the discrete time filter, along with the charge amplifier
- 2013: put everything into a single IC with several channels
- Early 2014: the final IC first tests



Thanks for your attention,

any questions?

Extra material



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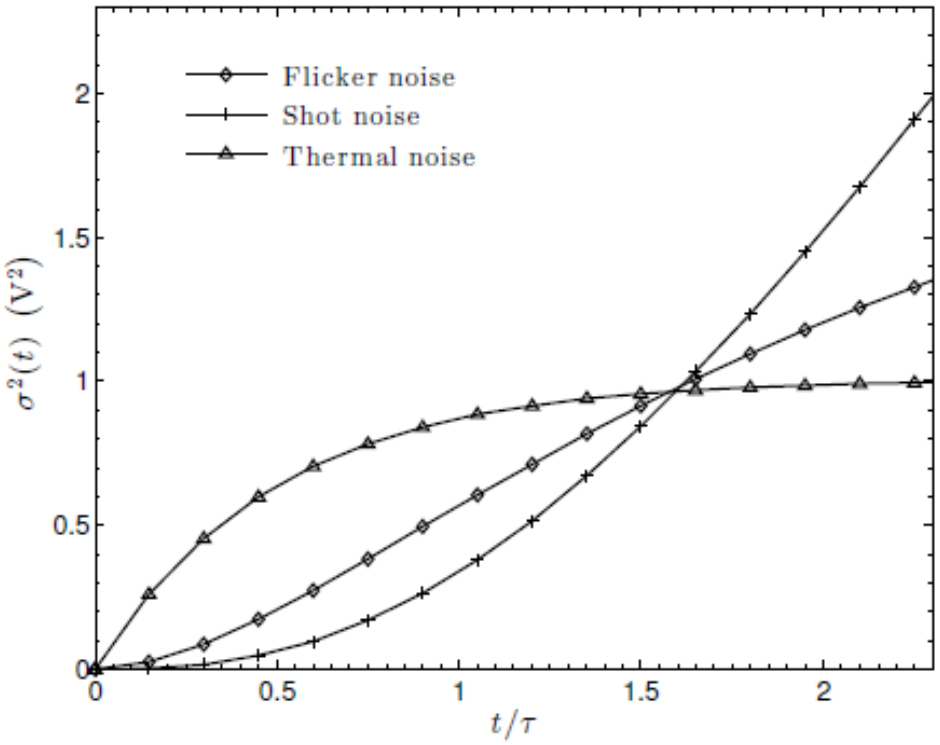

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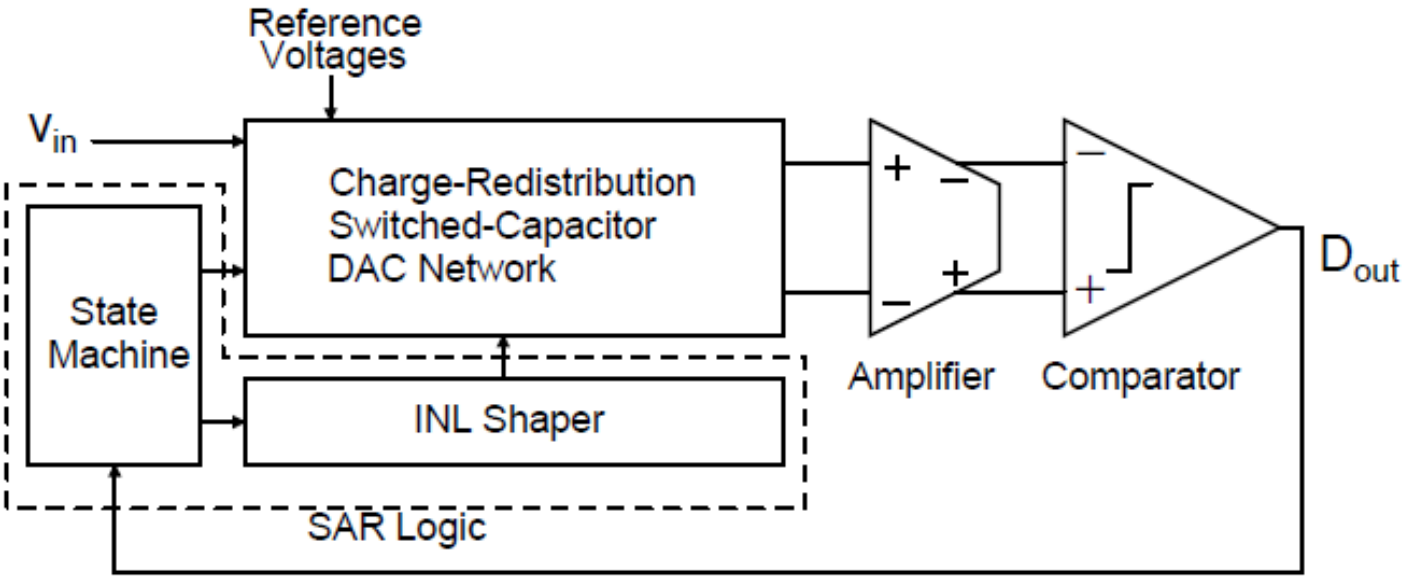

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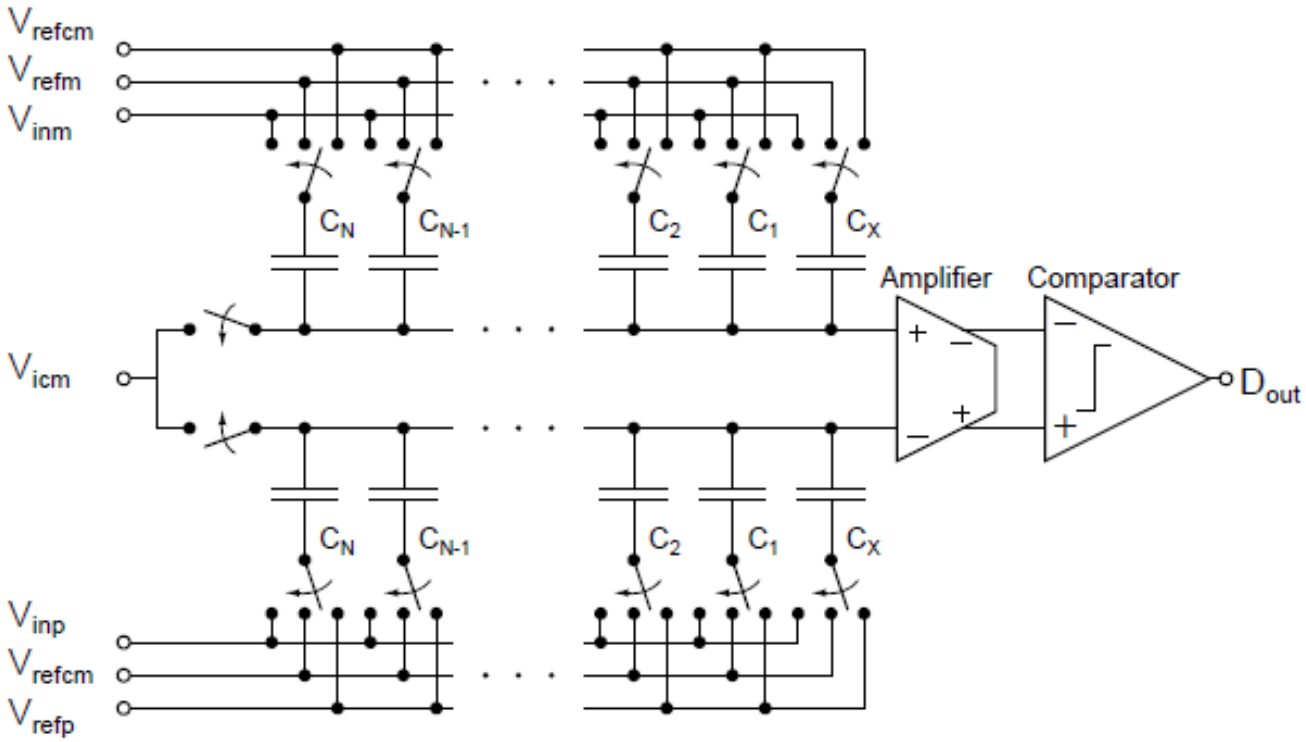

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