ASIC Technology Support and Foundry Services at CERN

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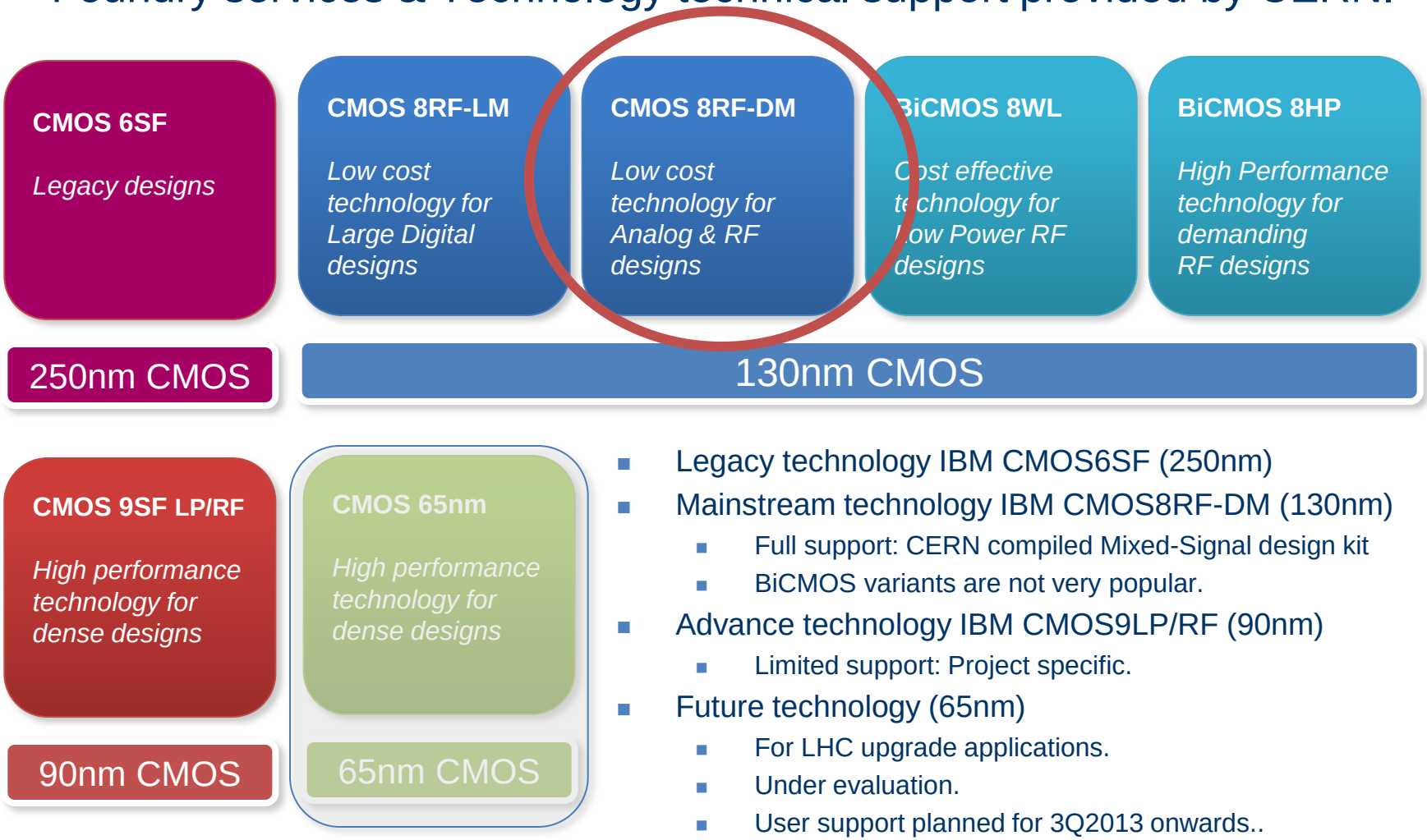
ASIC Technology Support

Overview of Technologies

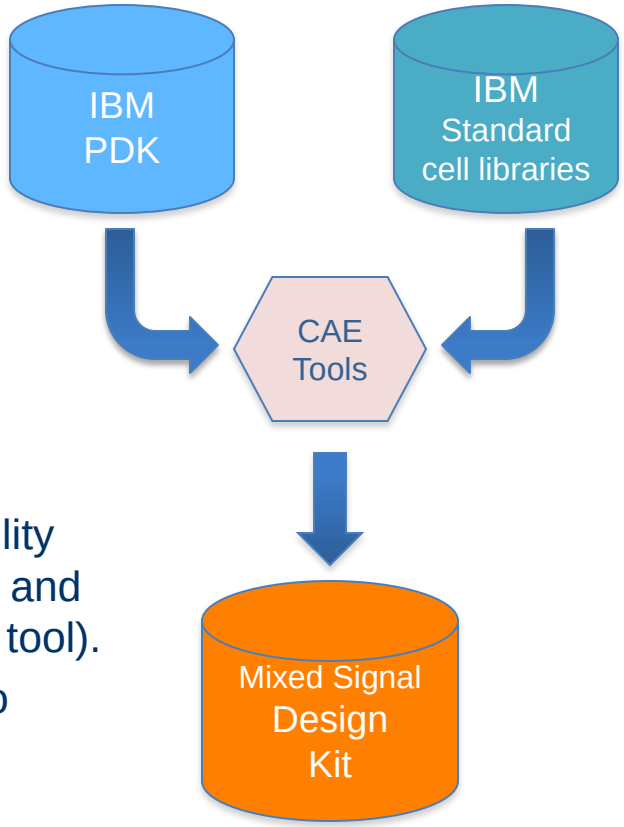
- Foundry services & Technology technical support provided by CERN.



- Legacy technology IBM CMOS6SF (250nm)
- Mainstream technology IBM CMOS8RF-DM (130nm)
  - Full support: CERN compiled Mixed-Signal design kit
  - BiCMOS variants are not very popular.
- Advance technology IBM CMOS9LP/RF (90nm)
  - Limited support: Project specific.
- Future technology (65nm)
  - For LHC upgrade applications.
  - Under evaluation.
  - User support planned for 3Q2013 onwards..

130nm Mixed Signal design kit

- Key Features:
  - **IBM PDK (Physical Design Kit)** for Analog designs merged with the
  - **IBM Digital Standard cell and IO pad libraries**
    - Physical Layout views available.
    - Access to digital standard cells libraries is legally covered by already established IBM CDAs



  - **Cadence based CAE Tool platform**
    - Open Access database that supports interoperability between analog full custom design (Virtuoso tool) and digital back-end implementation (SOC-Encounter tool).
    - Compatible with the “Europractice” distributions to facilitate the compatibility between collaborating institutes.
  - **Analog & Mixed Signal (AMS) Workflows**
    - Standardized, validated and qualified Design Workflows

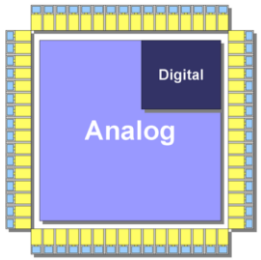
Two design kits for two metal stacks :

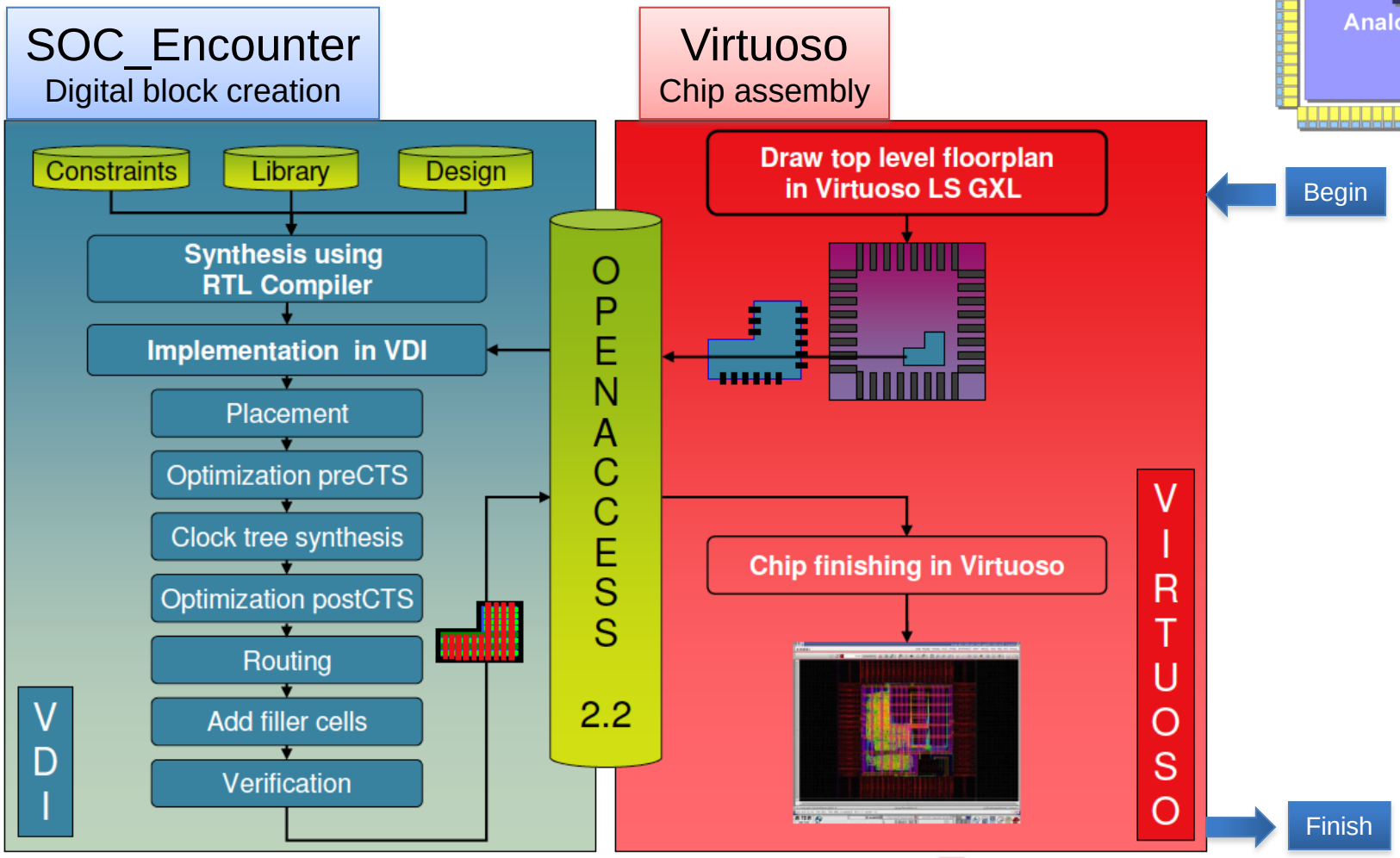
- CMOS8RF-LM (6-2 BEOL)
- CMOS8RF-DM (3-2-3 BEOL)

"Analog on Top" Design Flow

Chip Finishing in Virtuoso

For big 'A' small 'D' designs.

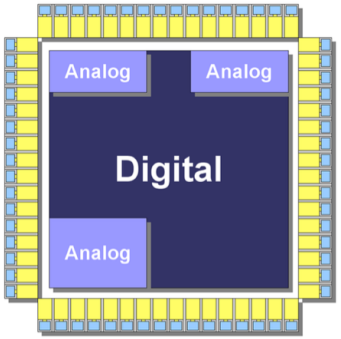




"Digital on Top" Design Flow

Chip Finishing in SOC_Encounter

For big 'D' small 'A' designs.



Virtuoso
Analog Block Creation

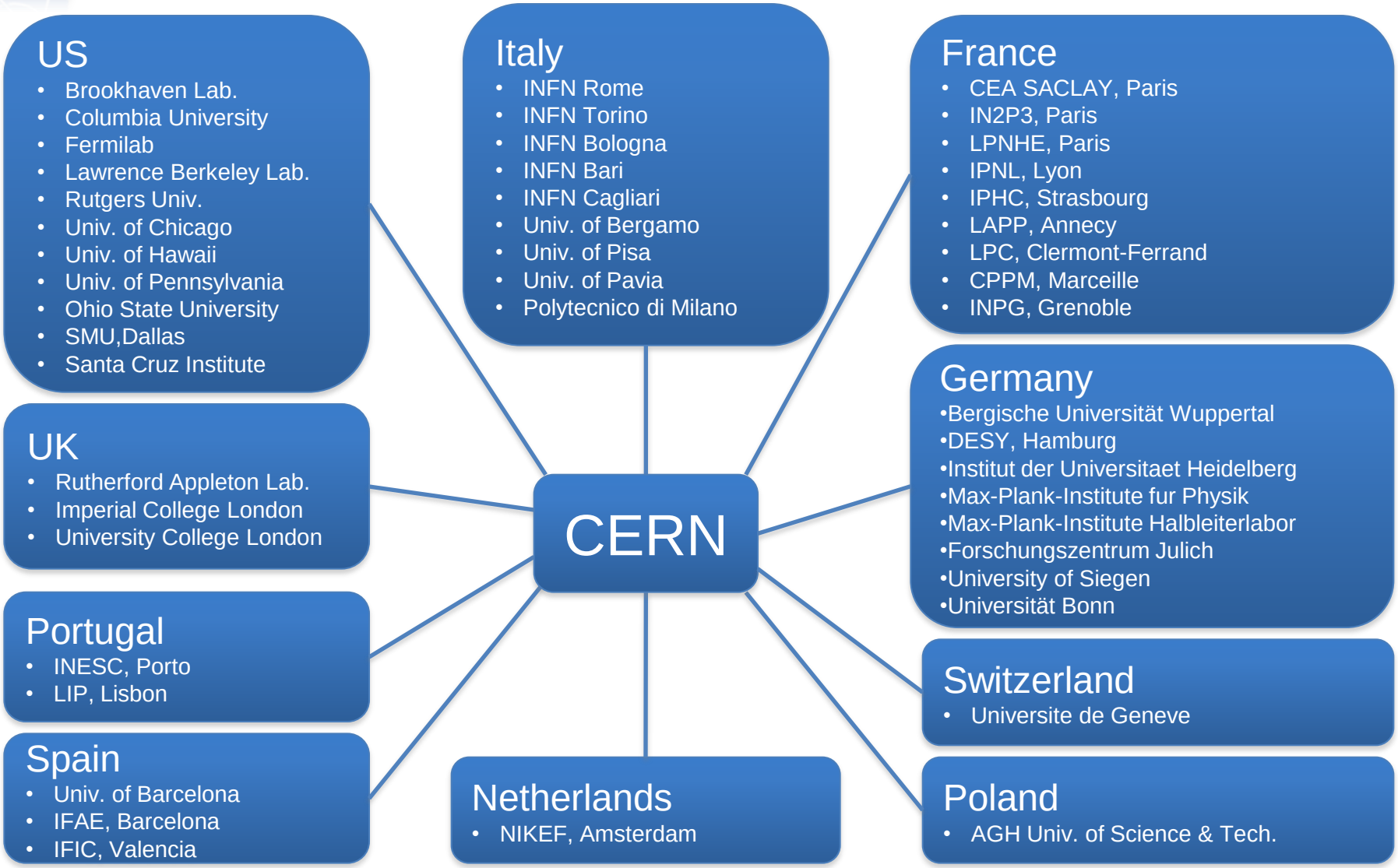
Open Access

SOC_Encounter
Chip Design

Automated task
User task

RTL synthesis
Logical Equivalence Checking
Floorplanning & power routing
Placement
Congestion analysis
Timing optimization
Clock tree synthesis
Timing optimization
Routing
Timing optimization
DFM
Signoff RC extraction
Timing analysis
Logical Equivalence Checking
DRC
LVS
Tape-out

130 nm Mixed Signal Kit Distribution



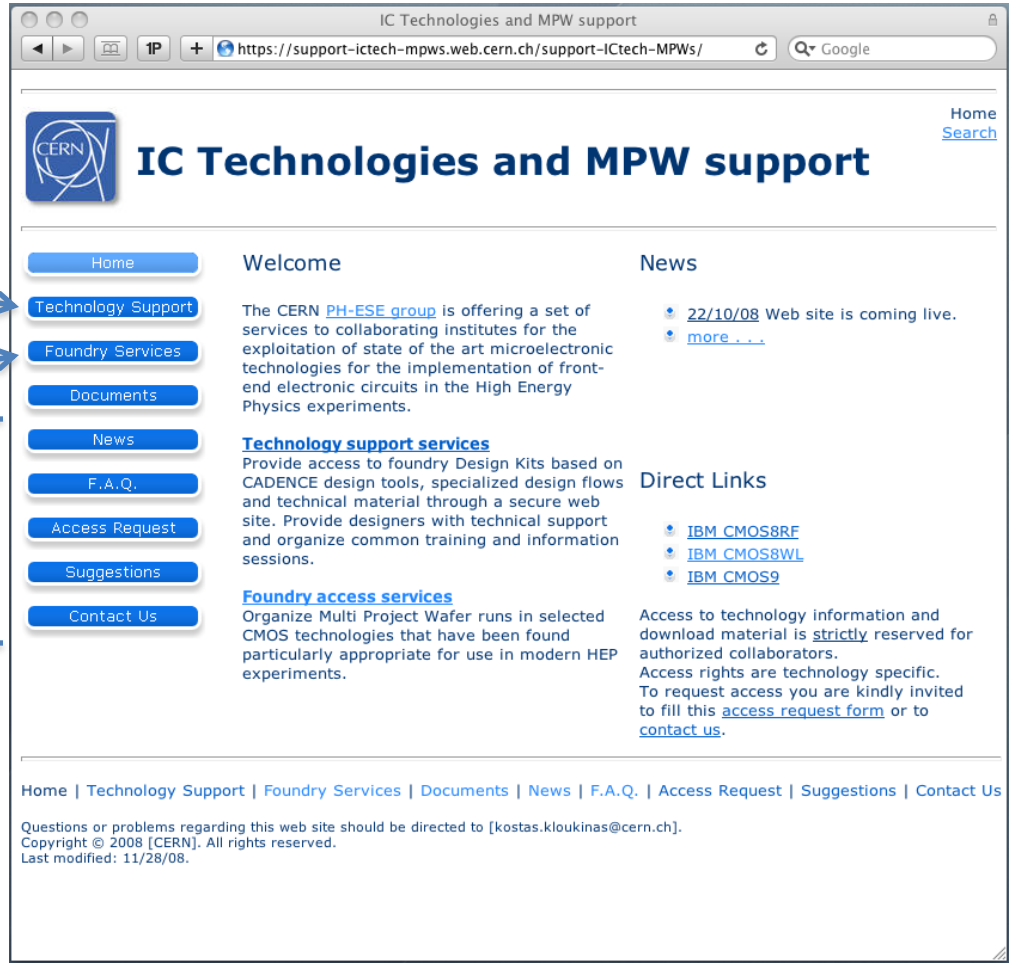
The CERN ASIC support website

http://cern.ch/asic-support

Download Design Kits and access technical documents (**restricted access**)

Information about MPW runs and foundry access services.

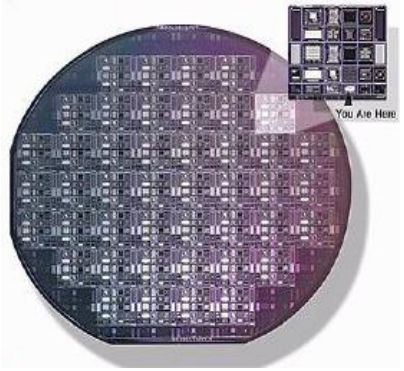
Communicate news and User support feedback forms and access request forms.



Foundry Access Services

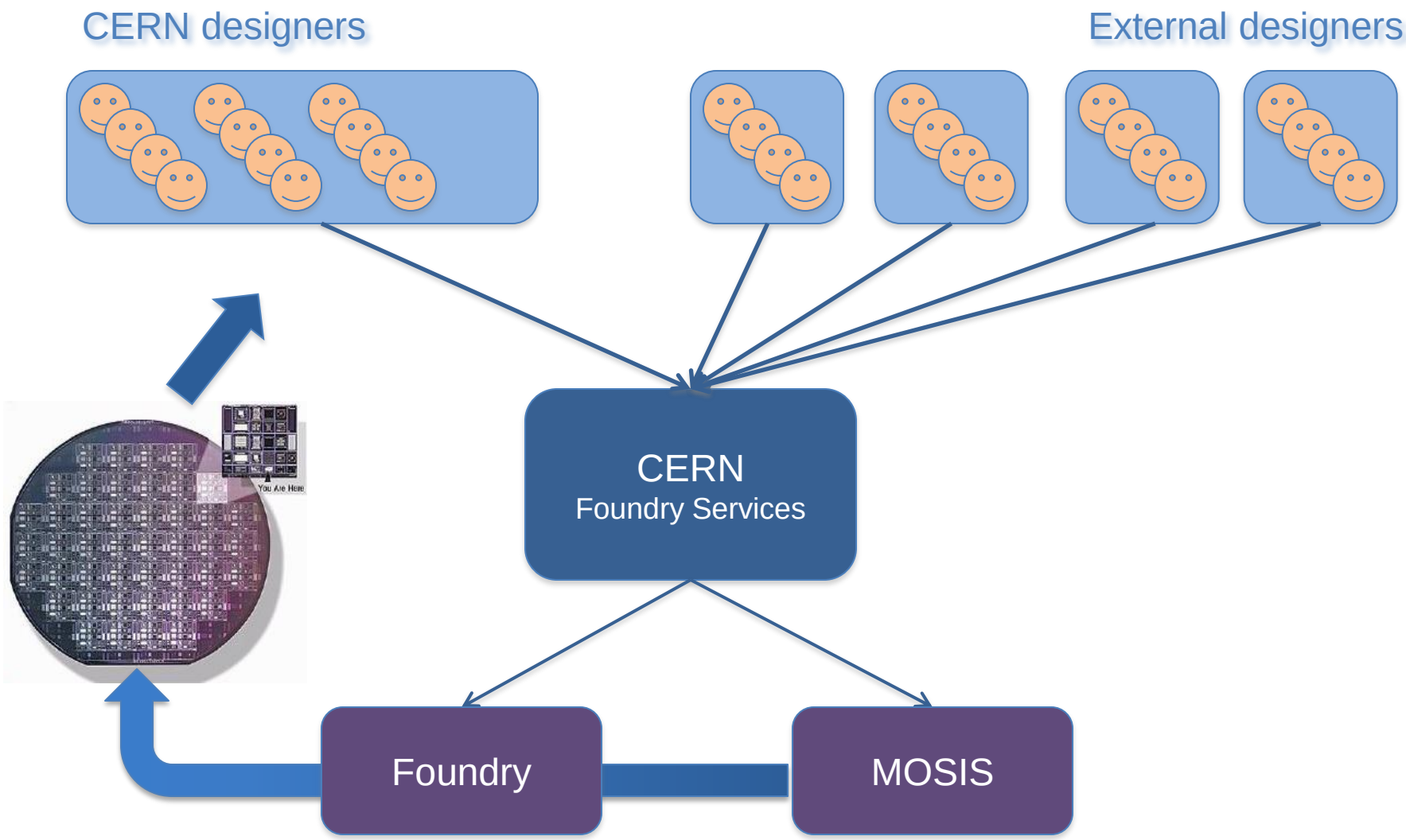
Access to Foundry Services

- Supported Technologies:
  - IBM CMOS6SF (250nm), legacy designs
  - IBM CMOS8RF (130nm), mainstream process
  - IBM CMOS8WL & 8HP (SiGe 130nm)
  - IBM CMOS9SF (90nm)



- MPW services:
  - CERN is organizing MPW runs to help in keeping low the cost of fabricating prototypes and allow for small-volume production by enabling multiple participants to share production overhead costs (NRE).
  - CERN has developed very good working relationships with the MPW service provider MOSIS as an alternate means to access silicon for prototyping.
- Engineering runs
  - CERN organizes submissions for design prototyping and volume production directly with the foundry.

Foundry Access Services

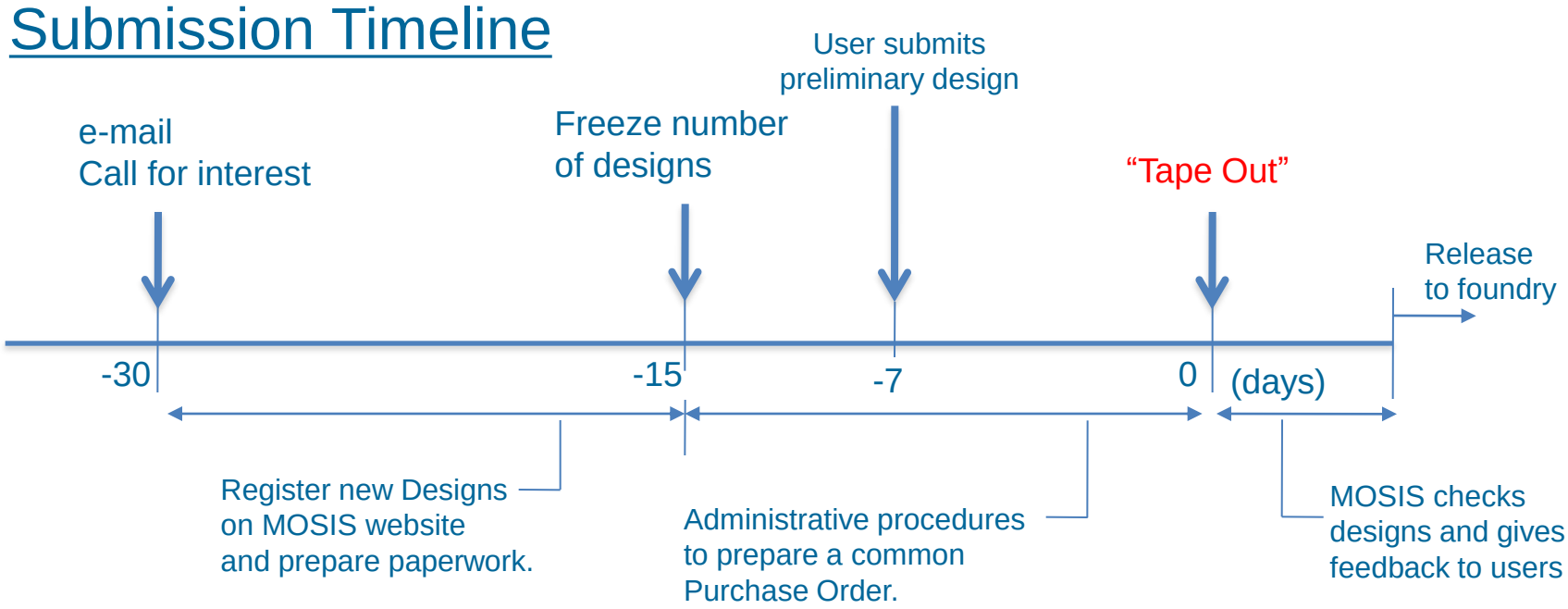


MPW runs with MOSIS

- Advantageous pricing conditions for the CMOS8RF (130nm) process
  - MOSIS recognizes the central role of CERN in research and educational activities
  - 35% cost reduction compared to standard prices
  - Waives the 10mm2 minimum order limit per design
  - CERN appreciates the excellent collaborating spirit with MOSIS
- Convenience of regularly scheduled MPW runs.
  - There are 4 runs per year scheduled every 3 months.
  - 2013 schedule: Feb. 19, May 20, Aug. 19, Nov. 18
- Typical Turn Around Time: 3 months
  - Delivery: 1 lot (40 parts) with possibility to order a few more lots at reduced cost
  - Packaging services available
- Convenience for accommodating different BEOL options:
  - DM (3 thin - 2 thick – 3 RF) metal stack
  - LM (6 thin – 2 thick) metal stack
  - C4 pad option for bump bonding

Fabricating through MOSIS

- Our alternate path for prototyping

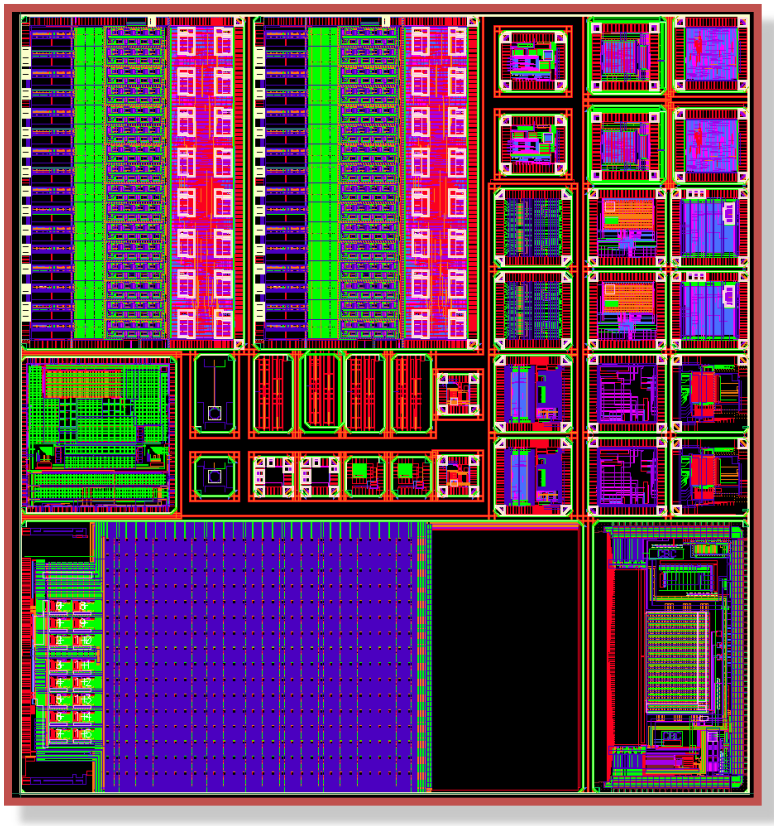


CERN organized MPW runs

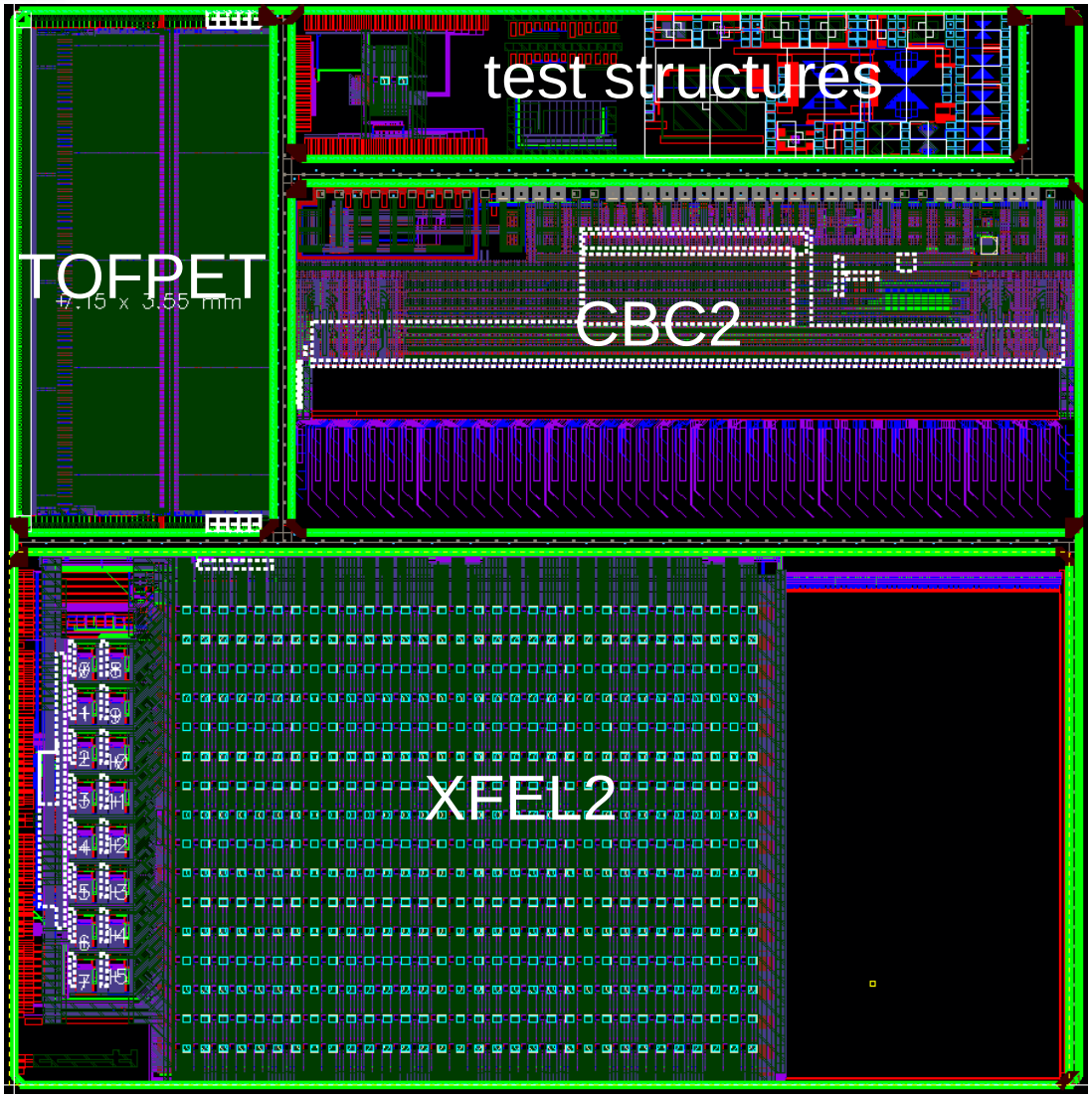
- The break-even point for the total silicon area (all designs together) between a CERN MPW and a MOSIS MPW is ~150mm^2
  - < 150mm^2 a MOSIS MPW is more cost effective
  - >150mm^2 a CERN organized MPW is more cost effective
- Targeted to large area designs and designs requiring a small volume production run at affordable cost
  - Maximum design size (max reticle size): 21mm x 19mm
- Schedule is determined by users request
  - The submission deadlines are defined with consensus among the participants
- Metal Stack supported:
  - CMOS8RF-DM (3-2-3)
  - C4 pad process split possible
- Turn Around Time:
  - Normal: 3-5 months (variable, depending on foundry load factor)
  - Rocket: 70 calendar days (fixed), cost adder

130nm CERN MPW

- CERN organized MPW
- Driven by 3 large area projects.
- 20 projects in total
- Total area: 240 mm^2
  - Small designs instantiated twice
- Cost: 2,000 USD/mm^2
- Yield: ~200 dies/project
  - More dies on request.



130nm CERN MPW in July 2012



Reticle Size:

X= 14,595, Y=14,710

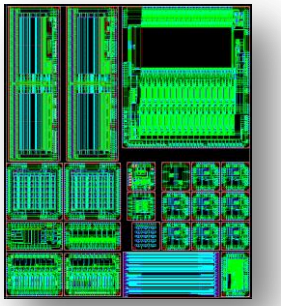
Chips per Wafer: 112

Process Split MPW run

Design	process
CBC2	C4
TOFPET	wirebond
XFEL2	wirebond
Test structures	wirebond

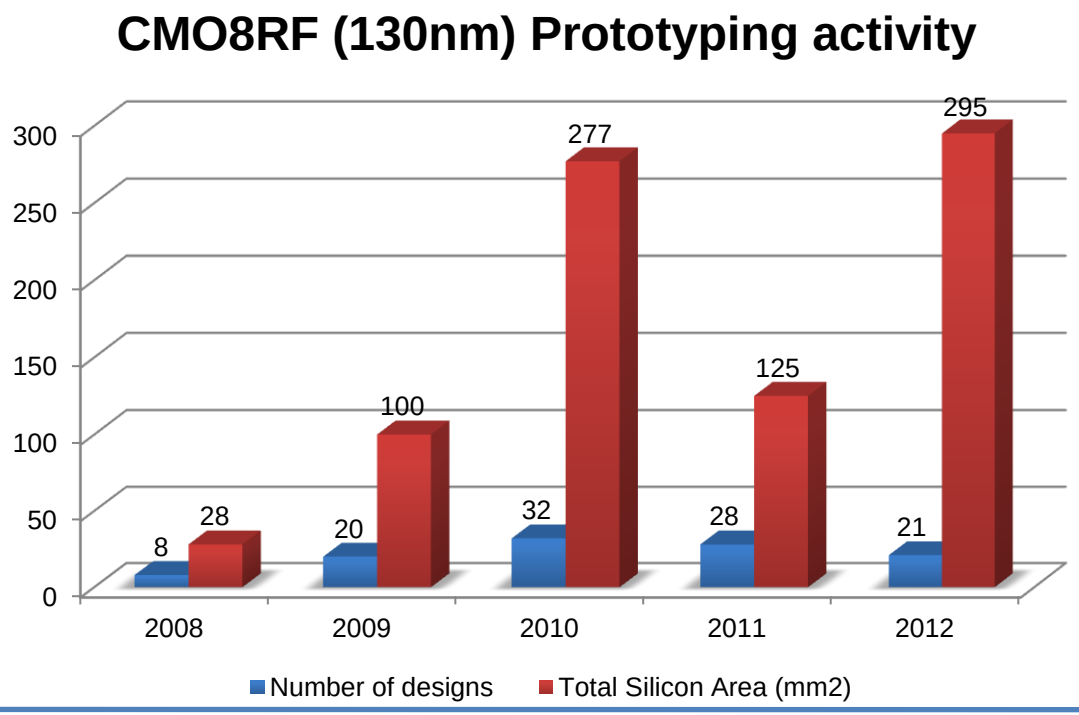
Submitted in July 2012

130nm MPW activity



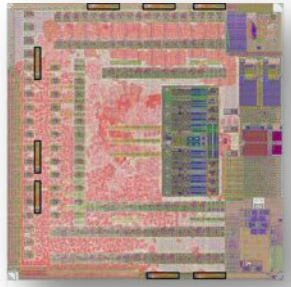
- CERN participates on all MOSIS MPW runs (4 runs/year) and organizes ad-hoc MPWs with the foundry for high volume and/or area demanding prototyping.
- CMOS8RF-DM (3-2-3) is the dominant metal stack option.
- Prototyping and Engineering run costs are kept the same for the last 2 years.

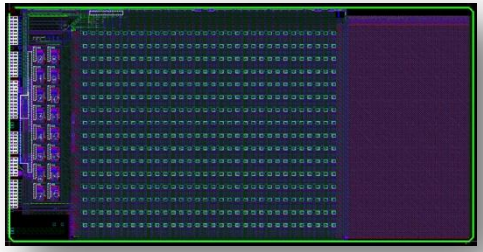
- Evolution of the Prototyping activity on CMOS8RF for the last 5 years

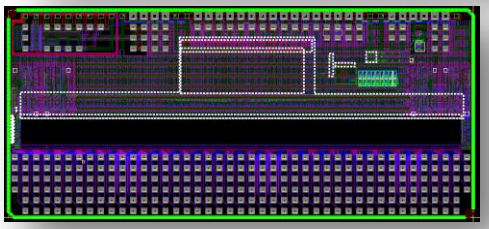


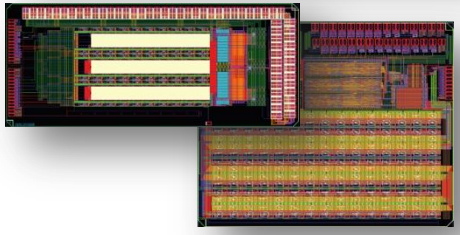
130nm Major Projects

- Gigabit Transceiver Project (GBT)
  - “GBLD” Gigabit Laser Driver chip final version in 2012.
  - “GBT-TIA” Transimpedance Amplifier chip in 2010.
  - “GBTX”, first prototype in 2009, second prototype in 2012.
- XFEL Project for the XFEL Synchrotron facility
  - First proto with all elements in the pixel, bump test chip in 2010 MPW.
  - Second prototype submitted in 2012 MPW.
- DSSC Project for the XFEL Synchrotron facility
  - Prototype submissions of circuit blocks in 2010, 2011, 2012.
- CBC: CMS Tracker Front-End ASIC
  - First prototype submitted in 2010 MPW.
  - Second prototype submitted in 2012 MPW.
- S-Altro: ALICE TPC Readout ASIC
  - Submitted in 2010 on an MPW (24 wafers).
- NA62 Pixel Gigatracker detector
  - Readout test chip with ON pixel TDC cell
  - Readout test chip with End-Of-Column TDC cell



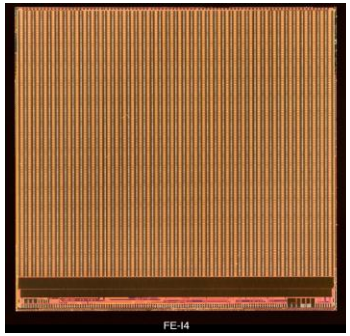




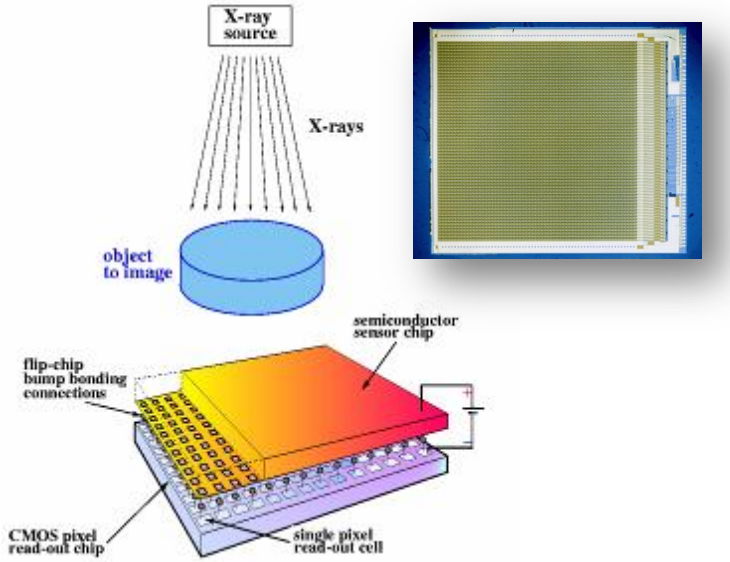


130nm Major Projects

- FE-I4_B: ATLAS PIXEL ‘b-layer upgrade’
  - Full scale prototype chip, 19x20mm2 (2010Q2 engineering run)
  - Final production (96 wafers) in 2012.



- MEDIPIX project
  - MEDIPIX3_V1: 12 wafers in 2009
  - MEDIPIX3_V2: 12 wafers in 2010
  - MEDIPIX_RX: 48 wafers in 2012



Medipix: Medical X-ray diagnosis with contrast enhancement and dose reduction


Thank You