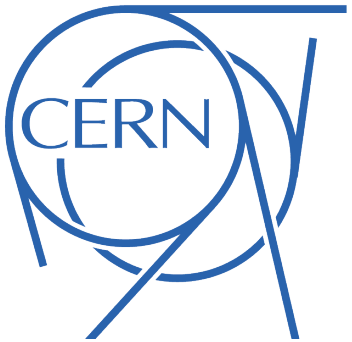


IP blocks for implementing the GBT interface

Filip Tavernier

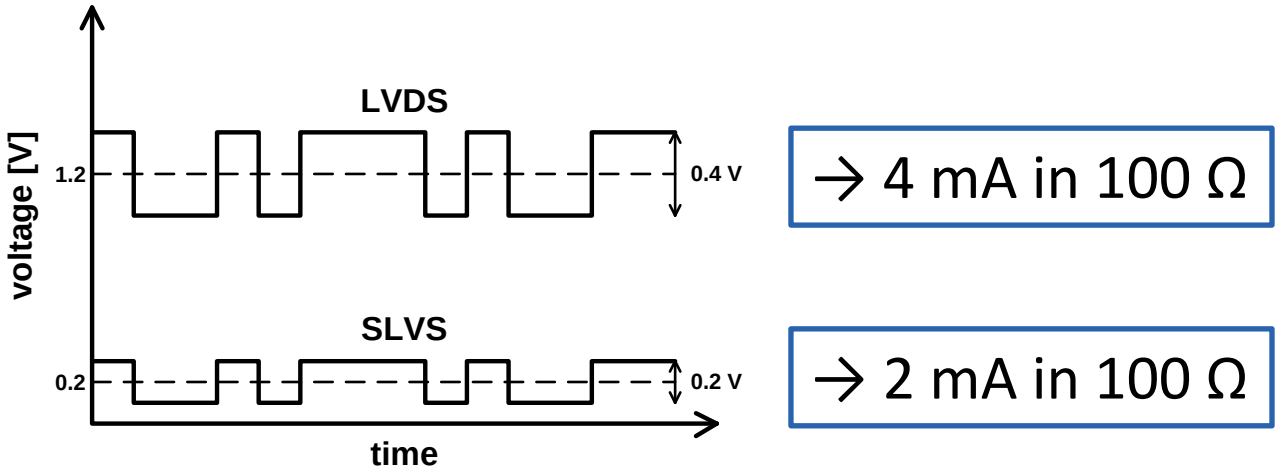
CERN

Outline

- SLVS driver and SLVS/LVDS receiver
- *ePLL-FM*
- *ePLL-CDR*

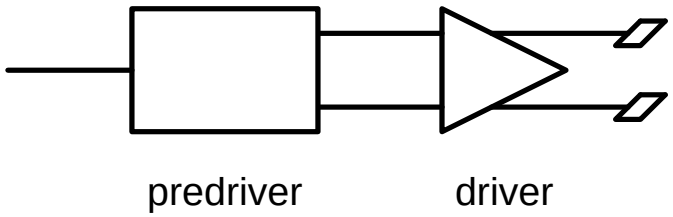
General specifications

- **TX:** transmit SLVS signals up to 320 Mbit/s or clocks up to 320 MHz
- **RX:** receive SLVS and LVDS signals up to 320 Mbit/s or clocks up to 320 MHz
- **Rx:** integrated programmable (ON/OFF) termination resistor
- **Tx/Rx:** working at a supply voltage between 1.2 V and 1.5 V (1.5 V is required if LVDS signals need to be received)
- **Tx/Rx:** can be disabled (Tx has then a high-impedance output)



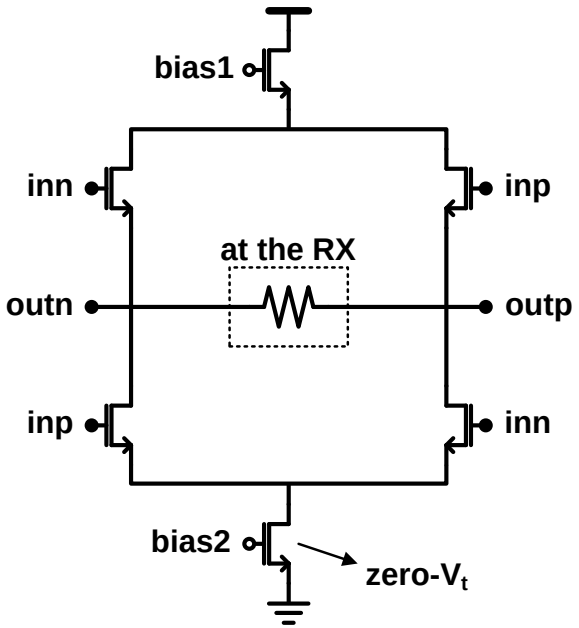
Architecture of the SLVS Tx

- signals:
  - input: digital single-ended voltage
  - output: analog differential current
- building blocks:
  - predriver: converts the input signal into a differential digital voltage
  - driver: converts the differential voltage into a differential current (programmable with cset<3:0>)

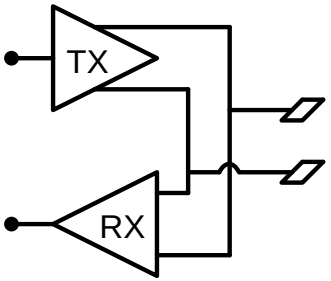


The TX driver

- off = **LOW**
  - inp = **HIGH** & inn = **LOW**
    → current flows 'from right to left' in the termination resistor
  - inp = **LOW** & inn = **HIGH**
    → current flows 'from left to right' in the termination resistor
  - The current in the driver stage is set by the 'cset' bits in the biasing circuit (not shown here)
- off = **HIGH**
  - bias1 = bias2 = 0 V (set by the biasing circuit)
  - Although the zero-Vt current source is never completely off, both inp and inn are **LOW** (see previous slide) so that the outputs are high impedant → can be used on a bus



Simulation of the SLVS Tx

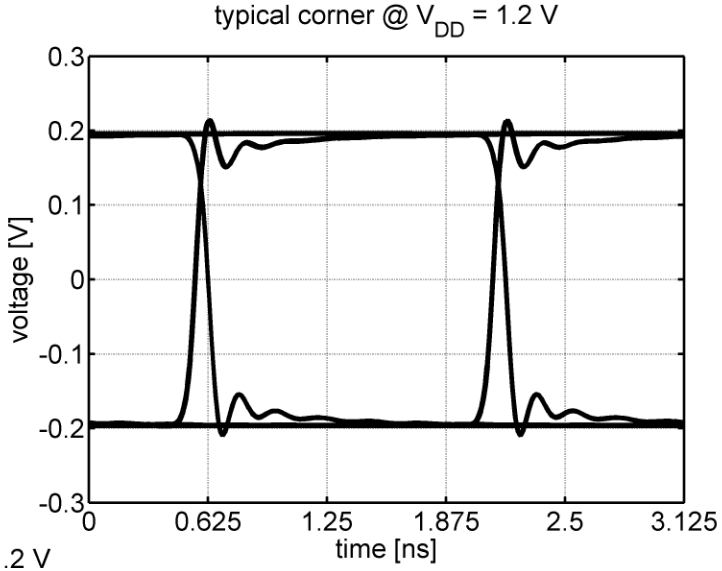


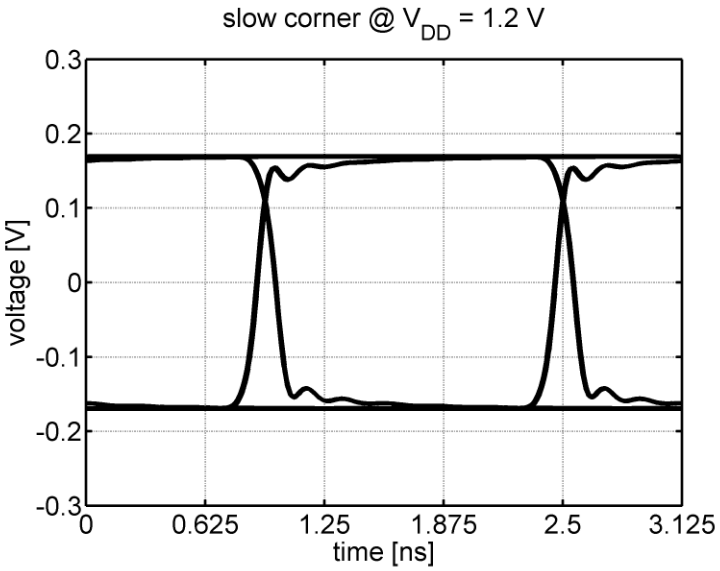
- simulation of the Tx in the bi-directional cell
- simulation of RC-extracted netlists
- simulation in 3 corners:
  - **typical:** V_{DD} = 1.2 V (1.5 V) / T = 27° C / TT models
  - **slow:** V_{DD} = 1.1 V (1.4 V) / T = 100° C / SS models
  - **fast:** V_{DD} = 1.35 V (1.65 V) / T = -30° C / FF models
- simulation with the 'nominal' current setting (2 mA)
- input signal: 2^7-1 PRBS @ 640 Mbit/s
- off-chip termination resistor of 100 Ω
- package modeled by 1 nH bondwire inductors and 1 pF off-chip parasitic capacitance

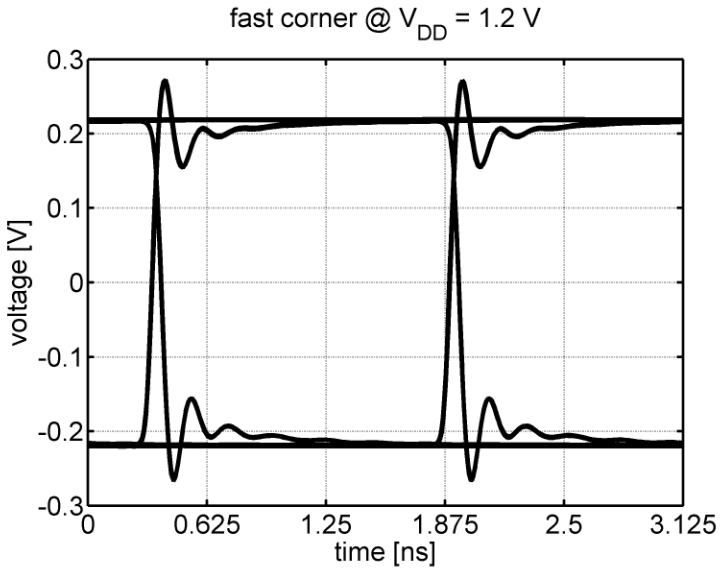
Simulation of the SLVS Tx @ V_{DD} = 1.2 V

current [mA] / power [mW]:

- typical: 3.31 / 3.97
- slow: 2.73 / 3.00
- fast: 4.13 / 5.58



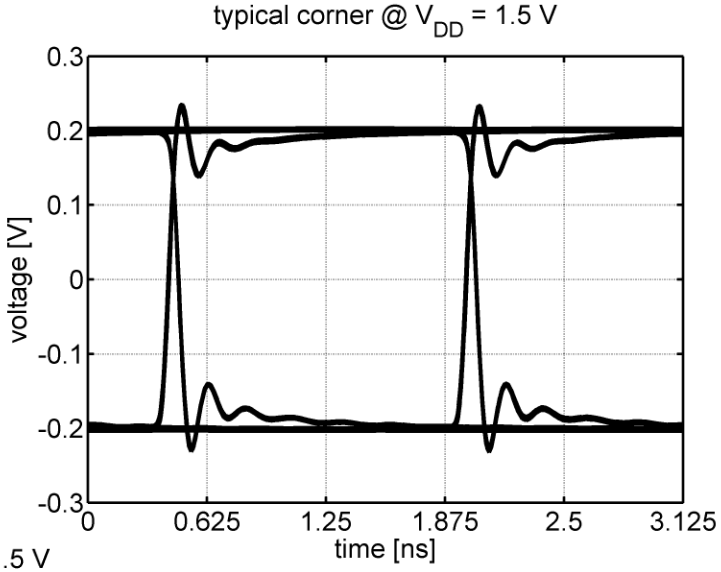


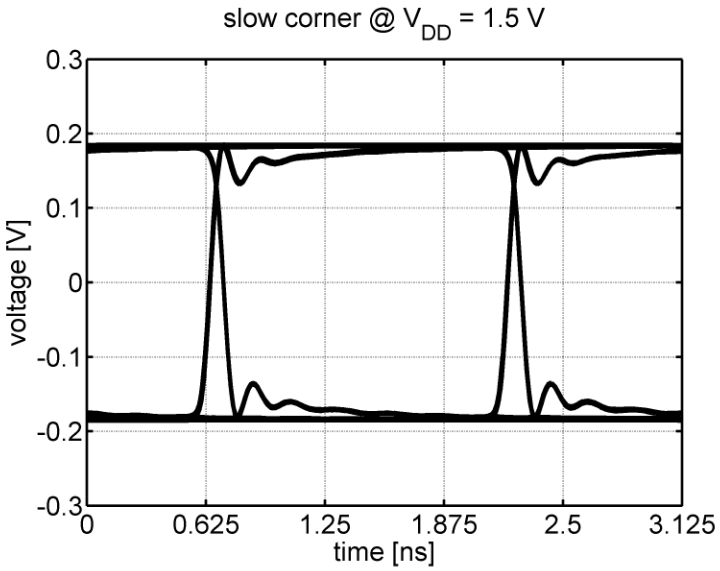


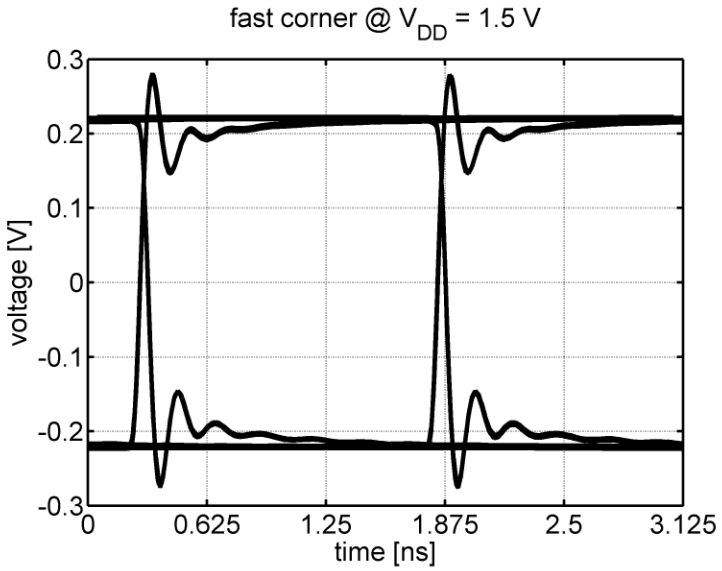
Simulation of the SLVS Tx @ V_{DD} = 1.5 V

current [mA] / power [mW]:

- typical: 4.01 / 6.02
- slow: 3.41 / 4.77
- fast: 4.93 / 8.13

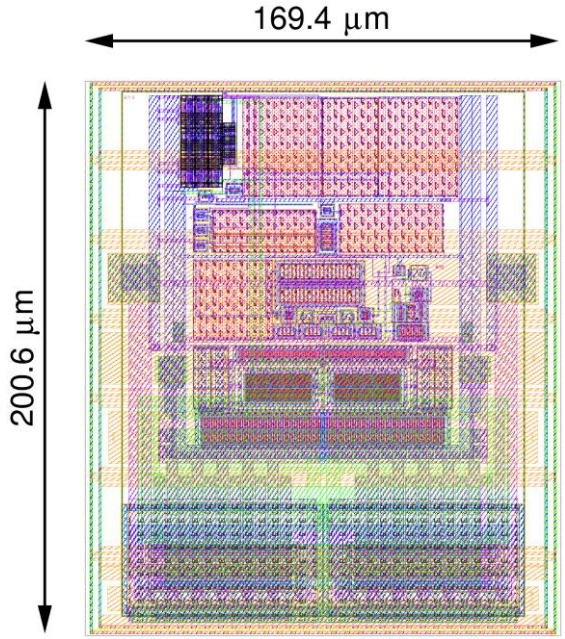






SLVS Tx versions

	C4	wirebond
technology	IBM 130 nm LM	IBM 130 nm DM
metals used	M1-M4	M1-MA
size	169.4 µm x 200.6 µm	146.28 µm x 215.28 µm
pitch	168.4 µm vertical 199.6 µm horizontal	146 µm vertical 215 µm horizontal



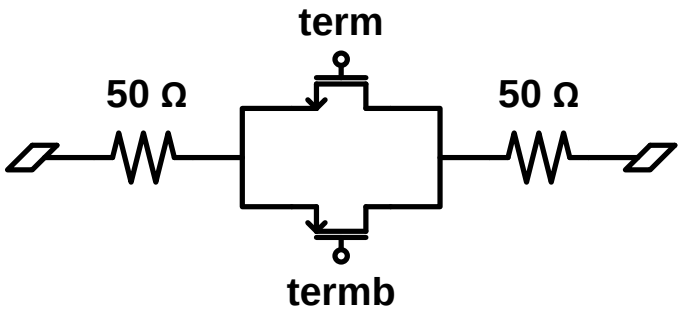
Programmable Rx termination resistor

Rx needs to terminate SLVS (V_{CM} = 0.2 V) and LVDS (V_{CM} = 1.2 V) signal levels with a 100 Ω resistance

→ nMOS switch is needed to enable a low switch resistance while receiving SLVS signals

→ pMOS switch is needed to enable a low switch resistance while receiving LVDS signals

→ large switches are needed to minimize the dependency of the termination resistance on supply voltage variations (design point: switch resistance < 10 Ω in all cases)

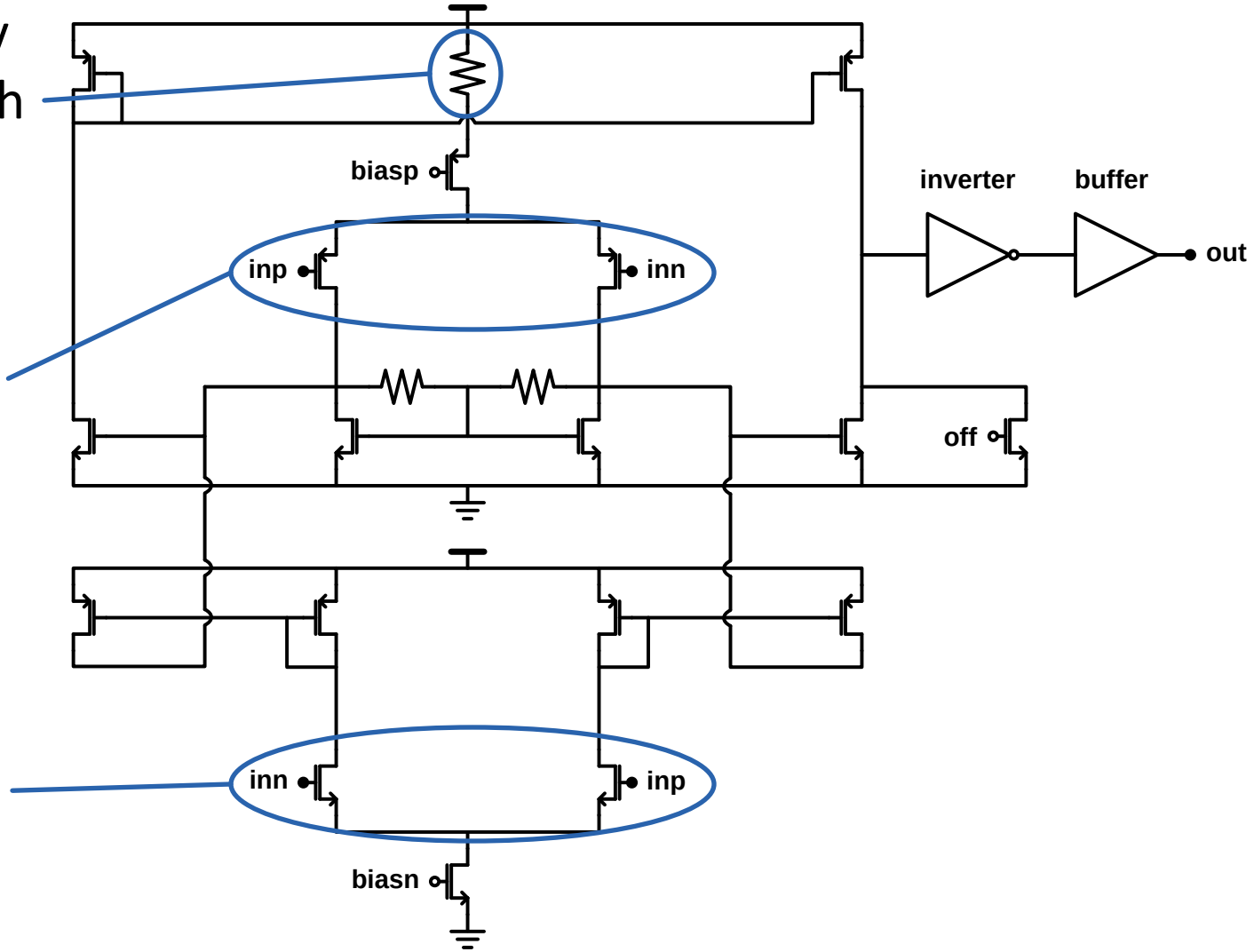


Amplifier of the SLVS/LVDS Rx

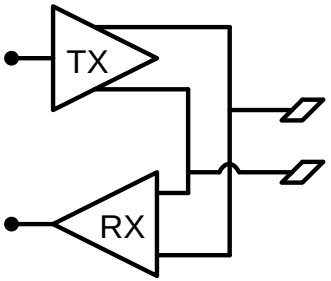
reduce sensitivity of the current with variations of V_{DD}

input pair for SLVS (off for LVDS)

input pair for LVDS (off for SLVS)



Simulation of the new SLVS/LVDS Rx



- simulation of the Rx in the bi-directional cell
- simulation of RC-extracted netlists
- simulation in 3 corners:

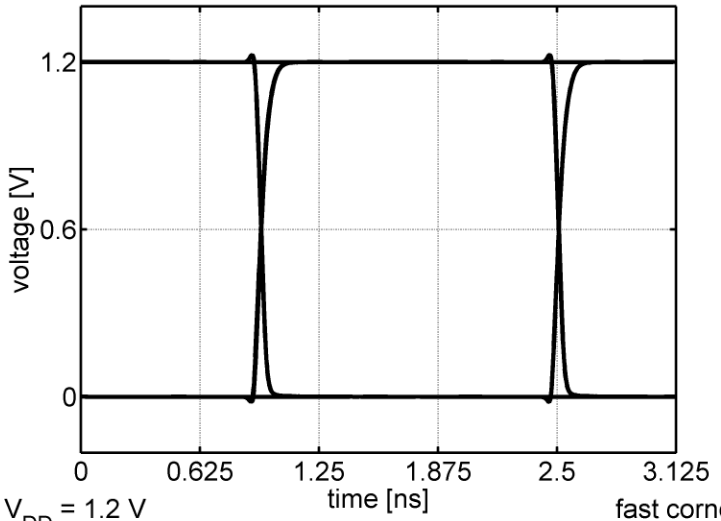
  typical: V_{DD} = 1.2 V (1.5 V) / T = 27° C / TT models
  slow: V_{DD} = 1.1 V (1.4 V) / T = 100° C / SS models
  fast: V_{DD} = 1.35 V (1.65 V) / T = -30° C / FF models
- simulation with the on-chip termination network activated
- input signal: 2^7-1 PRBS @ 640 Mbit/s
- package modeled by 1 nH bondwire inductors and 1 pF off-chip parasitic capacitance

Simulation of the Rx @ V_{DD} = 1.2 V with SLVS input signals

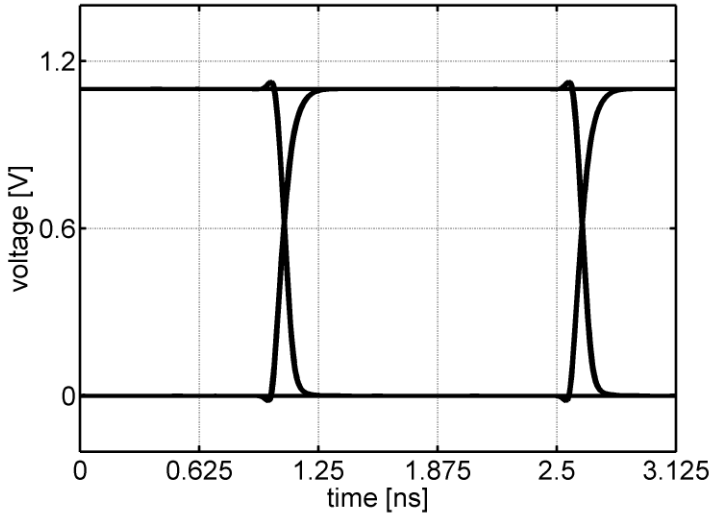
current [µA] / power [µW]:

- typical: 320 / 384
- slow: 310 / 341
- fast: 298 / 402

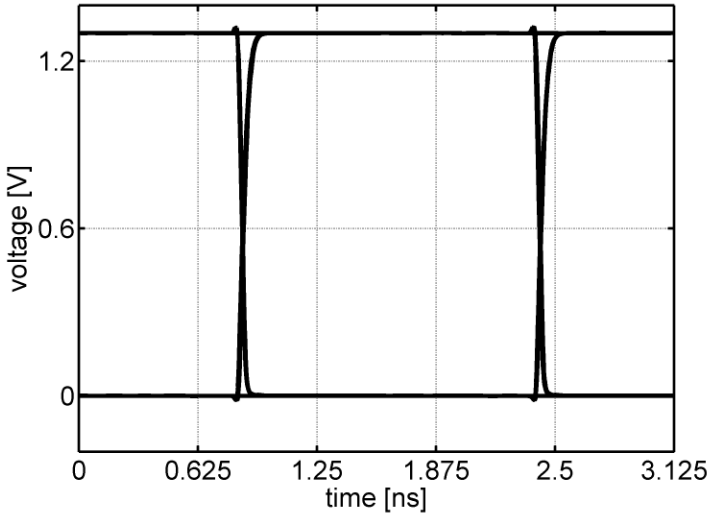
typical corner for SLVS signals @ V_{DD} = 1.2 V



slow corner for SLVS signals @ V_{DD} = 1.2 V



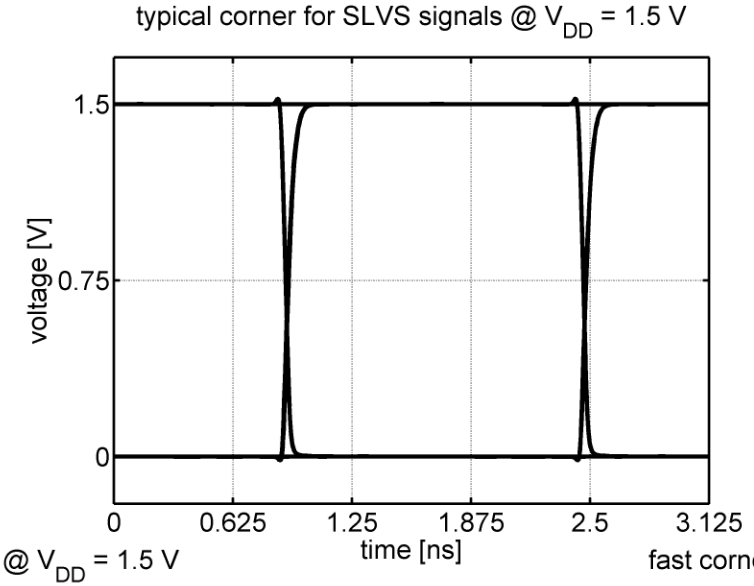
fast corner for SLVS signals @ V_{DD} = 1.2 V

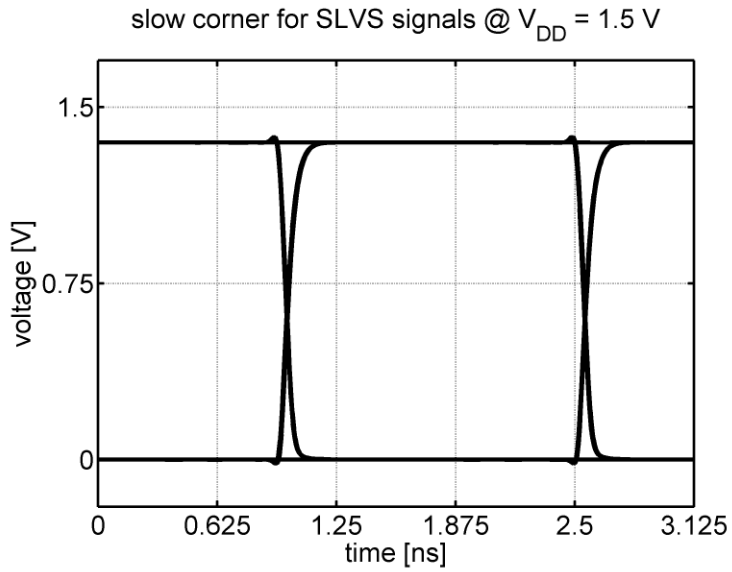


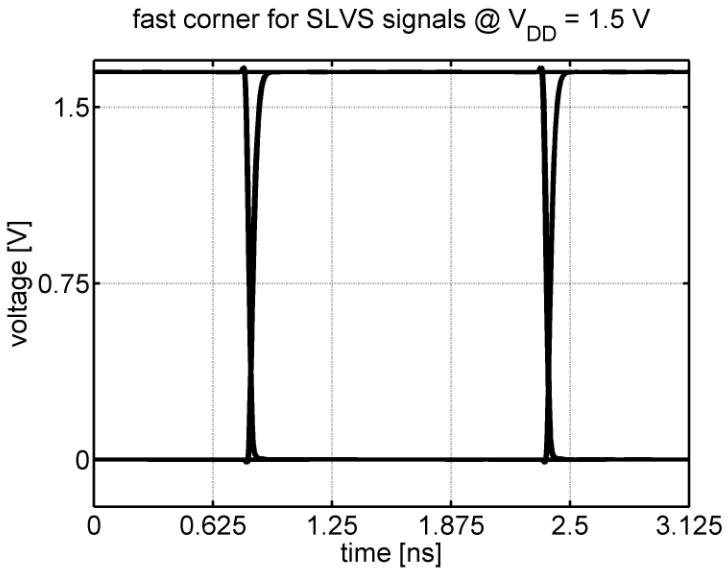
Simulation of the Rx @ V_{DD} = 1.5 V with SLVS input signals

current [µA] / power [µW]:

- typical: 391 / 587
- slow: 439 / 615
- fast: 390 / 644





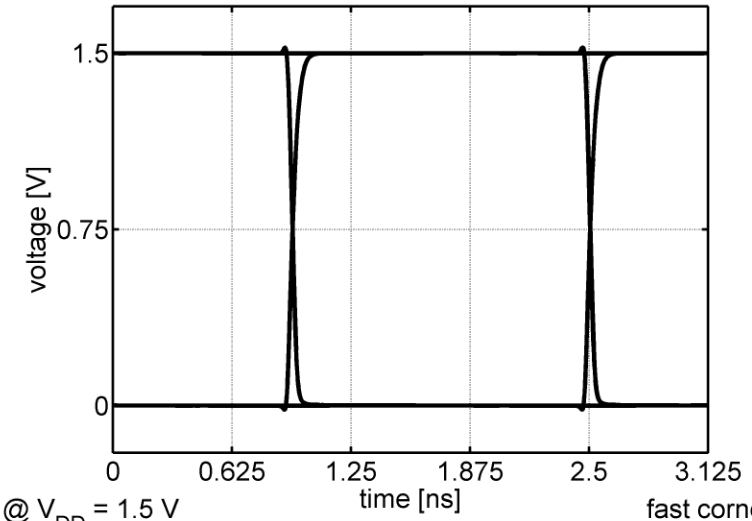


Simulation of the Rx @ V_{DD} = 1.5 V with LVDS input signals

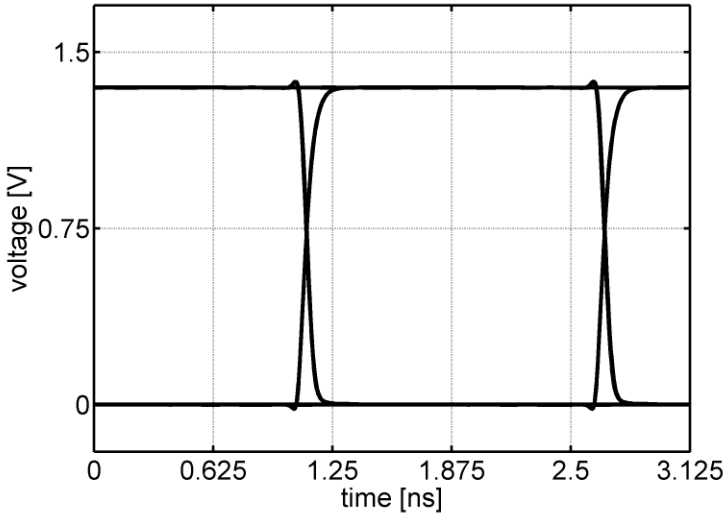
current [µA] / power [µW]:

- typical: 453 / 680
- slow: 474 / 664
- fast: 481 / 794

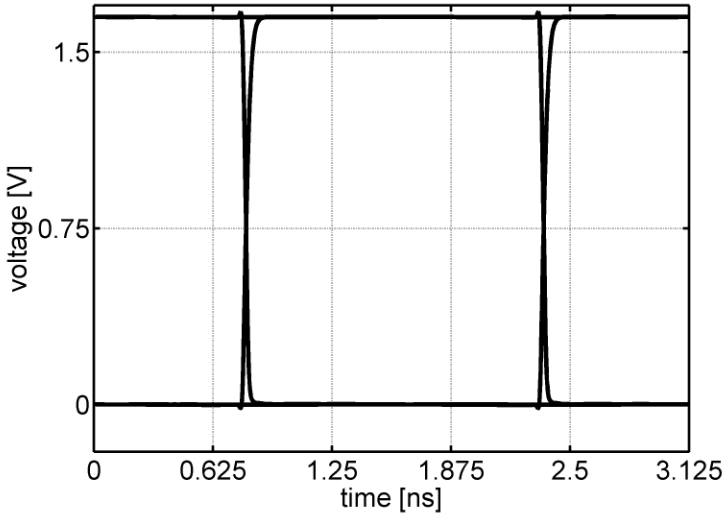
typical corner for LVDS signals @ V_{DD} = 1.5 V



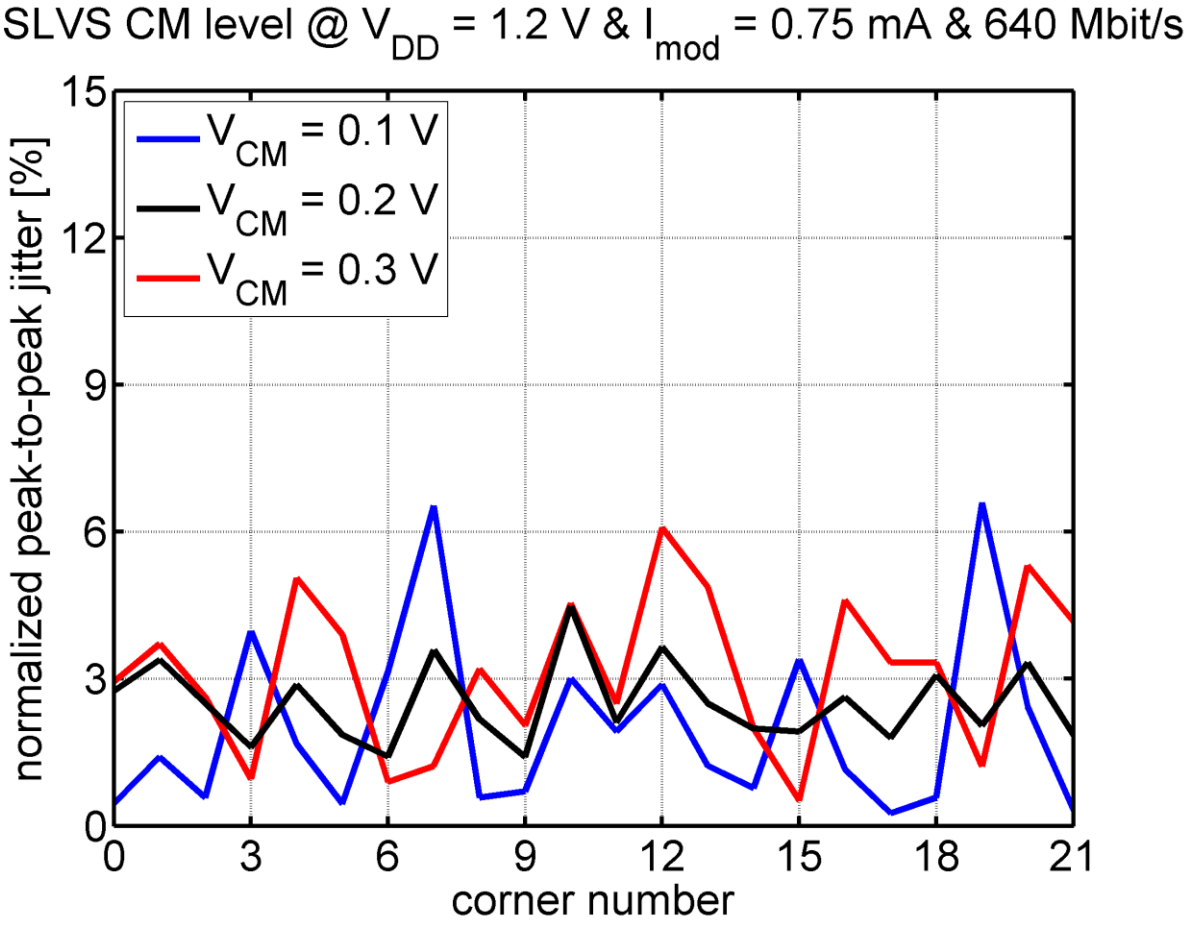
slow corner for LVDS signals @ V_{DD} = 1.5 V



fast corner for LVDS signals @ V_{DD} = 1.5 V

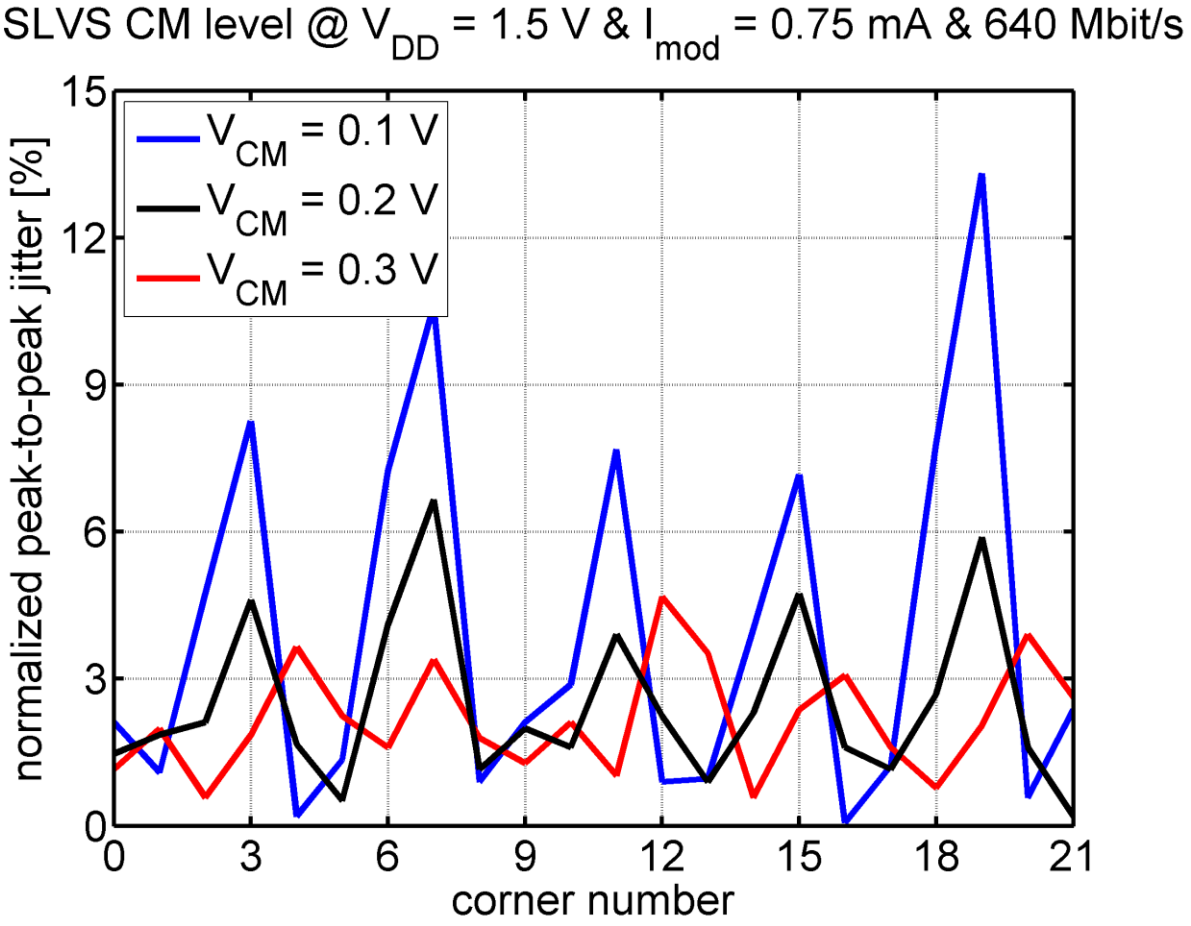


Cross-corner DDJ for **smaller-than-nominal** input signals (1)



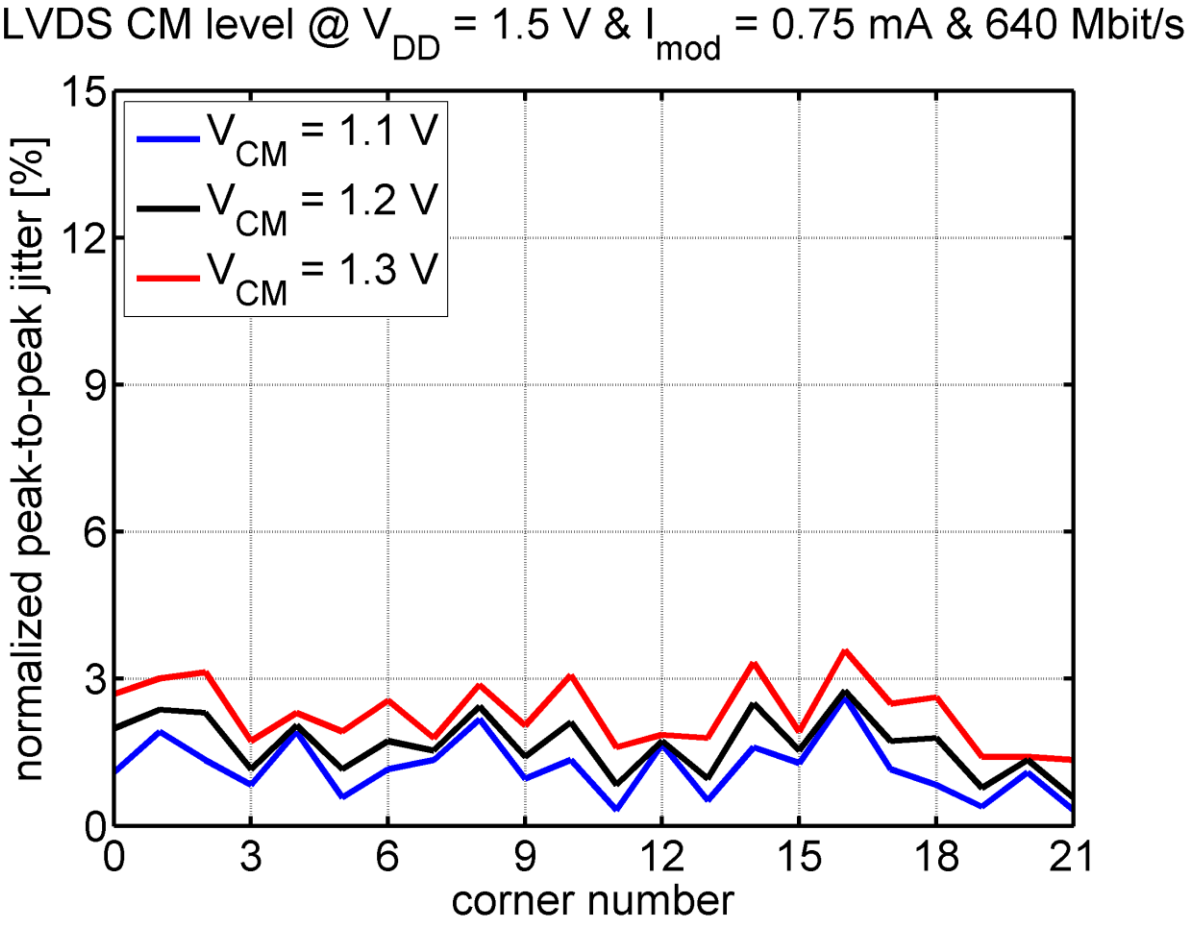
Peak-to-peak jitter is always smaller than 7 % of the bit interval (1.5625 ns @ 640 Mbits/s).

Cross-corner DDJ for **smaller-than-nominal** input signals (2)



Peak-to-peak jitter is always smaller than 14 % of the bit interval (1.5625 ns @ 640 Mbits/s).

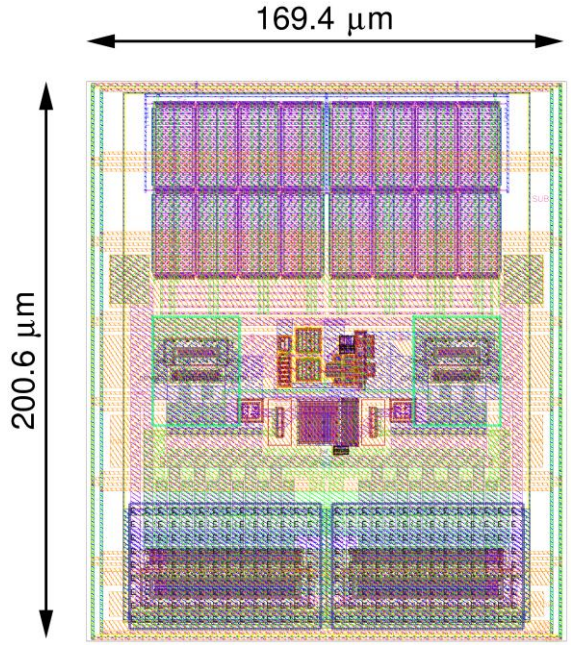
Cross-corner DDJ for **smaller-than-nominal** input signals (3)



Peak-to-peak jitter is always smaller than 4 % of the bit interval (1.5625 ns @ 640 Mbits/s).

SLVS/LVDS Rx versions

	C4	wirebond
technology	IBM 130 nm LM	IBM 130 nm DM
metals used	M1-M4	M1-MA
size	169.4 µm x 200.6 µm	146.28 µm x 215.28 µm
pitch	168.4 µm vertical 199.6 µm horizontal	146 µm vertical 215 µm horizontal



Outline

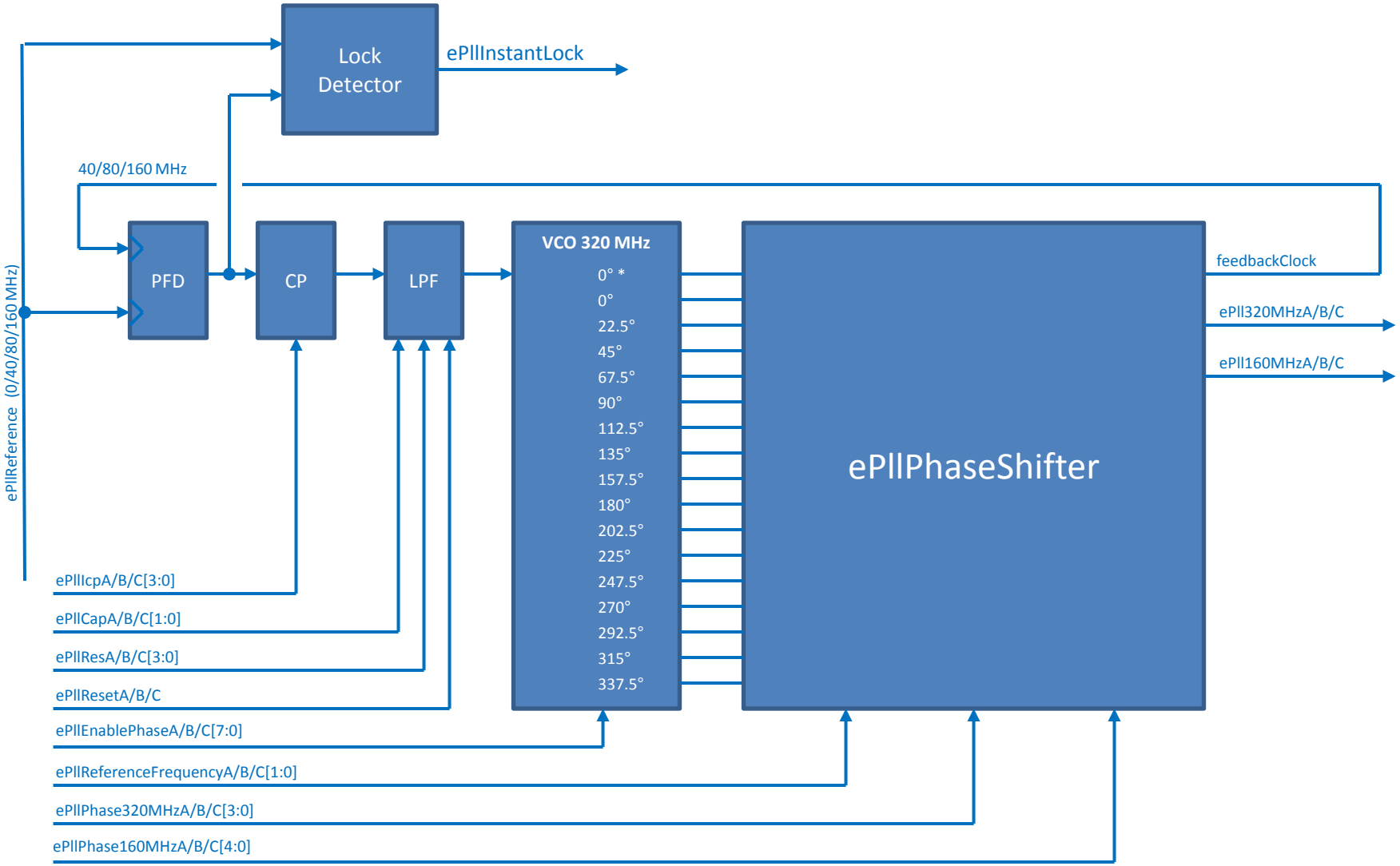
- *SLVS driver and SLVS/LVDS receiver*
- ePLL-FM
- *ePLL-CDR*

General description

The ePll-FM (frequency multiplier) is a highly flexible radiation-hard PLL that is available as a building block in the IBM 130 nm CMOS technology with the DM metal stack (3-2-3). It has the following characteristics:

- input frequency: 40, 80 or 160 MHz
- output frequency: 160 and 320 MHz
- programmable output phase: 11.25° for the 160 MHz clock
  22.5° for the 320 MHz clock
- programmable charge pump current, loop filter resistance and capacitance so as to modify/optimize the loop behavior
- supply voltage: 1.2 V - 1.5 V
- nominal power consumption: 20 mW @ 1.2 V - 30 mW @1.5 V
- operating temperature range: from -30°C up to 100°C

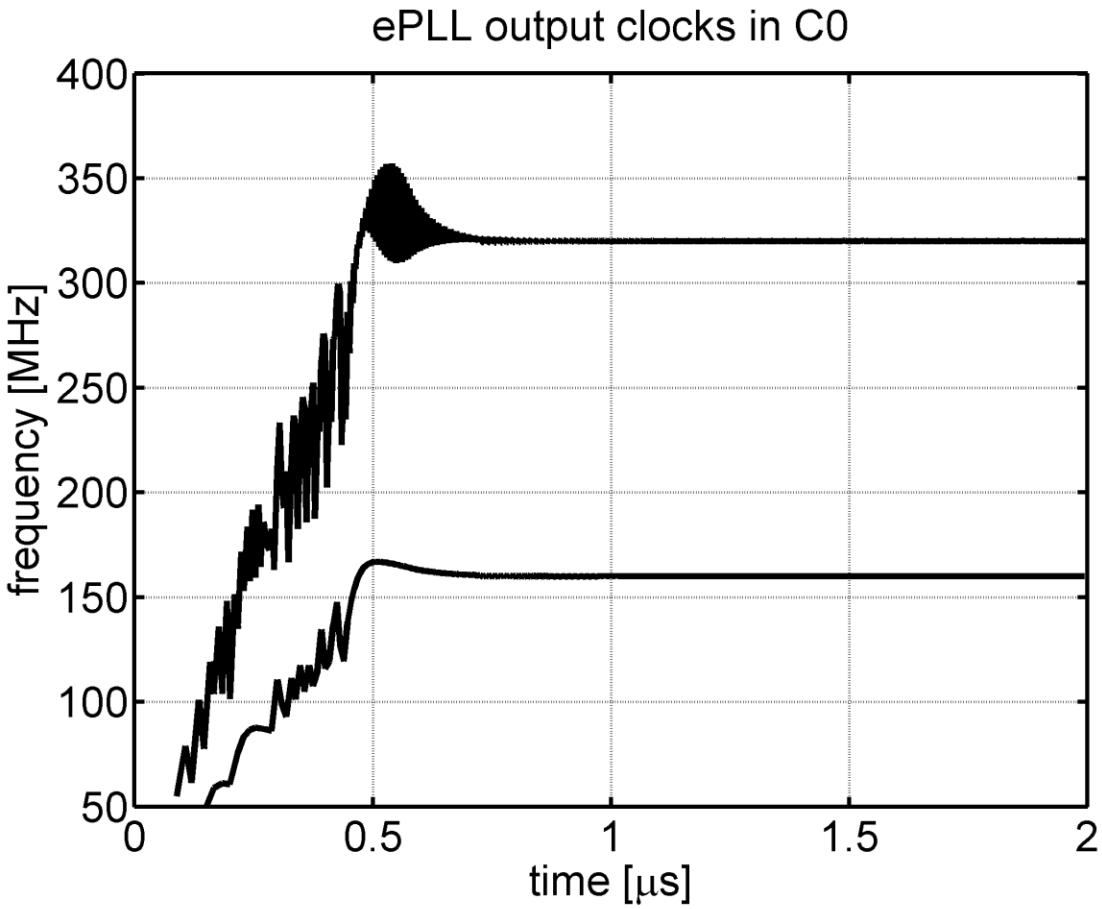
ePll-FM block diagram



Simulation conditions

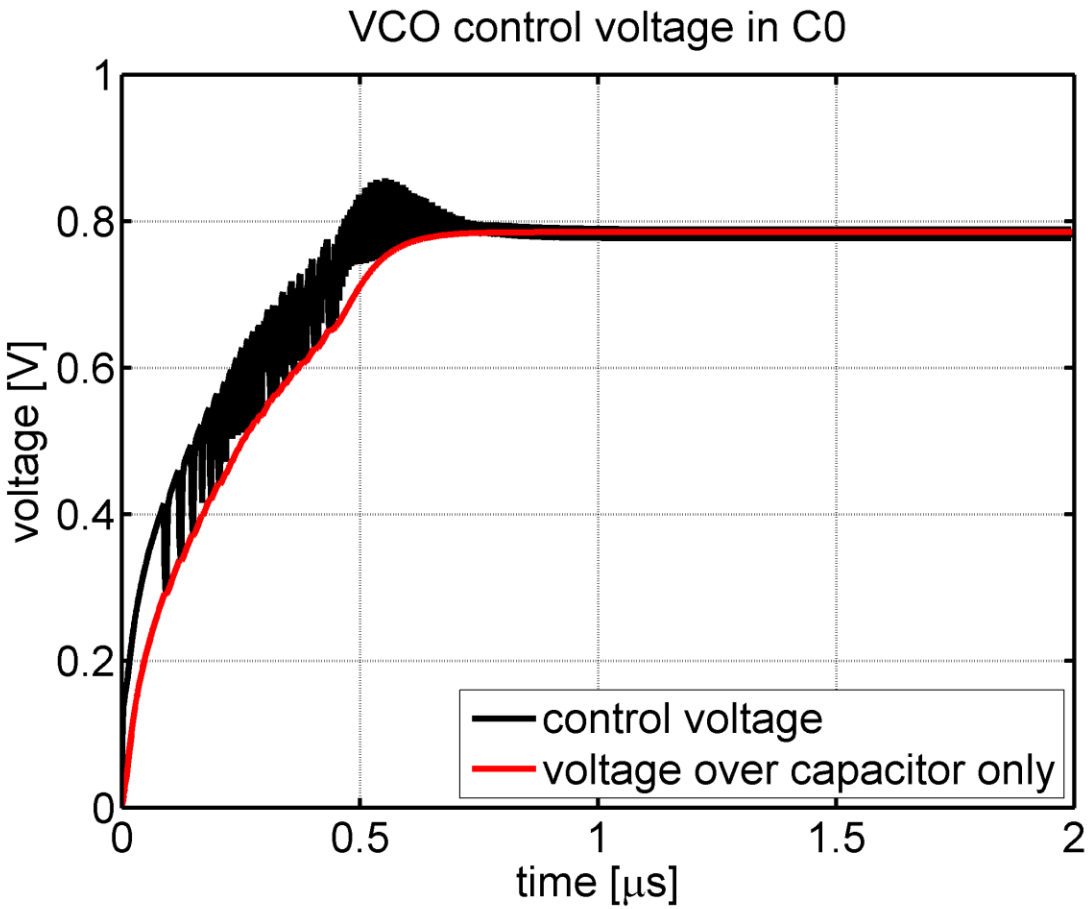
- RC-extracted netlist
- cross-corner transient simulation with 160 MHz input clock
- nominal loop parameter settings for C0:
  - filter capacitance: 50 pF (ePllCap = 10)
  - filter resistance: 1.5 kΩ (ePllRes = 0010)
  - charge pump current: 82.8 µA (ePllIcp = 1011)
- loop is started from a reset condition (control voltage is brought to supply voltage)
- results shown in C0, C9 and C10 only (typical, high and low VCO gain corners)

Simulation in C0 (typical VCO gain)



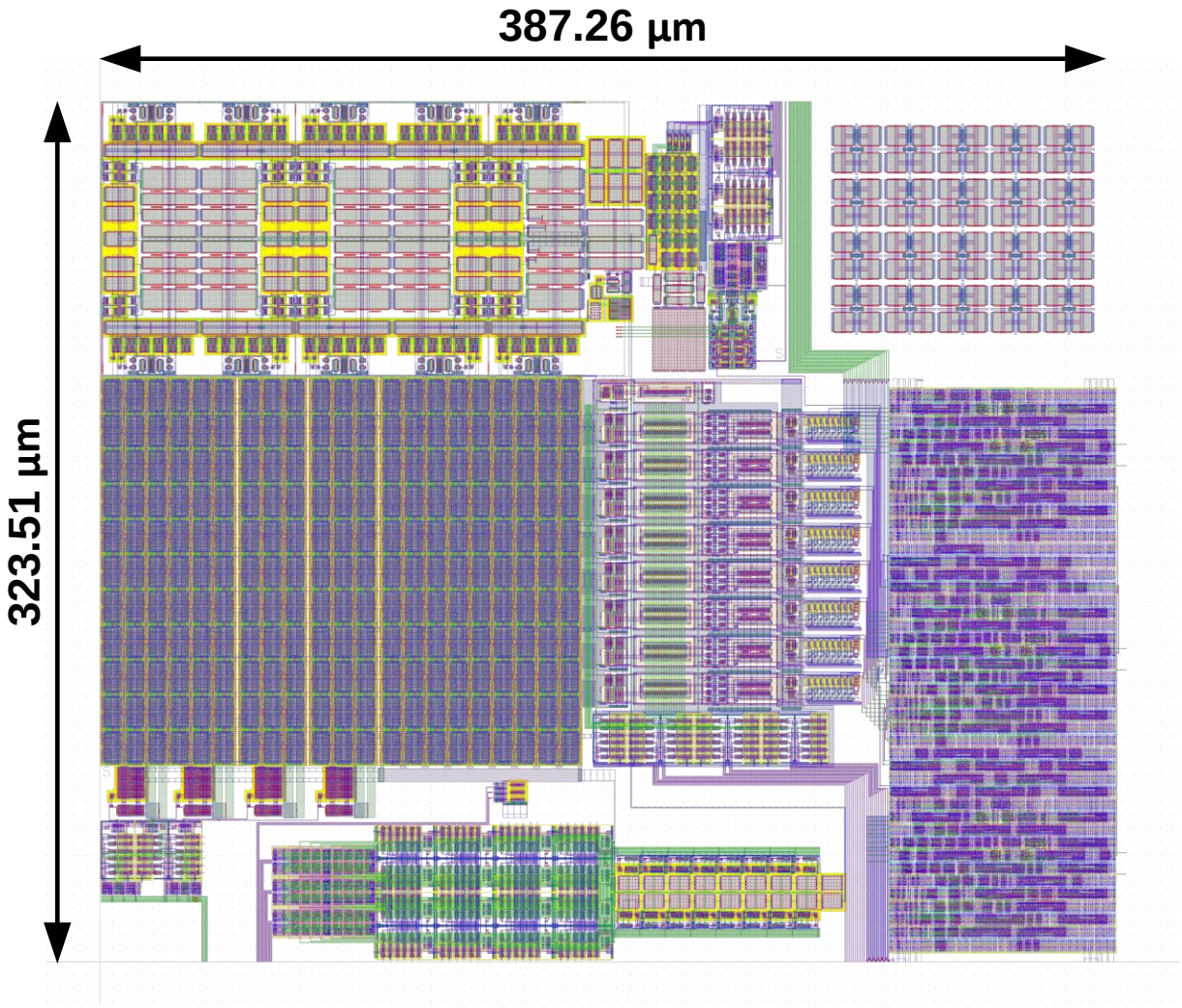
160 MHz and 320 MHz output clocks are stable within ± 750 ns after start-up

Simulation in C0 (typical VCO gain)



The control voltage stabilizes as well within ± 750 ns after start-up at around 0.79 V.

ePll layout



- power grid in MG and LY
- no use of E1 and MA
- no power clamps included
- no ESD on any of the I/O
- ± 12 pF internal power supply decoupling
- thick-oxide filter capacitor to reduce gate leakage

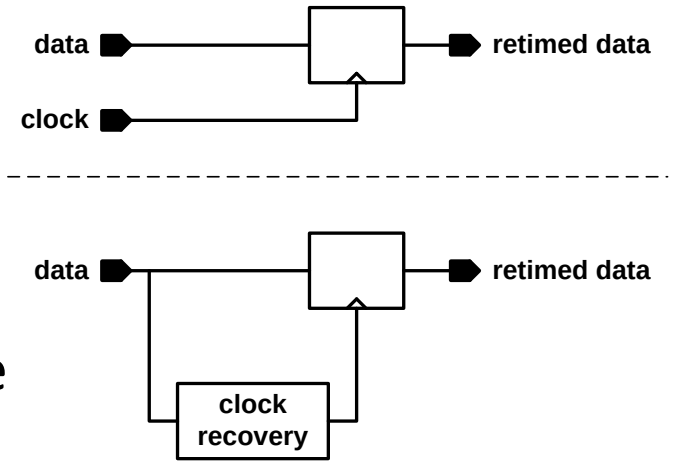
Outline

- *SLVS driver and SLVS/LVDS receiver*
- *ePLL-FM*
- ePLL-CDR

What is the benefit of having a CDR?

2 possibilities to recover the data in the Rx:

- 2 links: 1 for the data, 1 for the clock
  - data recovery by simply resampling the received data with the received clock
  - data recovery
  - expensive channel, easy Rx
- 1 link: only data
  - clocks needs to be extracted from the data after which the data can be resampled by it
  - clock and data recovery (CDR)
  - cheap channel, 'difficult' Rx

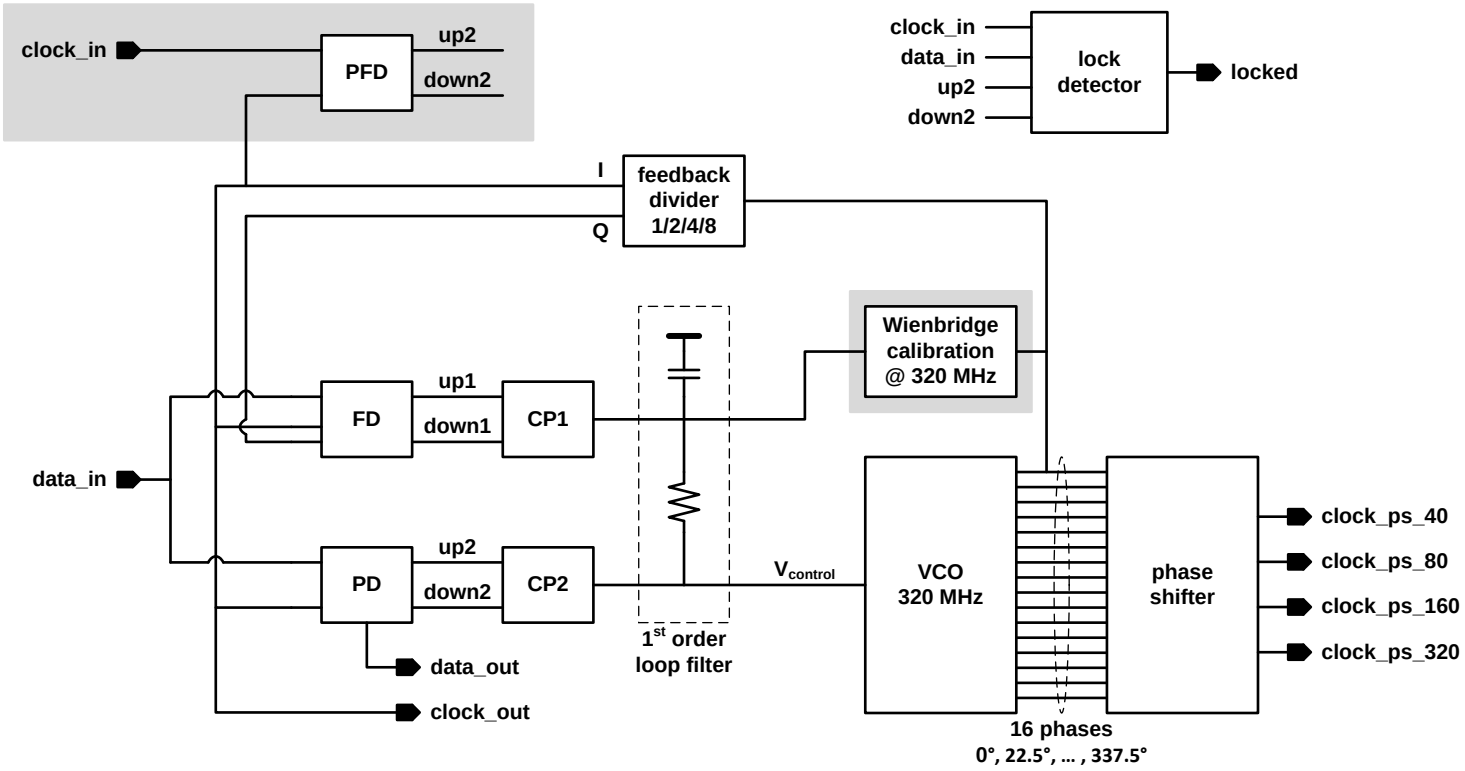


General description

The ePll-CDR (CDR for Clock and Data Recovery) is a highly flexible radiation-hard CDR that is available as a building block in the IBM 130 nm CMOS technology with the DM metal stack (3-2-3). It has the following characteristics:

- data rate: 40, 80, 160 or 320 Mbit/s
- output clocks: data rate clock + 40, 80, 160 and 320 MHz with programmable phase
- internal or external calibration of the VCO frequency
- possible to use it as a frequency multiplier without applying data
- programmable charge pump current, loop filter resistance and capacitance so as to modify/optimize the loop dynamics
- supply voltage: 1.2 V - 1.5 V
- operating temperature range: from -30°C up to 100°C
- under development (tape-out in May 2013, testing in fall 2013)

ePll-CDR block diagram

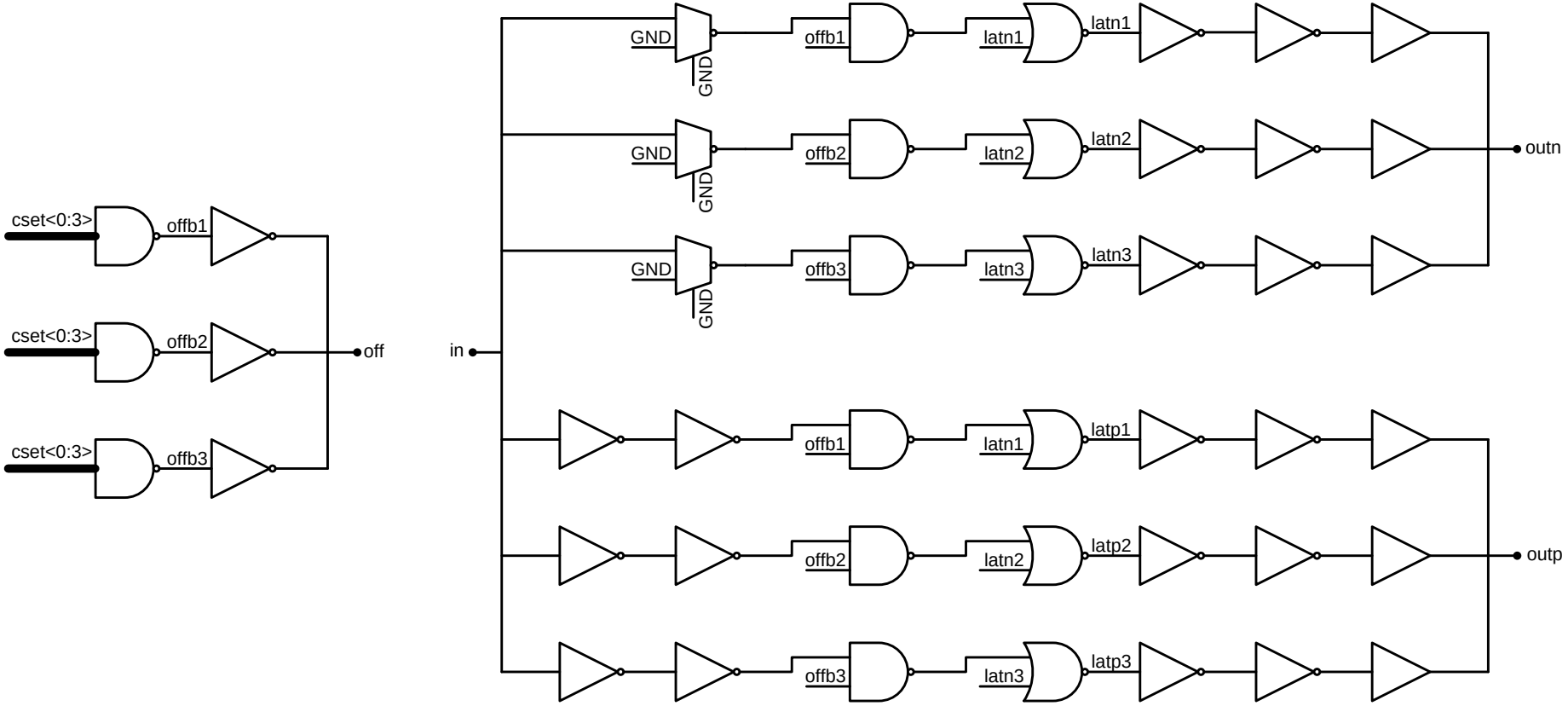


2 calibration possibilities:

- start in 'FM-mode' with an input clock at the same frequency as the data rate
- use the Wienbridge calibration before applying input data

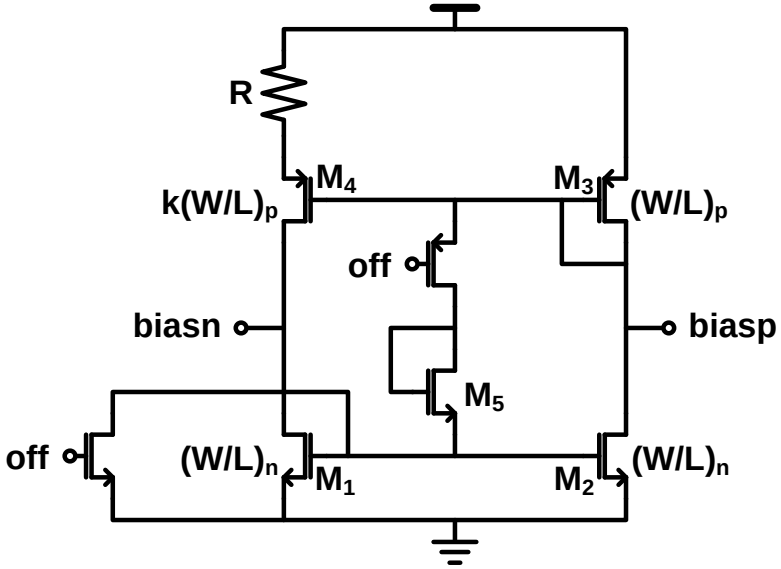
Backup slides

The Tx predriver



- 1 extra inversion in the upper branch results in a differential signal
- Tx is put in the OFF state by raising all of the 'cset' bits to **HIGH**
- off = **HIGH** → outp = **LOW** & outn = **LOW**

Biasing network of the SLVS/LVDS Rx



- current in the 2 branches is equal and completely determined by: $(W/L)_p$, k and R:

$$I = \frac{2}{\mu_p C_{ox} (W/L)_p} \cdot \frac{1}{R^2} \cdot \left(1 - \frac{1}{\sqrt{k}}\right)^2$$

- M_5 is a **start-up** device to force that biasn ≠ 0 V and biasp ≠ V_{DD}:

→ $V_{th,1} + |V_{th,2}| + V_{th,5} < V_{DD,min} = 1.1$ V

→ $V_{gs,1} + |V_{gs,2}| + V_{th,5} > V_{DD,max} = 1.65$ V

Input CM range of the Rx amplifier

- In theory, the Rx amplifier has a rail-to-rail CM input range thanks to the input stage with nMOS and pMOS transistors.
- In reality, the voltage gain changes with varying CM input voltage because the input transistors go out of saturation at 'extreme' CM voltages, reducing as such the gain of the amplifier.
- Note that the correct operation of the Rx amplifier relies on the clipping of the signal at the input of the inverter (see slide 12) so that it can make a reliable decision. This means that the amplifier should not work in its linear region.
- Therefore, the effective CM input range varies with the input signal amplitude (a larger signal can work over a larger CM input range), or alternatively, the minimal signal amplitude depends on the CM input voltage (a smaller signal can be used at the 'optimal' CM input voltage than at the extremes).

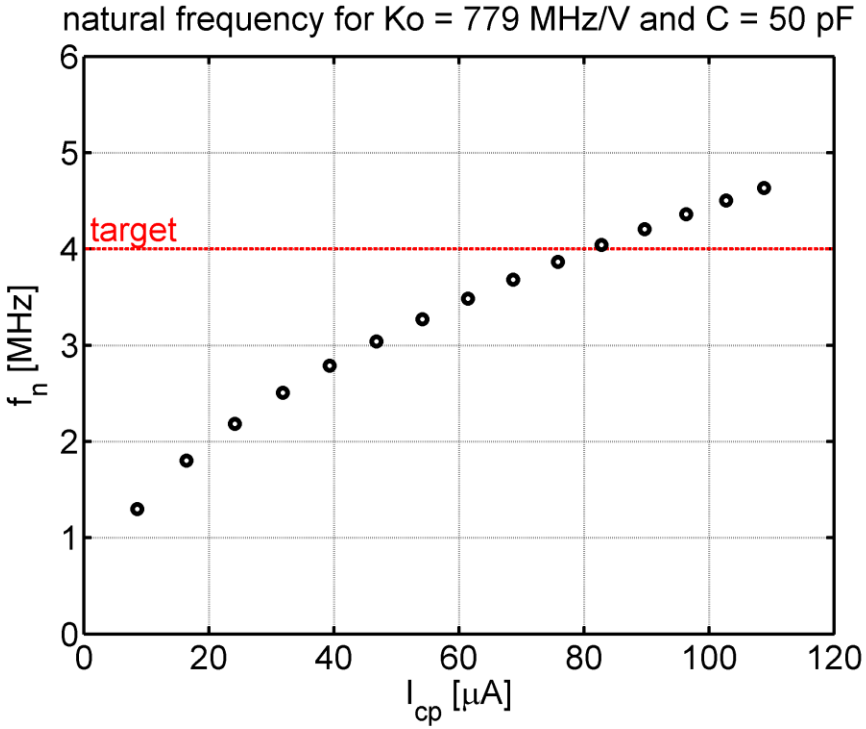
Simulation corners for a supply voltage of 1.2 V

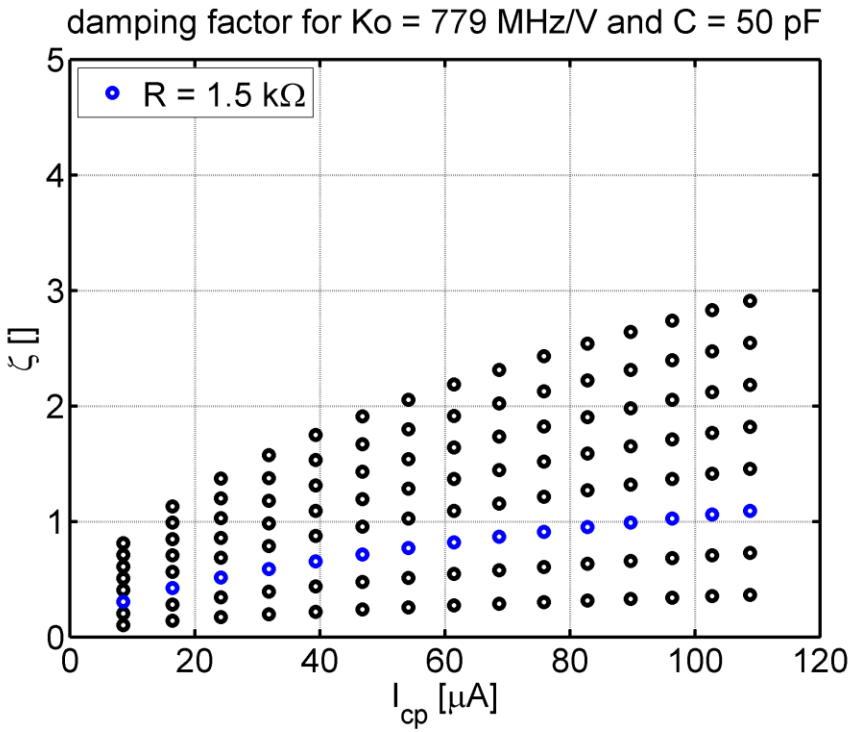
corner	model	temperature	supply voltage
0	TT	25 °C	1.2 V
1	TT	25 °C	1.1 V
2	TT	100 °C	1.1 V
3	TT	100 °C	1.3 V
4	TT	-30 °C	1.1 V
5	TT	-30 °C	1.3 V
6	FF	100 °C	1.1 V
7	FF	100 °C	1.3 V
8	FF	-30 °C	1.1 V
9	FF	-30 °C	1.3 V
10	SS	100 °C	1.1 V
11	SS	100 °C	1.3 V
12	SS	-30 °C	1.1 V
13	SS	-30 °C	1.3 V
14	FS	100 °C	1.1 V
15	FS	100 °C	1.3 V
16	FS	-30 °C	1.1 V
17	FS	-30 °C	1.3 V
18	SF	100 °C	1.1 V
19	SF	100 °C	1.3 V
20	SF	-30 °C	1.1 V
21	SF	-30 °C	1.3 V

Simulation corners for a supply voltage of 1.5 V

corner	model	temperature	supply voltage
0	TT	25 °C	1.5 V
1	TT	25 °C	1.35 V
2	TT	100 °C	1.35 V
3	TT	100 °C	1.65 V
4	TT	-30 °C	1.35 V
5	TT	-30 °C	1.65 V
6	FF	100 °C	1.35 V
7	FF	100 °C	1.65 V
8	FF	-30 °C	1.35 V
9	FF	-30 °C	1.65 V
10	SS	100 °C	1.35 V
11	SS	100 °C	1.65 V
12	SS	-30 °C	1.35 V
13	SS	-30 °C	1.65 V
14	FS	100 °C	1.35 V
15	FS	100 °C	1.65 V
16	FS	-30 °C	1.35 V
17	FS	-30 °C	1.65 V
18	SF	100 °C	1.35 V
19	SF	100 °C	1.65 V
20	SF	-30 °C	1.35 V
21	SF	-30 °C	1.65 V

ePll settings with 160 MHz input clock @ 1.5 V (1)





- Typical VCO gain is 779 MHz/V.
- With a 50 pF loop filter capacitance, the natural frequency can be programmed between 1 and 5 MHz, depending on the charge pump current.
- The wide range of loop filter resistances (0.5-8 kΩ, only 0.5-4 kΩ shown) allows the damping factor to be set in the wanted region (0.7-1.4).