Low Level Interface Implementation plans

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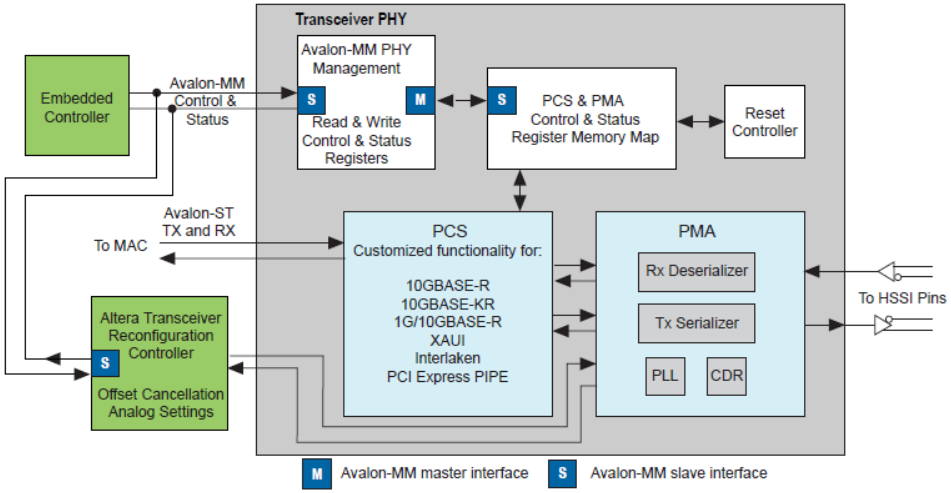
Outline

- General principles
- LLI overview
- GBT and 10GbE/Infiniband blocks
- Pattern memory dimensionning
- Conclusion

LLI General principles



Masks complexity of interfaces

- Physical layer
  - 6 Minipods (~2300 registers)
  - 44 Transceivers PCS & PMA (~5600 registers)
  - 44 Transceivers management (~700 registers)
- MAC layer
  - 12 transceivers (~2000 registers)
- Clock configuration
  - 3 PLLs (24 registers)
- More than10 000 registers in total on a single AMC40 !

Remains independent of any application

- No storage buffer, no fill rate monitoring
- No embedded ECS or TFC function

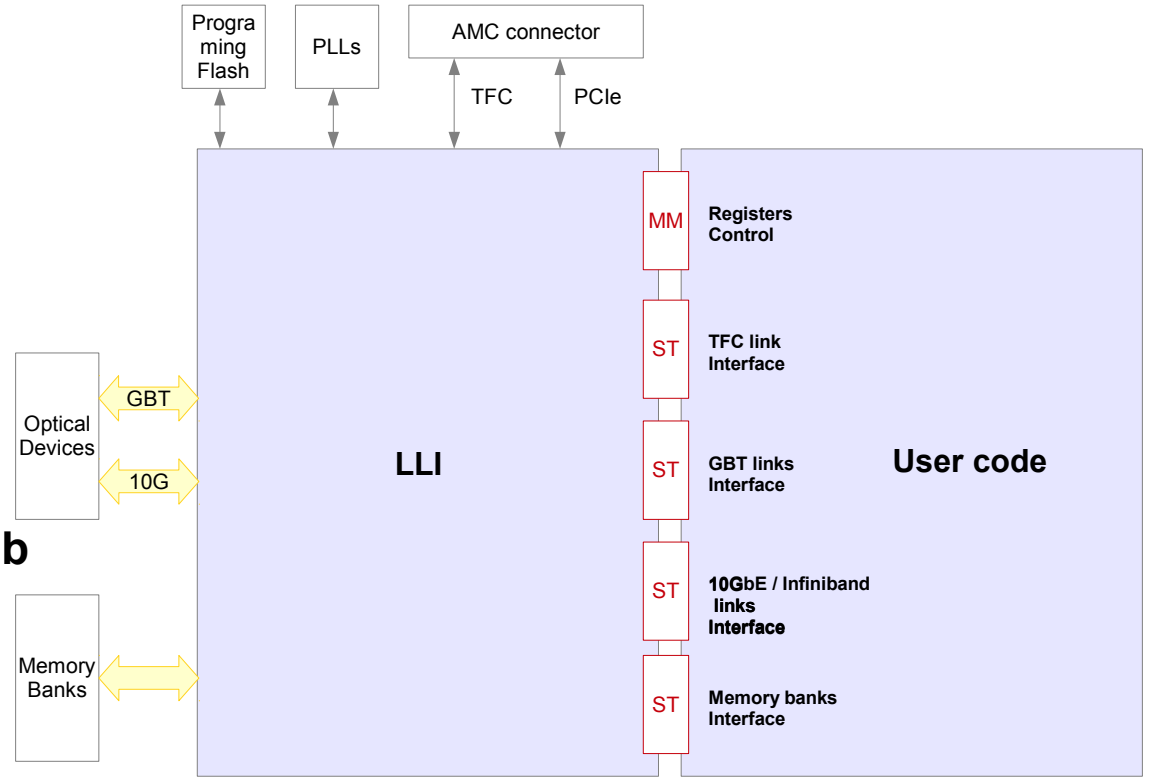
LLI General principles

Clear frontier between LLI and user code

- QSYS Memory Mapped interface
- QSYS Streaming interface

No direct acces to ressources for user

- Access through **Llib** et **Hlib** (see Pierre-Yves presentation)
- Not really a black box: **open source code**
  - Suggestions from users or help welcome



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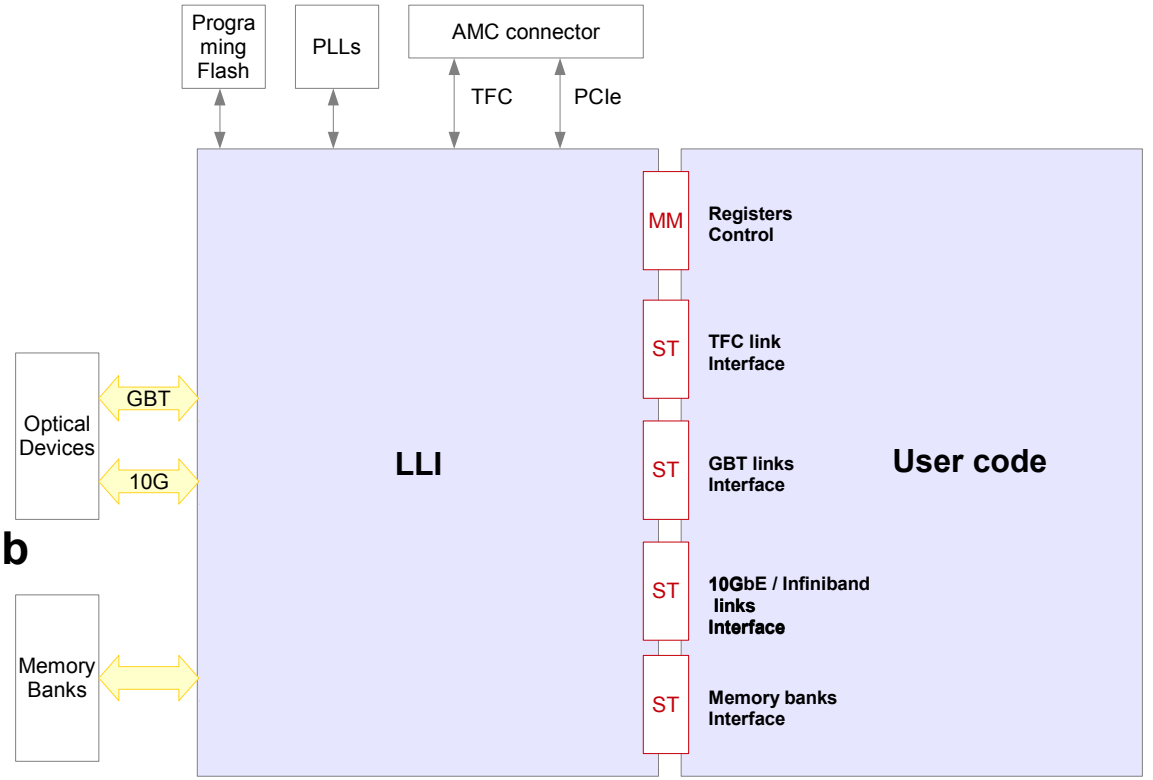


LLI details

Register control MM interface

- 32 bits wide 125 MHz
- Burst mode

TFC Streaming interface

- 48 bits 40 MHz

X-FPGA interface

- 12 bits at 160 MHz

GBT Streaming interfaces

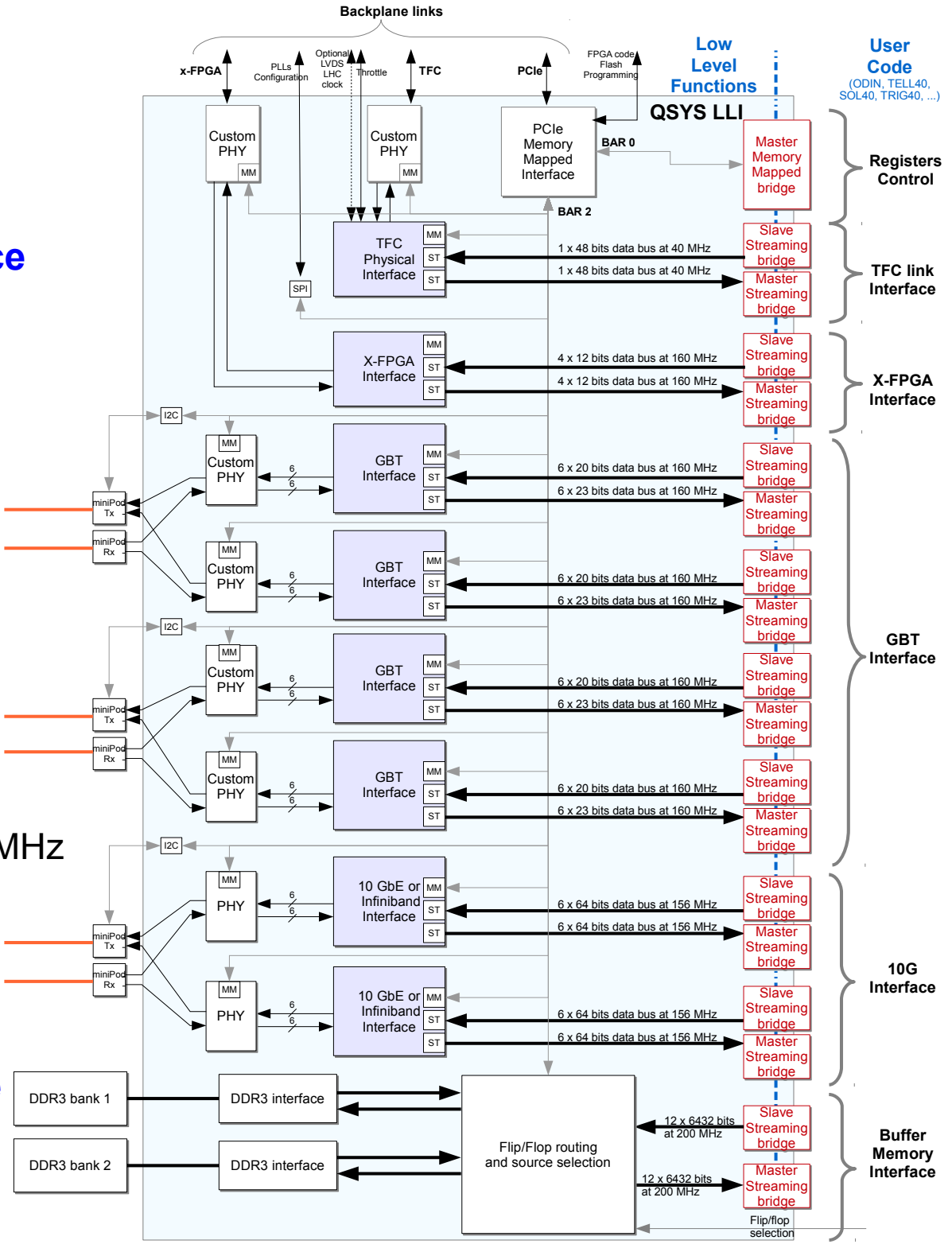
- 24 x 20 or 23 bits 160 MHz

10G Streaming interfaces

- 12 x 64 bits 156 MHz

Memory Streaming interface

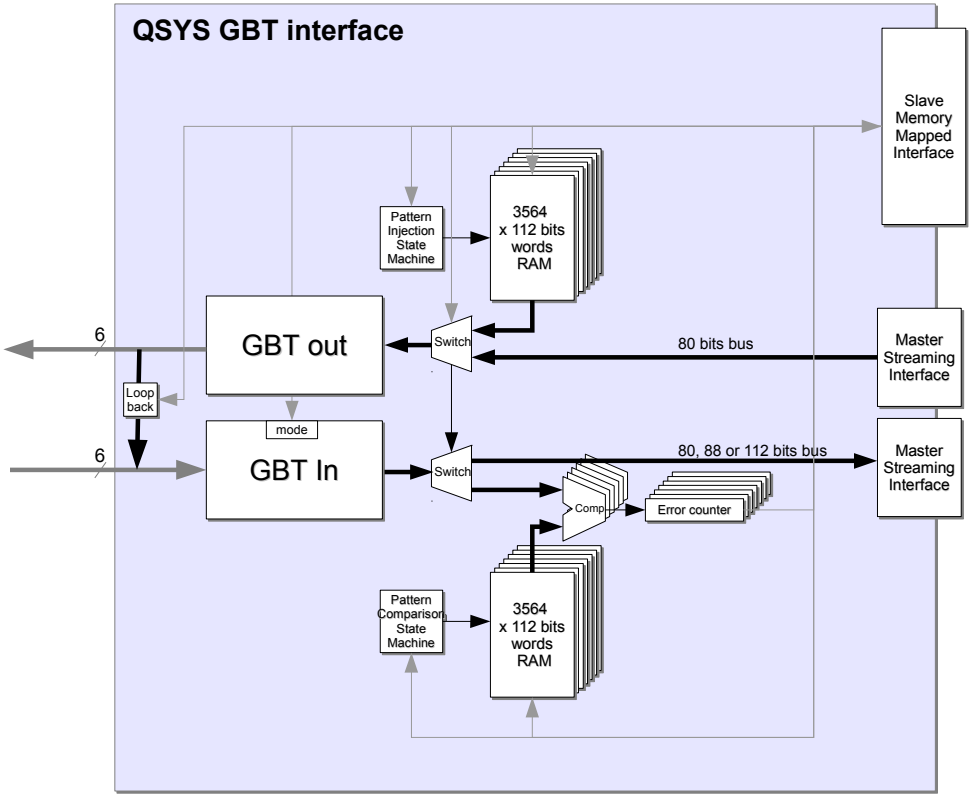
- 12 x 32 bits 200 MHz

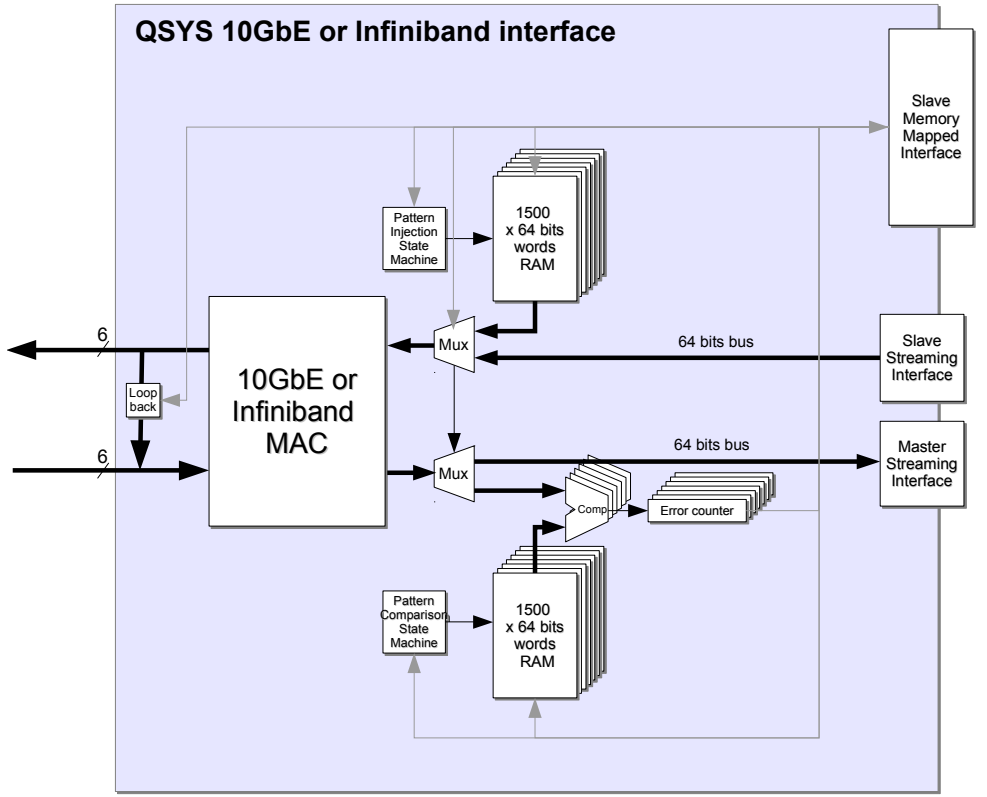


GBT and 10GbE or Infiniband blocks

Ideal design:

- Pattern generator and reference pattern in RAM
- Pattern generator can be looped back for injecting emulated data





Memory size dimensionning and associated features

Size of injection patterns

- 3564 x 112 x 24 x 2 = 19 Mbits (= 36 % Stratix V GX memory)
  + 1500 x 64 x 12 x 2 = 2.3 Mbits (=4.6 %)
  - ➔ 40 % certainly too much

Clues for reducing size

- GBT injection of only one quarter of a machine cycle
  - ➔ 13.6 %
- Use same memory for injection and comparison
  - ➔ 7 %
- Use a single injection memory for 6 serial links
  - ➔ 1.5 %

Proposal

- GBT injection of only one quarter of a machine cycle (13.6%)
- Can be improved latter on if required: incremental approach
  - ➔ Users must express their needs

Conclusion

Ongoing specification document

- Will be circulated ASAP for comments

LLI development will follow an incremental approach

- Simple version for Early Setups including :
  - 6 GBT streaming interfaces
  - 1 TFC streaming interface
  - 1 Control Register memory mapped interface
- Improved version with 10 GbE
- Improved version with Infiniband
- Full version with DDR3 interface

Improved Llib et Hlib version provided at each step

Backup

Minipods registers

Byte	Type	Lower Memory Page 5ih for TX, 6i for RX
0	RO	Identifier
1-2	RO	Status
3-27	RO	Interrupts Flags: LOS, Fault, Monitor
28-39	RO	Module Monitors (internal temperature, Vcc33, Vcc25
40-87	RO	Channel Monitors (TX bias, TX Output Power, RX Input Power)
88-89	RO	Elapsed Operating Time
90	RWn	Reserved
91-105	RWv	Volatile Controls (Reset, CH Diasble, CH Squelch Diable, TX Margin Enable, RX Rate Select)
106-117	RWv	Masks: LOS, Fault, Module Flags
118-126	RWv	Reserved
127	RWv	Upper Page Select Byte

RO	Read Only
RWv	Read/Write volatile
RWn	Read/Write non-volatile

Byte	Type	Upper Memory Page 00h
128-129	RO	Identifiers
130	RO	Description: Power Supplies
131	RO	Description: Max Case Temp
132-133	RO	Description: Min/Max Signal Rate
134-137	RO	Description: Wavelength
138-143	RO	Description: Supported Functions
144-151	RO	Reserved
152-170	RO	Vendor Information: Name & OUI
171-188	RO	Vendor Information: PN & PN rev
189-204	RO	Vendor Information: SN
205-212	RO	Vendor Information: Date Code
213-222	RO	Vendor Information: Customer Specific
223	RO	Checksum
224-239	RWv	Reserved
240	RO	Reserved
241-253	RO	Vendor Specific
254-255	RO	Reserved

Byte	Type	Upper Memory Page 01h
128-175	RO	Module Thresholds
176-223	RO	Channel Threholds
224	RO	Checksum
225.243	RWn	Non-volatile Controls (IntL Mode, CH Polarity, TX Equalization, RX De-emphasis & Output Amplitude)
244-255	RWv	Masks: Channel Monitor Flags

Transceivers configuration