Calorimeter electronics review summary

Summary of the review
Answers to the referees

On behalf of the calorimeter upgrade group

Upgrade Electronics meeting

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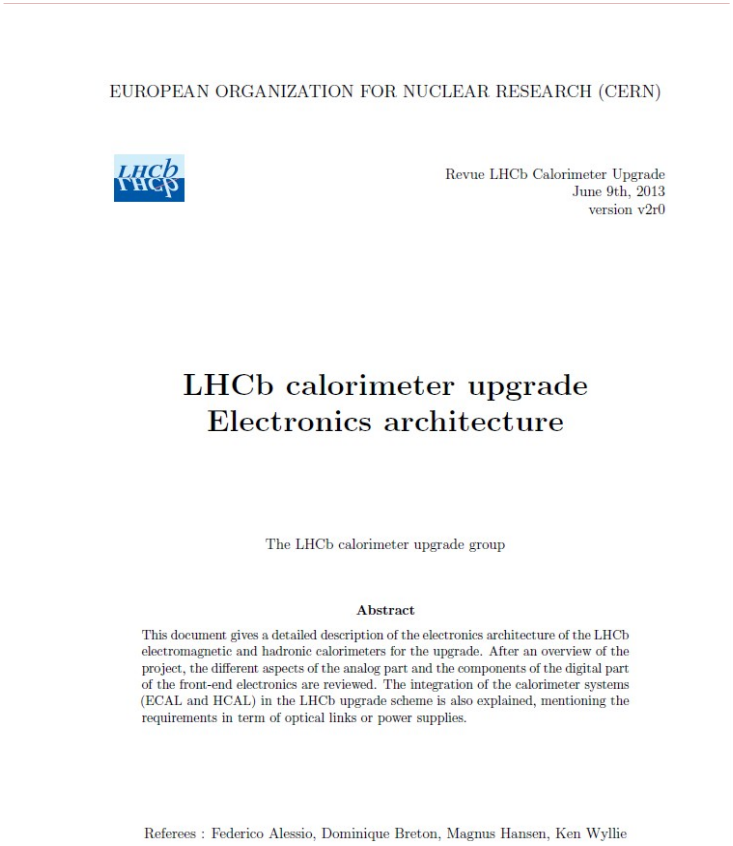
Scope of the Upgrade of the calorimeter

- The upgrade consists of
  - running the experiment up to $2x10^{33}cm^{-2}.s^{-1}$
    - x5 with respect to max reached
  - Integrate up to $L=50fb^{-1}$
- Scope of the upgrade – what is kept or modified ?
  - On the detector side:
    - most of the modules are kept → some modules (inner region) replaced (LS3)
    - PMT → a reduction factor is applied on the gain to keep them alive
    - Cockcroft-Walton bases (and PS) , signal cables, etc... are kept
    - Remove the SPD, PRS and Lead absorber
  - On the balcony:
    - Keep the crates, backplanes, power supplies,...
    - Replace the Front-end electronics (GBT 40MHz readout)
      - Make it compliant with the crates, power supplies, ...
    - Keep the L0-Calo electronics → modified to be a LLT-Calo
  - Counting room:
    - TELL1 → GBT
    - Slow control : GBT-SCA

Report on the Calorimeter electronics review

- The Calorimeter electronics was reviewed at the end of June
- Agenda
  - Morning :
    - Introduction
    - Analog electronics
  - Afternoon
    - Digital electronics
- 4 referees
  - Federico Alessio (CERN)
  - Dominique Breton (LAL/Orsay)
  - Magnus Hanssen (CMS)
  - Ken Wyllie (CERN)
- Information (slides, document supporting the design, report) can be found at
  http://indico.cern.ch/conferenceDisplay.py?confId=256798
- We would like to thank the referees for the careful study of the system and the fruitful comments we received concerning the design



EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH (CERN)

Revue LHCb Calorimeter Upgrade
June 9th, 2013
version v2r0

LHCb calorimeter upgrade
Electronics architecture

The LHCb calorimeter upgrade group

Abstract

This document gives a detailed description of the electronics architecture of the LHCb electromagnetic and hadronic calorimeters for the upgrade. After an overview of the project, the different aspects of the analog part and the components of the digital part of the front-end electronics are reviewed. The integration of the calorimeter systems (ECAL and HCAL) in the LHCb upgrade scheme is also explained, mentioning the requirements in term of optical links or power supplies.

Referees : Federico Alessio, Dominique Breton, Magnus Hansen, Ken Wyllie

General remarks from the reviewers (I)

- No major problem with the foreseen implementation
  - Based on the present system that works well
- Expensive crates and power supplies re-used → cost efficiency. The presented system also offers a viable solution to be compatible with the FE crate backplanes.
- An intensive discussion during the review to see whether other auxiliary boards could be removed → no viable solution was found
- Data format and event size is fixed and there is no need for sparsification
- Full GBT bandwidth is used allowing for a reasonable number of links
- Removal of the TVB and direct transmission of the trigger data to the farm is agreed → removes a level of complexity of the system
  - LLT increases the complexity although the solution is clearly defined and feasible
  - Using a common link for data and trigger would save 1 link per board.

General remarks from the reviewers (II)

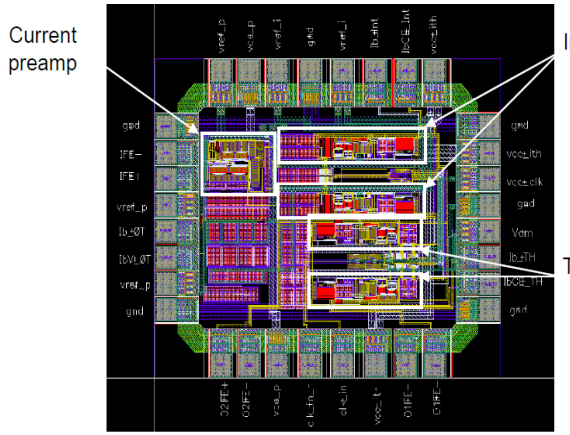
- Demands on spill-over, dead-time, efficiency are solved in the analog domain
  - Recommendation is to investigate whether digital filtering could be considered after ADC conversion to relax the requirements on the analog circuitry
  - If it means to perform a waveform digitization in real time
    - Major change of the philosophy
    - Test bench/beam measurements indicate that the performances are ok
    - Sampling rate ~>200Ms/s → A3PE cannot do it
      - Process in the barracks after full data transfer and with a fast electronics
      - How can we conceal this with the LLT ?
      - Cannot afford this (money, manpower, time scale)
    - Can be considered only if a problem occurs on the current design
- Radiation levels in the region of the calorimeter are modest (~ 100 rad/fb^{-1})
  - Care must be taken in the selection of the components
    - Many components which had been tested for the present electronics are planned to be re-used for the upgrade
    - The reviewers endorse the plan to irradiate a complete FE prototype
    - This is something we want to do in 2014
      - Difficulties to find good beam conditions
      - Probably useful to perform dedicated irradiation of specific components also.

General remarks from the reviewers (III)

- Manpower is scarce in many areas
  - Many people (physicists) who contributed to the calorimeter software/firmware are now busy with the data-taking and the analysis of the data
  - The situation will have to improve to finalize the calorimeter system

- The proposed planning meets the requirements if the manpower issues are resolved

Analog electronics (I)



- 2 solutions pursued in parallel
  - ASIC and COTS (Components Off The Shelf) systems. Both solutions have pros ans cons.
  - The decision on the adopted solution should be more clearly defined
  - Decision criteria proposal
    - The solutions must fulfill requirements
      - Very close, but not the case yet for any (plateau: ASIC & spill-over: COTs)
    - The test must be done in a significant number of channels (10 – 50)
      - Cannot choose before having a 4 channel ASIC working
    - Consider non-vital aspects: cost, detector intervention, power, requirement of additional complexity (e.g. delay chips)

- The present prototype implements 2 options
  - Common and separated grounds
  - The reviewers suggest to have an equi-potential ground widely interconnected between ground planes and to adopt it as a baseline
  - Was interesting to test common and separate grounds …
    - We will of course follow the LHCb philosophy for what regards grounds
    - ground mesh as recommended by reviewers (mixing strategies is dangerous)

Analog electronics (II)

- The ASIC solution is based on two interleaved integrators
  - The calibration of the two paths should be more clearly addressed
  - Should the integrator performing the charge measurement be tagged in the data ?
    - Dynamic pedestal subtraction should remove any offset difference
    - Calibration difference should be <5%
    - Nevertheless the DLL generates the 20 MHz clock based on a divider which is synchronously reset with the bunch ID reset
      - Odd/even BCID belong to a given integrator
      - Tagging exists by construction and offline correction can be applied

- In the present analog design spill-over seems to be solved. Nevertheless, it could be considered to remove the effect at the digital level
  - It could be interesting to study spill-over removal in the digital processing
  - This would require MC simulations
  - This is indeed a very good point that we must evaluate precisely
    - We are crually missing manpower... if someone is interested

Analog electronics (III)

- The analog requires a large number of phase adjustable 40MHz clocks
  - The clock resources of the GBTX should be maximally used
  - We want to minimize clocks and we will use the GBT when we can
    - Not sure we will have enough clocks on the GBT for the COTS solution
    - Additional clock phases are needed for the ASIC
      - But they are generated in the ASIC (delay chip to test the block seems to be successful)
      - The alignment between different clocks phases of a channel will be fixed
      - At the end: a phase per channel and a global phase to be adjusted.

- Slow control of the analog well integrated to the global architecture
  - A solution could be found to generate a refresh pulse for the triple voting registers of the SPI interface reset. An ad hoc pulse could be transmitted regularly in the ECS field of the TFC+ECS word to the FE in order to refresh the TMR registers without the need to use a fast command for this purpose
  - Want SPI to be quiet during collisions. Would be happy to have such a signal...

- The effect of digital clock activity on the analog circuitry should be investigated when the full prototype is available
  - Indeed this is an important study → fully agree

Digital electronics + infrastructure (I)

- Design seems compatible with the global scope of the upgrade of the calo
  - 4 TRIG40 (4 AMC each)
  - 2 SOL40
  - 11 TELL40
  - 1 or 2 ATCA crate (TRIG+DATA+Slow_control) are enough

- Architecture require
  - ~ 260 New FE board
  - ~ 20 New control board (located in the central slot of the crates)

- The reviewers wondered whether the number of FPGA could be reduced
  - This a possibility that can emerge from the design process
    - We will of course try if we have enough resources
  - We are advised to look at the new SmartFusion FPGA from MicroSemi
    - A3PE seems to be a good compromise between costs, radiation tolerance and resources. This needs some investigation.

Digital electronics + infrastructure (II)

- The packing algorithm is simple and robust:
  - No compression and zero-suppression
  - Latency is fixed, BXID is sent at every clock cycle

- GBTX uses the SLVS type signals (low common mode and low excursion)
  - We claim this could be dangerous is we want to use our backplane and propagate those signals on it
    - Suggest to transform it to LVDS on the boards (FPGA) before backplane transmissions
  - The referees ask to evaluate this method in term of clock phase and jitter
    - Re-use of the backplane has clear advantages for distributing clock, SC, TFC
    - Usage of FPGA or buffers may lead to jitter, clock phase
  - We want to test jitter, clock phase on the next prototype
  - GBT should be implanted on the next PCB when available
  - Still, we do not plan to have SLVS on the backplane (SLVS seems risky)

SLVS is a chip-to-chip signaling protocol which is designed from the beginning for maximum performance and minimum power consumption.

  - NB: We will need buffers anyway, so the argument of the jitter is valid... whatever the signal standard used !

Digital electronics + infrastructure (III)

- Serialisers and optical emitters are on mezzanines in baseline architecture
  - A direct implementation of the link on the PCB could lead to a sensible cost reduction
  - Could resolve some potential cooling problems related to the use of a mezzanine
  - We decided to get rid of the optical mezzanines and to go for a full PCB implementation

- Design of mezzanines (slow control for auxiliary systems) is not fully defined
  - This is true: Work on the slow control mezzanines starts now

- Referee in favour of the possibility of programming the FPGA in situ
  - Of course, we have always said that we want it !

Some other issues

- The calorimeter group foresses to re-use a fraction of the present system
- This has consequences on the spares
- We are already thinking about replacing modules and PMT because of the aging
- We may imagine to replace other systems
  - Power supply
  - Can bus
  - …
- Our group did not spend much time thinking of those problems
- This is a problem common to several groups in LHCb
  - Could it be the subject of a discussion
  - Is there a global strategy on spare and equipments like PS, … in LHCb ?