

STATUS OF DCDC DEVELOPMENT

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CERN, PH-ESE

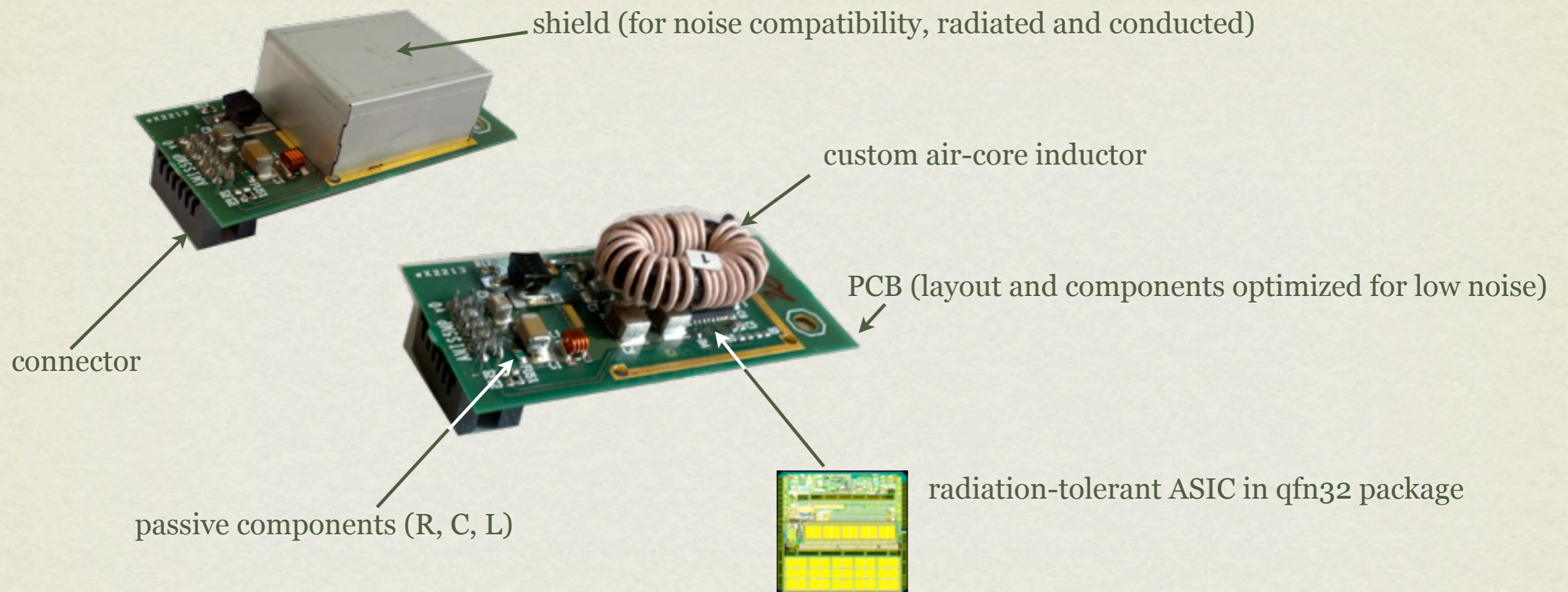
<http://project-dcdc.web.cern.ch>

GOAL



	positive	negative
V_{in}	6 to 12V	positive, $6V < V_{in} - V_{out} < 12V$
V_{out}	0.9 to 5V	-0.9 to -5V
I_{out}	$\leq 4A$ (but $P_{out} \leq 10W$)	as positive
protection features	OCP, OTP, UVLO	as positive
radiation hardness	$> 10Mrad$, $> 5E14$ n/cm ² , SEE tolerance	as positive
magnetic field	4T	as positive
conducted noise	class B (CISPR11)	as positive

COMPONENTS



COMPONENTS

	production-ready
ASIC	
Custom inductor	
Shield	
Connector	
PCB design	

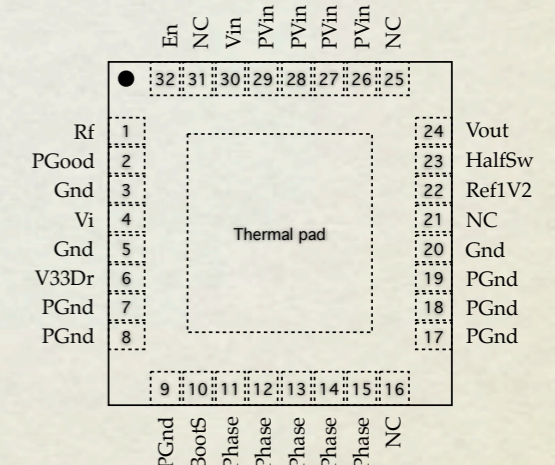
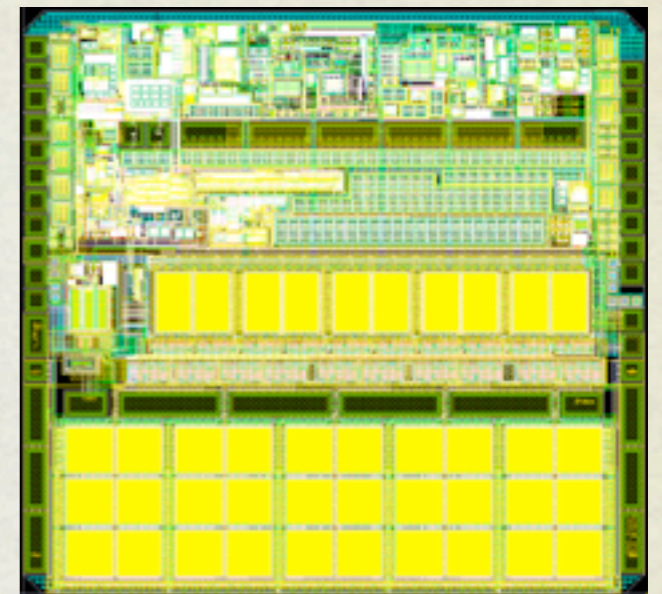
ASIC: FEAST

- Some features:

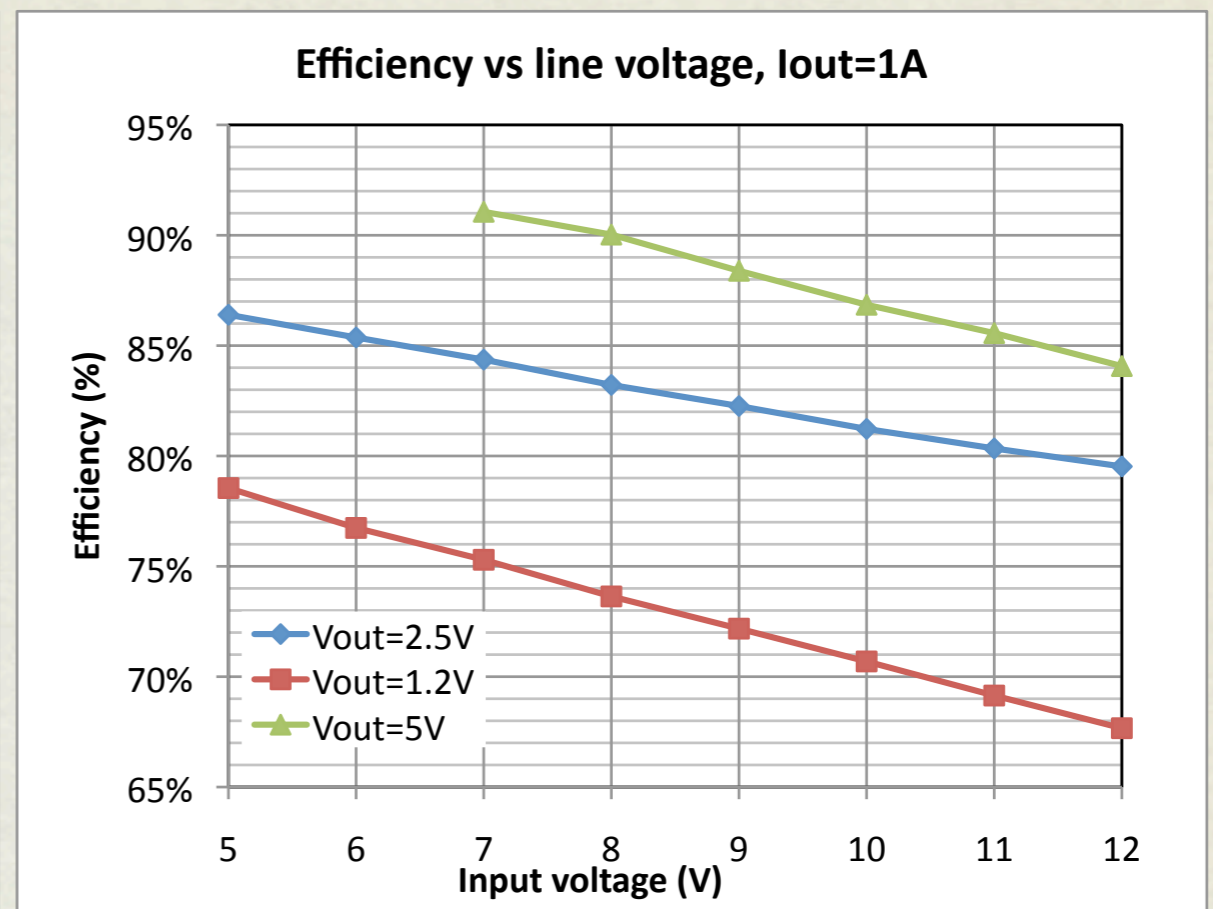
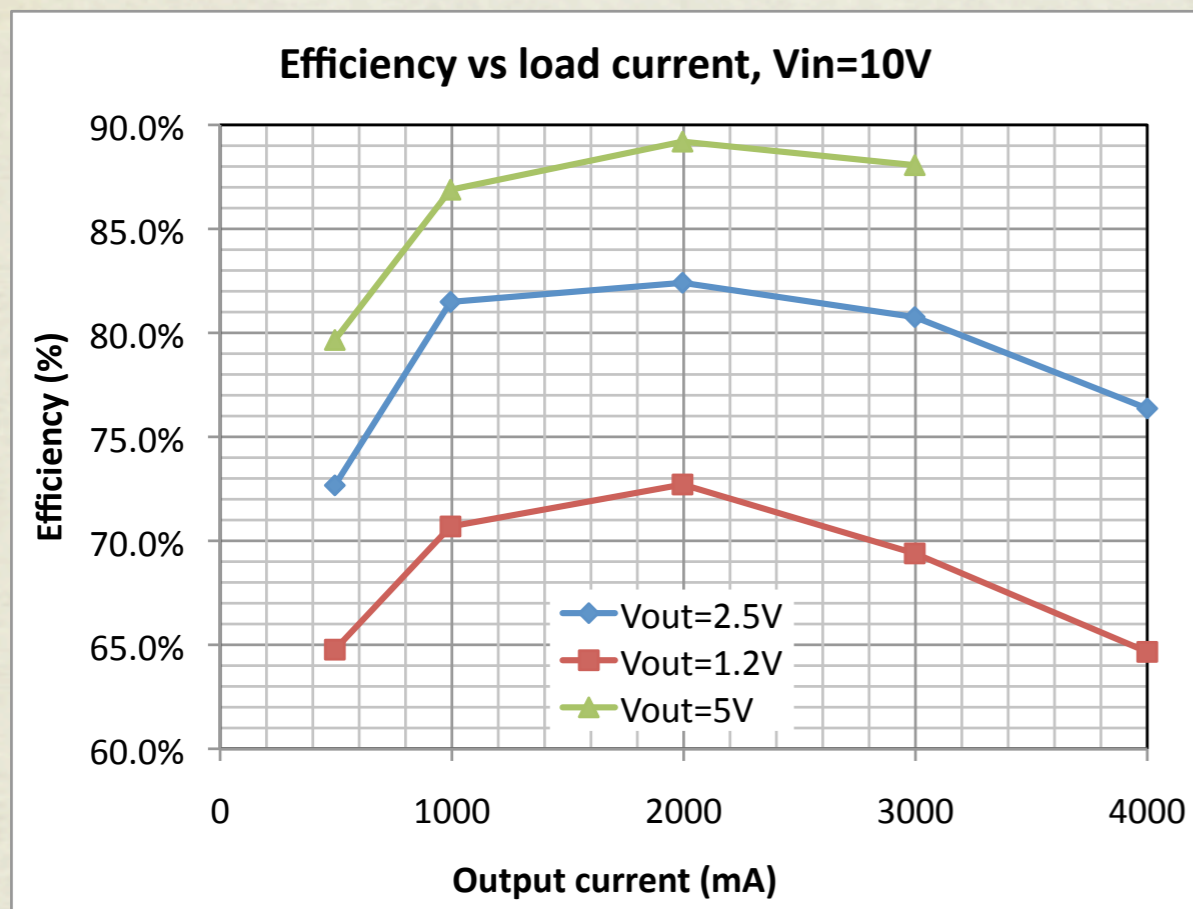
- ✓ 2.8x2.88mm size, packaged in plastic qfn32 (5x5mm)
- ✓ Switching frequency selectable 1-3MHz (selected to 1.8MHz in modules)
- ✓ Protection features:
 - Over-Current (OCP), Over-Temperature (OTP), Input Under-Voltage Lock-Out (UVLO)

- ✓ Accessible configuration pins:

- Enable (threshold $\approx 0.8V$)
- Power Good (open-drain, asserted if $V_{out} \approx$ nominal)
- Half_Switch (to increase efficiency for small load currents $\leq 700mA$)



EFFICIENCY

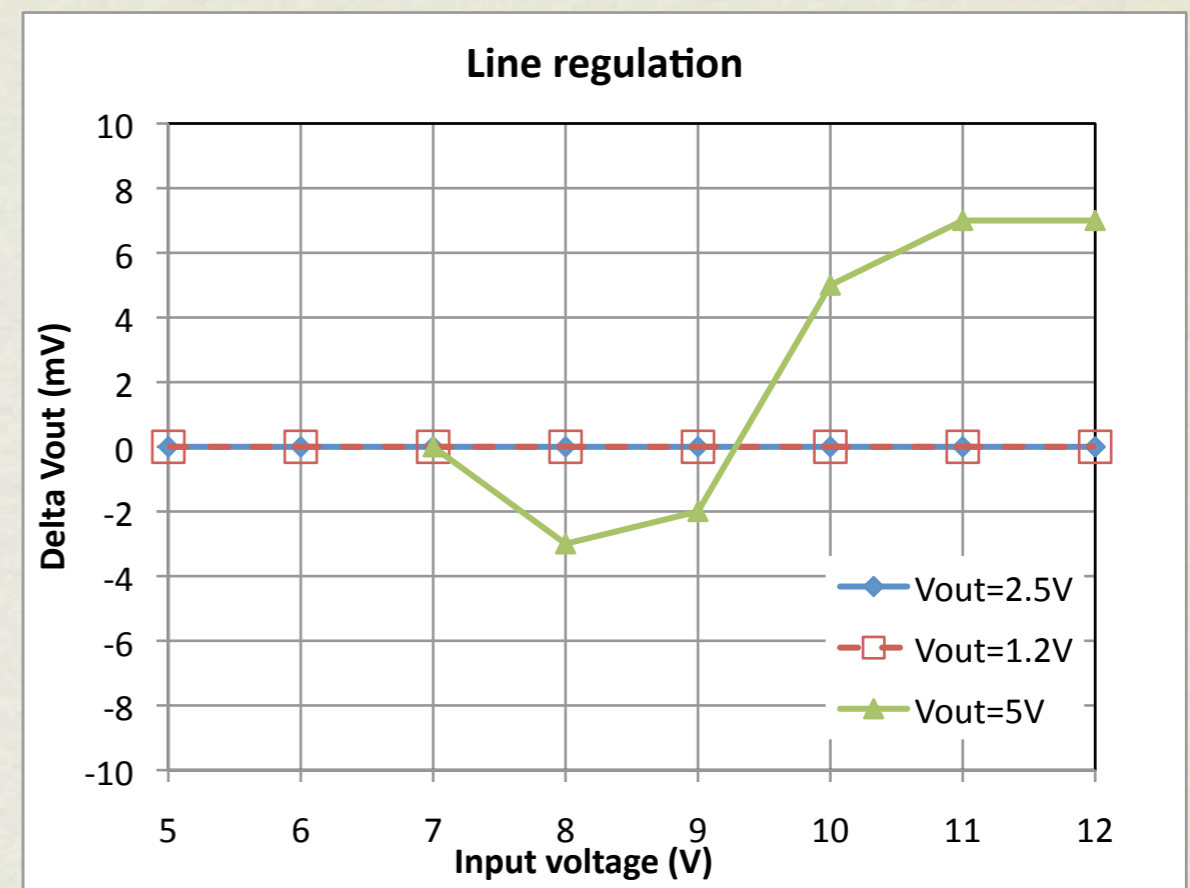
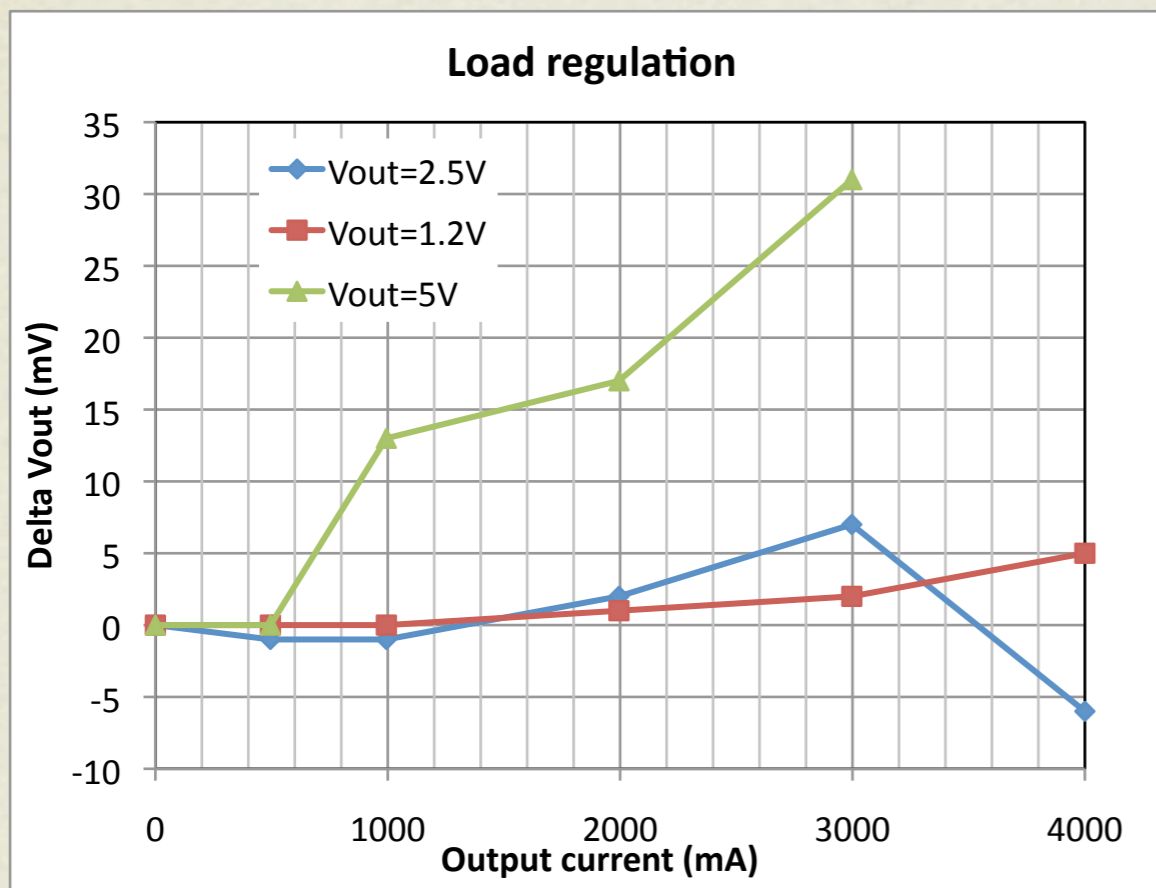


Conditions: cooling plate at about 18C, $L=430nH$ oval toroidal (bulk Cu wire), $f=1.8MHz$

REGULATION

Load regulation is the capability to maintain a constant output voltage level despite changes to the output current.

Line regulation is the capability to maintain a constant output voltage level despite changes to the input voltage level.

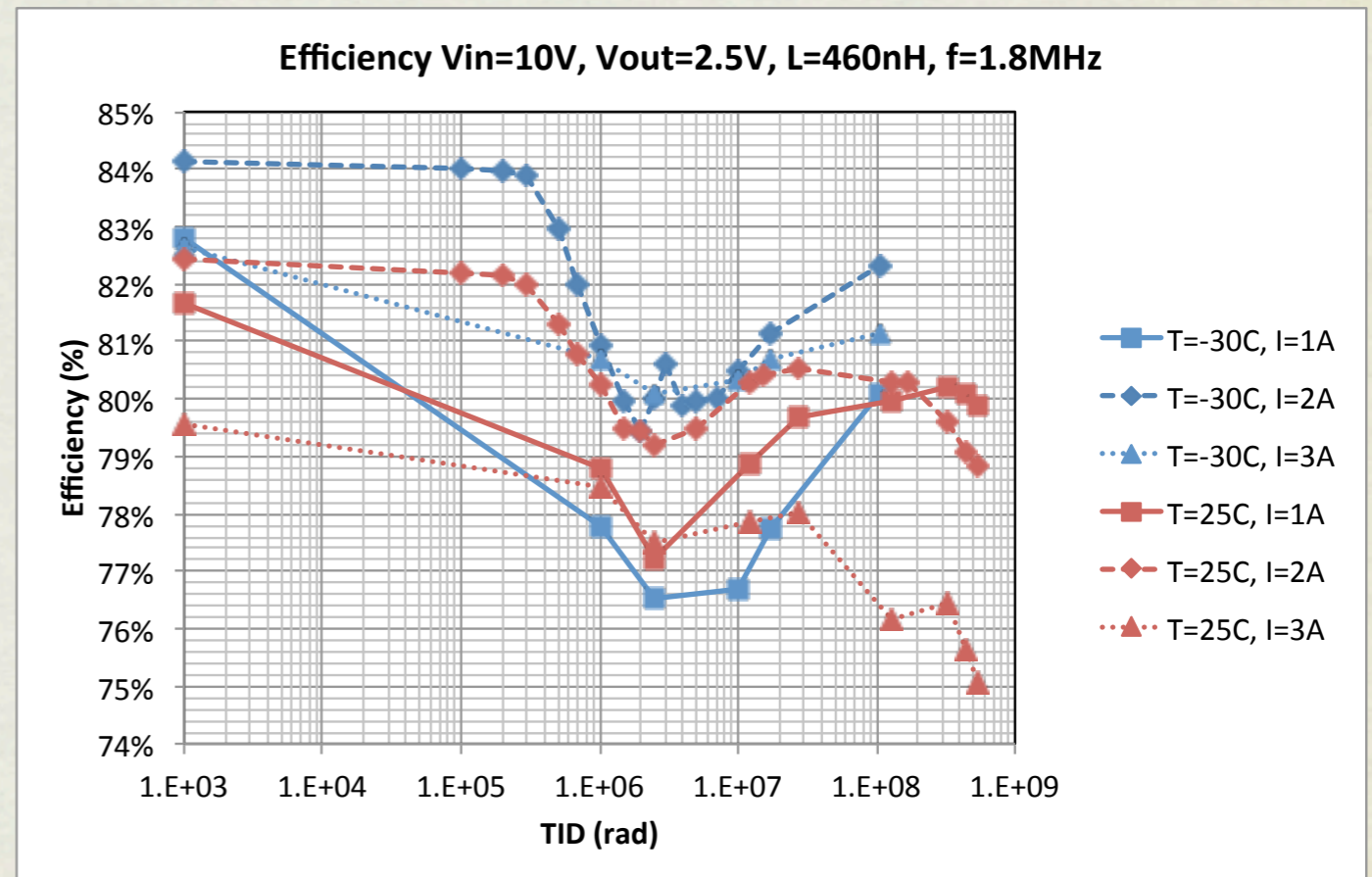


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f=1.8MHz

TID EFFECTS

- Irradiation performed at our X-ray irradiation system at controlled T (-30C, 25C) at a dose rate of 100krad/min
- Maximum TID reached: 547Mrad(SiO₂)

- Efficiency drop limited to a few % in quick irradiation (but with annealing it is expected to be practically negligible)
- Line and load regulation properties practically unaffected up to 100Mrad
- All safety features unaffected



DISPLACEMENT DAMAGE

- Displacement damage tests have been done on several previous prototypes in the same technology. The last one, AMIS5, is very similar to FEAST (the changes do not determine different radiation responses for displacement)
- AMIS5 is qualified up to $7e14$ n/cm² (1MeV-n equivalent)
 - After this fluence the HV PMOS pass-transistors of the linear regulators are excessively damaged
 - The linear regulators present in FEAST are exactly the same of AMIS5, therefore the performances of FEAST should be comparable
- Displacement damage test on FEAST is foreseen end 2013 - beginning 2014

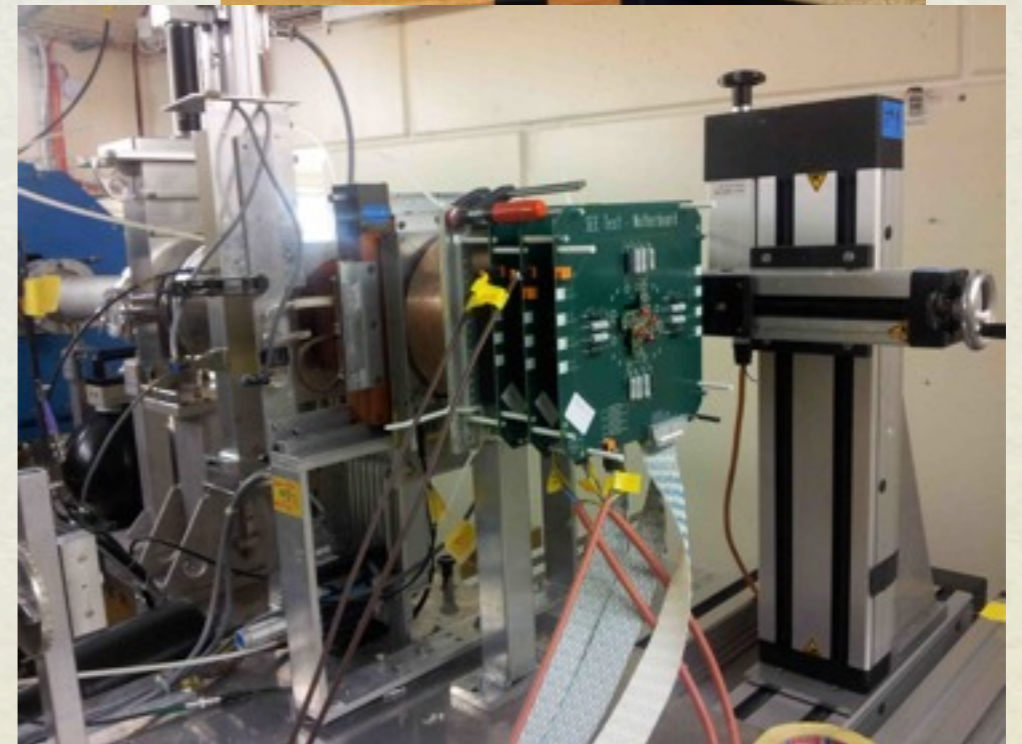
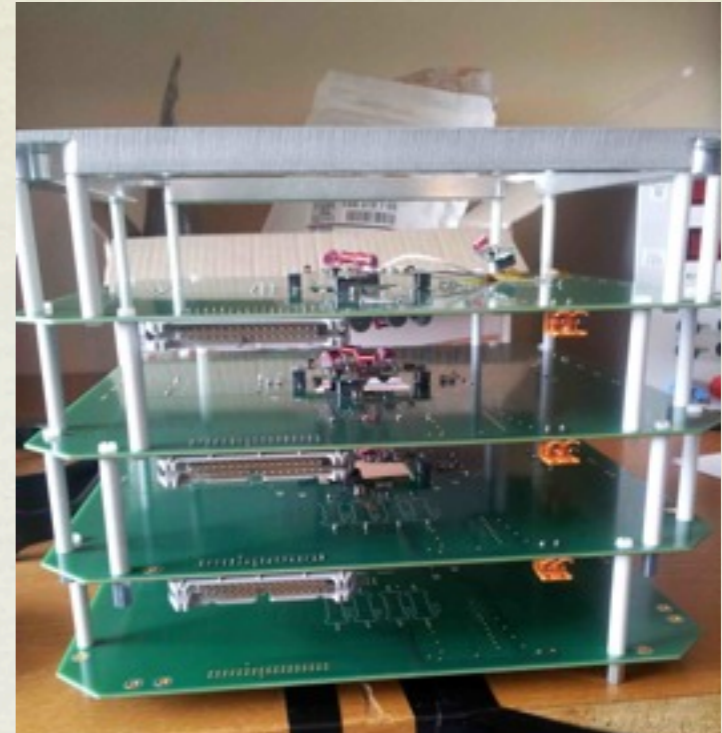
SEE

Measurements performed with different particle beams:

- Heavy Ions (CRC, Louvain-la-Neuve)
 - ✓ Results have been found NOT to be representative of our hadron-dominated radiation environment
 - ✓ However, they exclude the possibility of destructive SEEs (SEB) up to an LET of $30\text{MeV}\cdot\text{cm}^2\text{mg}^{-1}$ (even at 45degrees incidence)
- 230MeV protons (Paul Scherrer Institute, Villigen)
 - ✓ very representative of our environment

SEE: PROTONS AT PSI

- ✓ 23 DCDC on-beam for 36 hours at a flux $\sim 5E8 p \cdot cm^2 s^{-1}$
- ✓ Integrated fluence $\sim 5E13 p \cdot cm^2$ per DCDC
- ✓ 2 type of events happen in our environment:
 - ▶ short transients of V_{out} ($<2\mu s$, $<200mV$)
 - ▶ resets of the DCDC, where the converter goes into soft-start. V_{out} drops to gnd and gently rises to the nominal in 4-500 μs . The measured cross-section is $2-3E-13 cm^2$
 - In an environment with an integrated flux of hadrons (10 years) above 20MeV of $1E12 cm^{-2}$, the expected rate of reset is 2-3 every 10 DCDC over the full lifetime of the experiment



ASIC STATUS

- FEAST ASIC fully tested, including radiation effects. It is qualified for production
- 6 wafers have been produced (about 1300 chips/wafer)
- Packaging in qfn32 of 3 wafers is ongoing, parts expected at CERN in about 6 weeks

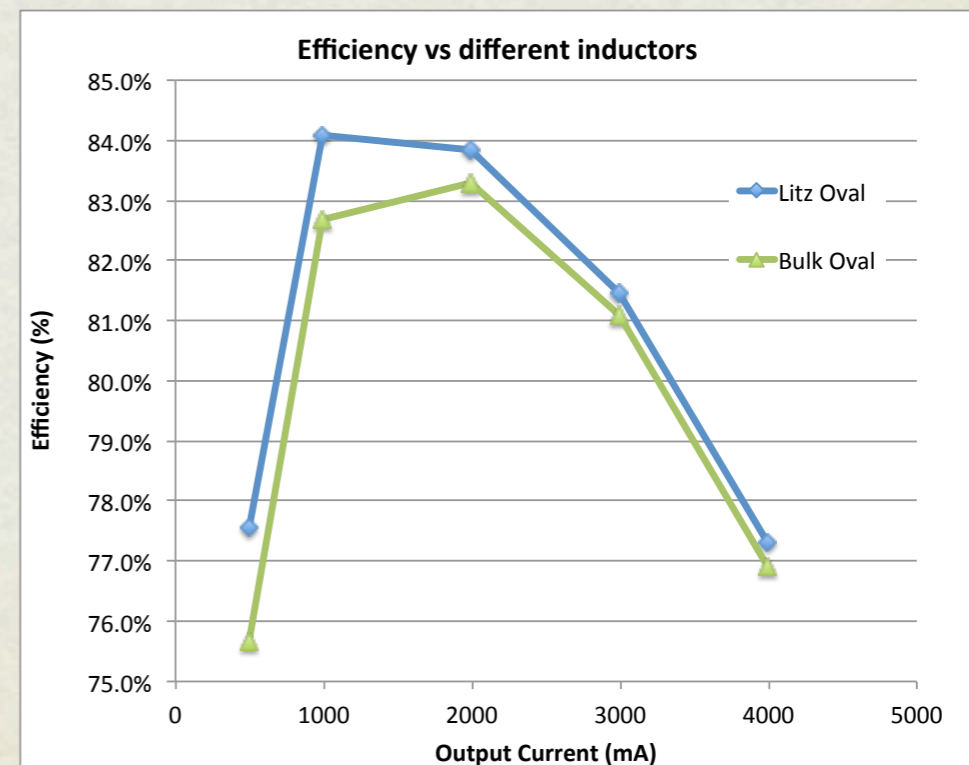


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	production-ready
ASIC	✓
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Connector	
PCB design	

CUSTOM INDUCTOR

- Best shape determined with 3-D simulations and trials. It minimizes radiated fields and optimizes efficiency
- Custom development made with Coilcraft
- $L=430\text{nH}$ as benchmark
- 2 different wires explored with Coilcraft:
 - ✓ bulk=copper wire with diameter $480\mu\text{m}$
 - ✓ litz=146 copper wires with diameter $\sim 40\mu\text{m}$
 - ✓ comparable DC resistance, but much lower AC resistance for the litz wire due to skin effect
 - ✓ However, cost considerably larger for the litz wire solution (due to much more complex construction of the terminals)
- Choice made: bulk Cu wire. Large production order about to be launched

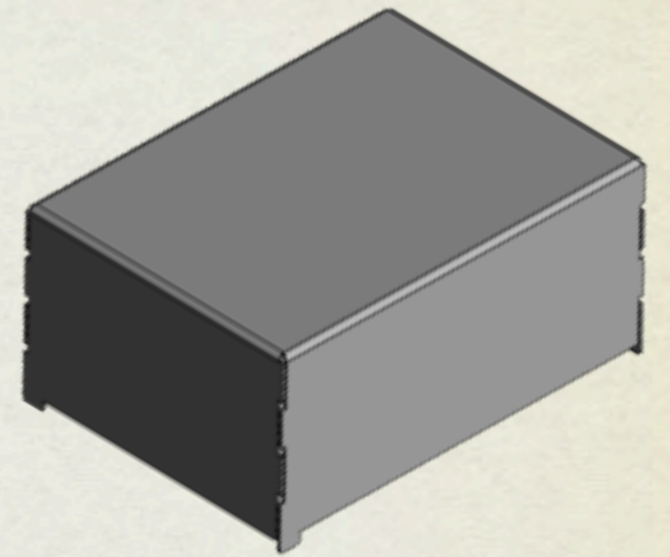


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SHIELD

- Totally commercial shield from Orbel company
 - ✓ 127 μ m thick bulk copper
 - ✓ Matte tin plating to avoid oxidation/corrosion
 - ✓ SMD component
 - ✓ Use of multi-louvered corners
 - ✓ Alignment pin to improve assembly
 - ✓ Small slots to deal with thermal expansion of the air inside the shield volume

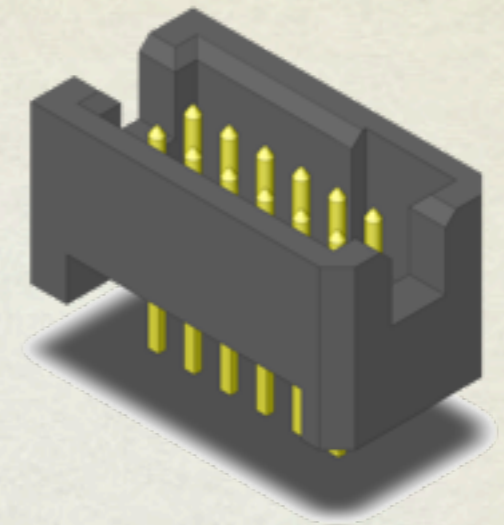


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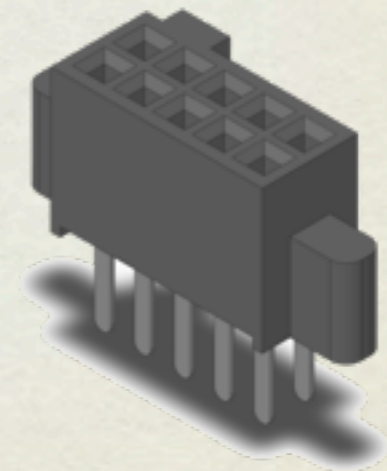
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CONNECTOR

- The connector chosen for our module is SAMTEC TFM-106-01-L-D:
 - ✓ Through-hole male connector
 - ✓ 12 pins
 - ✓ High current rating per contact (5A@20°C)
 - ✓ Shrouded body for blind mating
 - ✓ Classified as a ruggedized product by the manufacturer
 - ✓ Good quality/price compromise
- The female connector is the model SFM-106-01-L-D from the same manufacturer



TFM-106-01-L-D



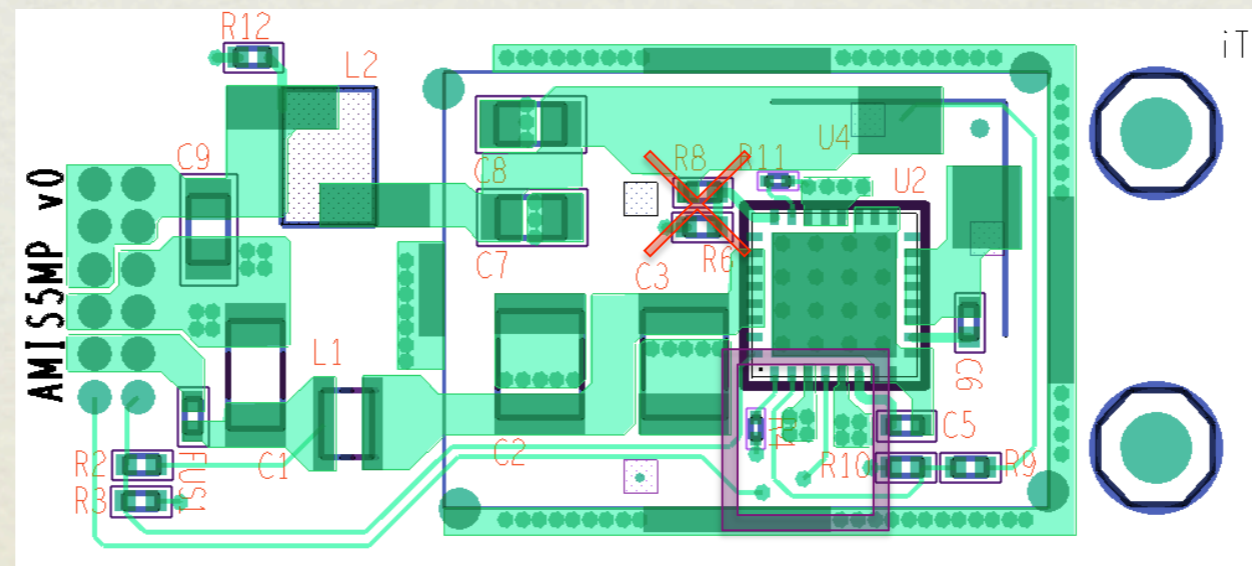
SFM-106-01-L-D

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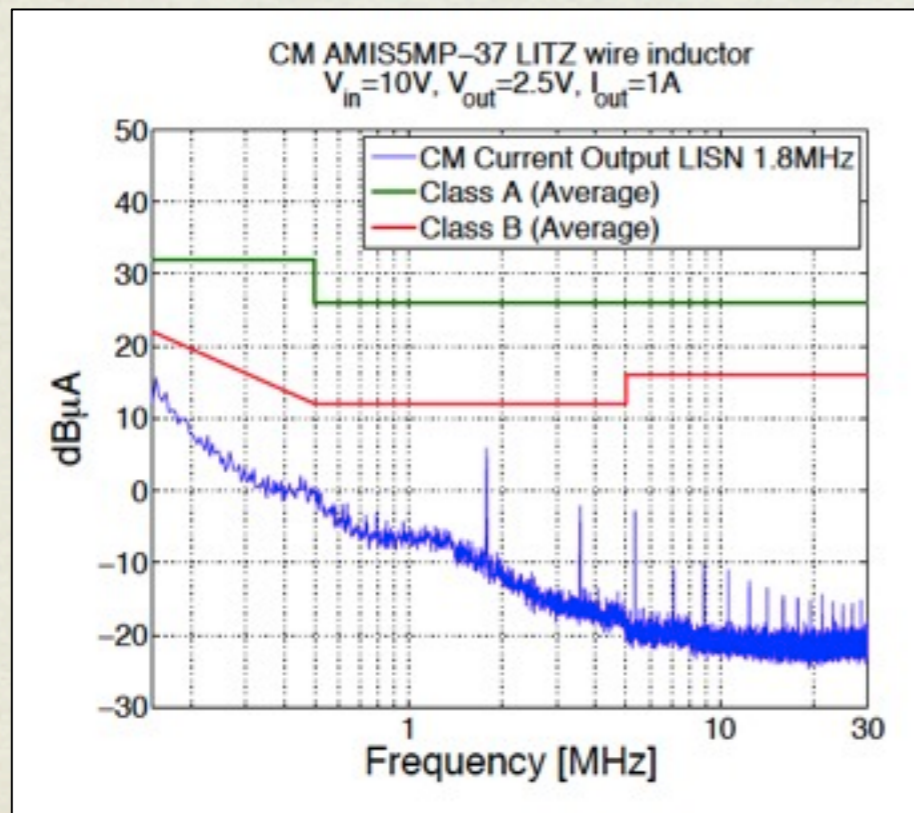
PCB AND PASSIVES

- The design of the PCB and the choice of the passives is the fruit of a long and systematic study within the R&D project (C.Fuentes, G.Blanchot, I.Troyano)
- The final design guarantees excellent noise performance and good streamline of the assembly steps - boards are fully assembled in Industry. Quality assurance can be improved that way.

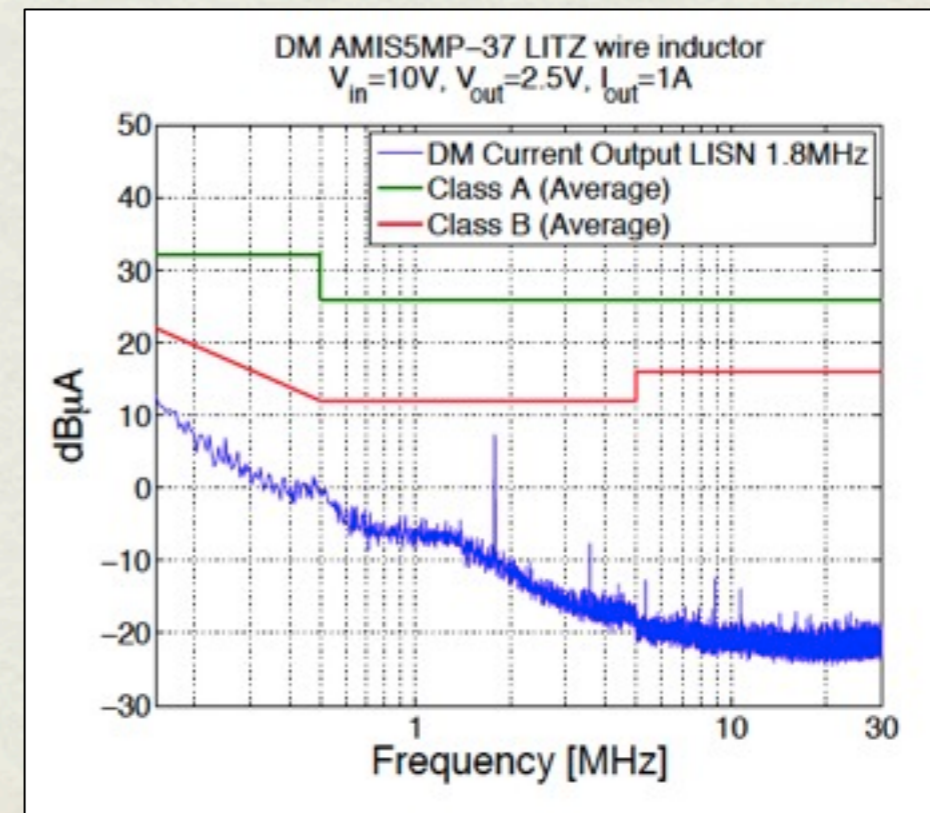


NOISE

Common mode output
conducted noise



Differential mode output
conducted noise

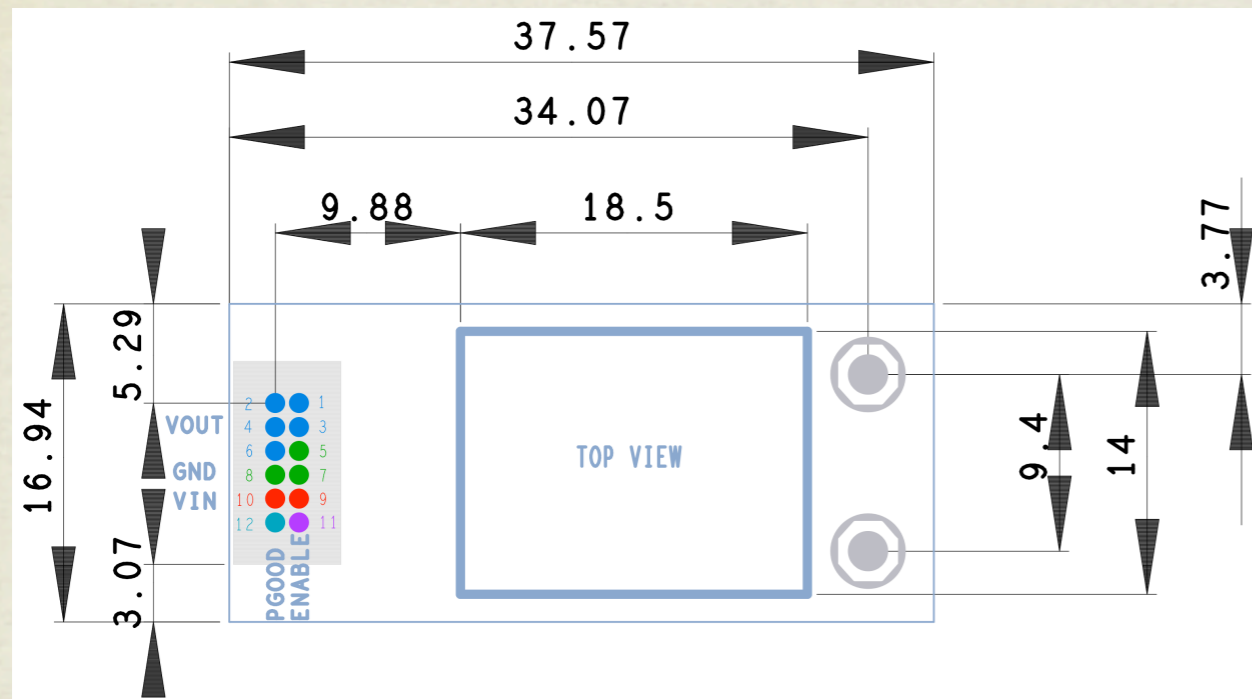


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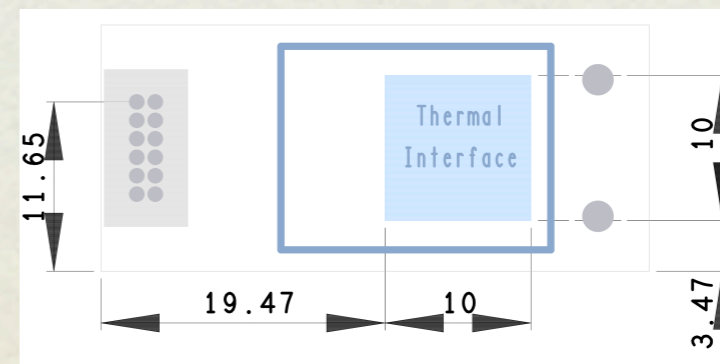
OVERALL DIMENSIONS

footprint



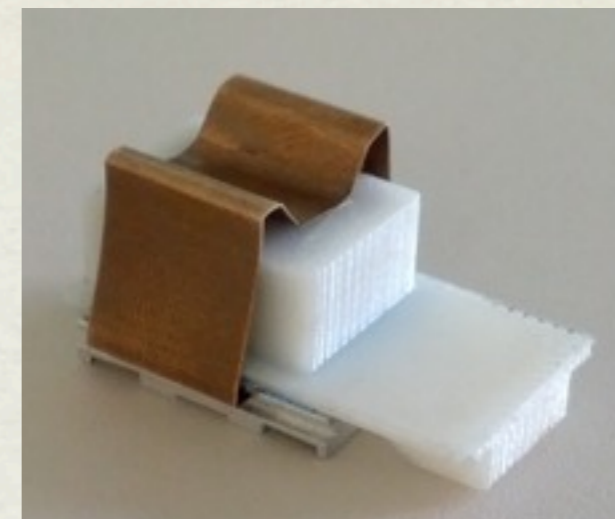
stack height:
mated connector ~6mm
pcb ~0.4mm
shield ~8.5
Total just short of 15mm

Thermal interface (required)



OPTIONAL MECHANICAL SUPPORT SUPPORT

- An optional mechanical support structure is being developed at CERN (PH-DT) to ensure easy and reliable attach of the converter module on a mother board
- Cooling should be ensured from the motherboard gnd plane or from the back of it (connection to the cooling system via a screw)



TIMELINE

- Today
 - ✓ We can distribute modules very representative of final ones, but still using the previous prototype ASIC (AMIS5) and hand-wrapped coils. These are available for 'positive' and 'negative' types (the negative has not been extensively tested so far)
- Procurement of all final components is on-going. We expect having all required parts before the end of 2013
 - ✓ A pre-production lot of about 200 parts will be launched at the beginning of 2014 (larger lot if requests are filed in advance)
- Reliability testing procedure has been developed and first measurements have been made (at the PH-DT QART Lab). A more complete qualification will be done on the pre-production lot (a full HAST is considered)

WHAT WE NEED FROM YOU

Experiments

DCDC stock

3.3V 2.5V 5V
testing

stock of components

CERN

coilcraft

orbel

farnell, ...

PCB manufacturer

Assembly house

Stocks are provisioned on the basis of your requests. It takes time for assembly and testing, so we need to know in advance (the earlier, the better):

- Number of parts required
- Vout
- Iout