



# MiniDAQ status



C.Abellan, **J.P. Cachemiche**, P.Y. Duval, F. Hachon  
M. Jevaud, R. Le Gac, F. Réthoré  
**Centre de Physique des Particules de Marseille**

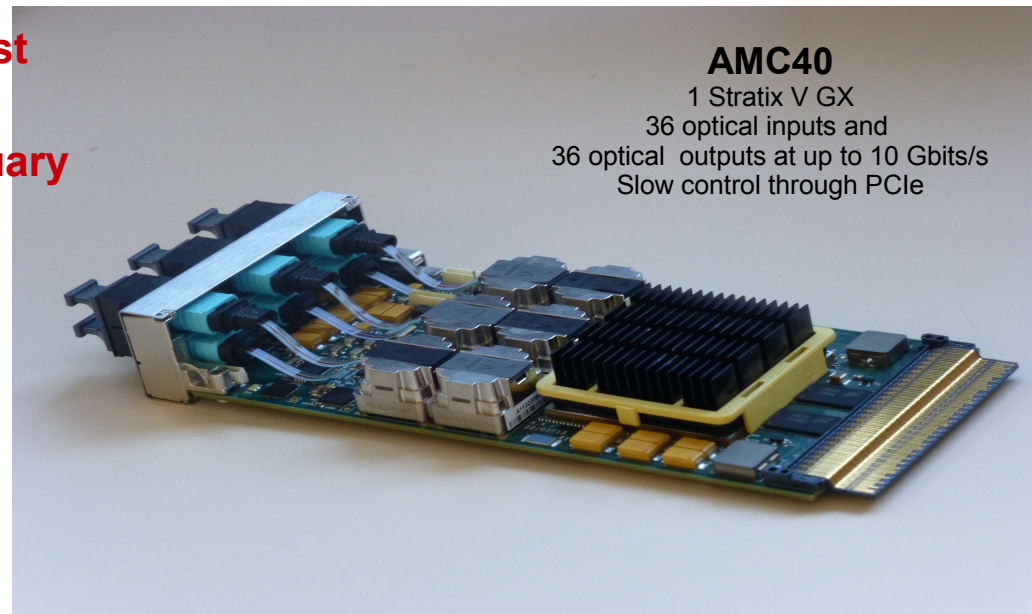
## Outline

- **AMC40\_V1 status**
- **MiniDAQ status**
- **Firmware status**
- **AMC40\_V2 status**

# AMC40\_V1 status

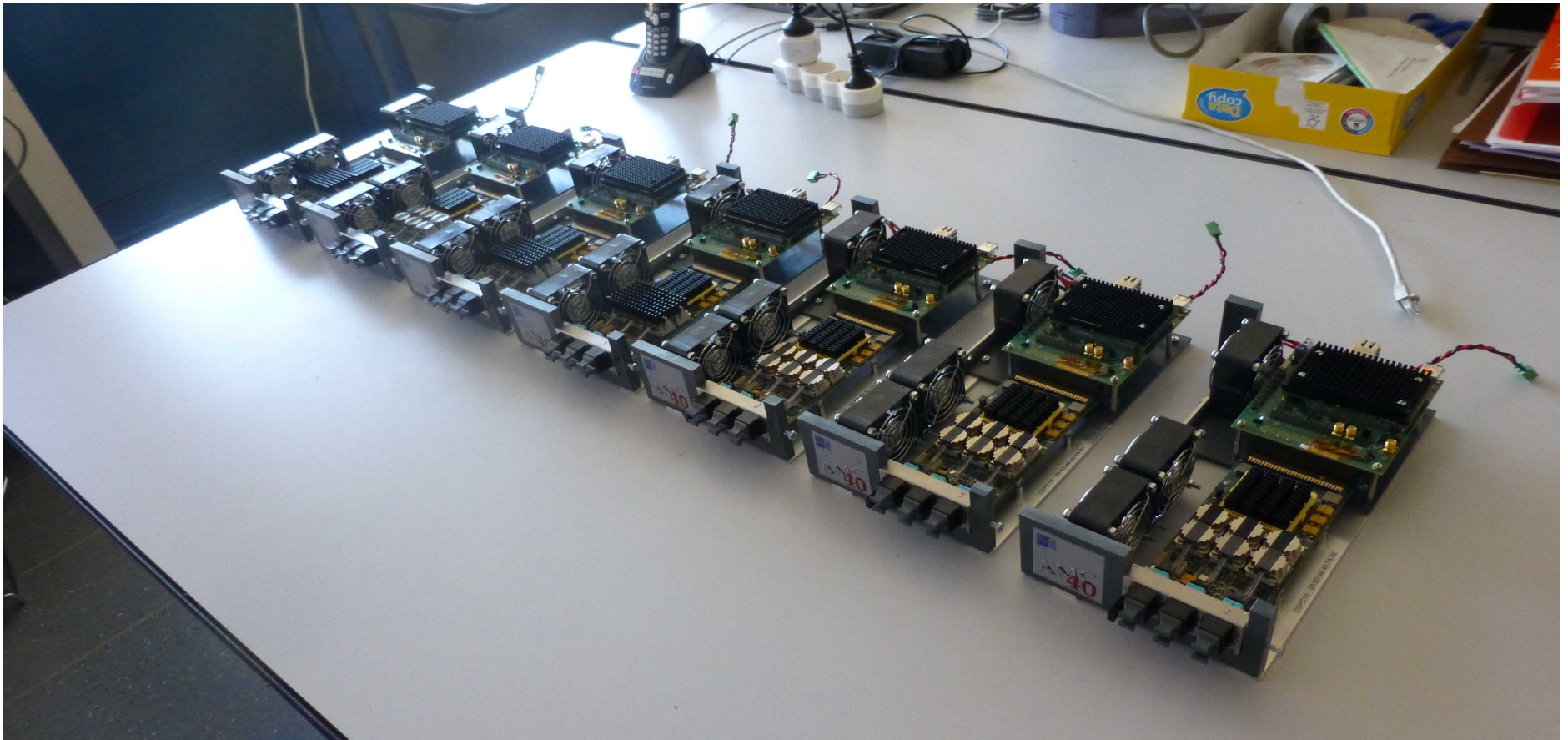
- Completely debugged including DDR3 memory
  - Works at 666 MHz (21 Gbits/s)
- However bug found on one bank
  - Rework needed to get the flip/flop functionality
  - **Opportunity to order new MiniDAQ setups for those who missed the first production**
  - **Orders to be received at last in January for a delivery by mid-2014**

Interface	ZUP	V	FUR
Rank 0			
DQS0			
DQ0			
DQ1			
DQ2			
DQ3			
DQ4			
DQ5			
DQ6			
DQ7			
DQS1			
DQ8			
DQ9			
DQ10			
DQ11			
DQ12			
DQ13			
DQ14			
DQ15			



# MiniDAQ status

7 MiniDAQ produced ... and available in Ken's office ! ... (Sorry Ken !)

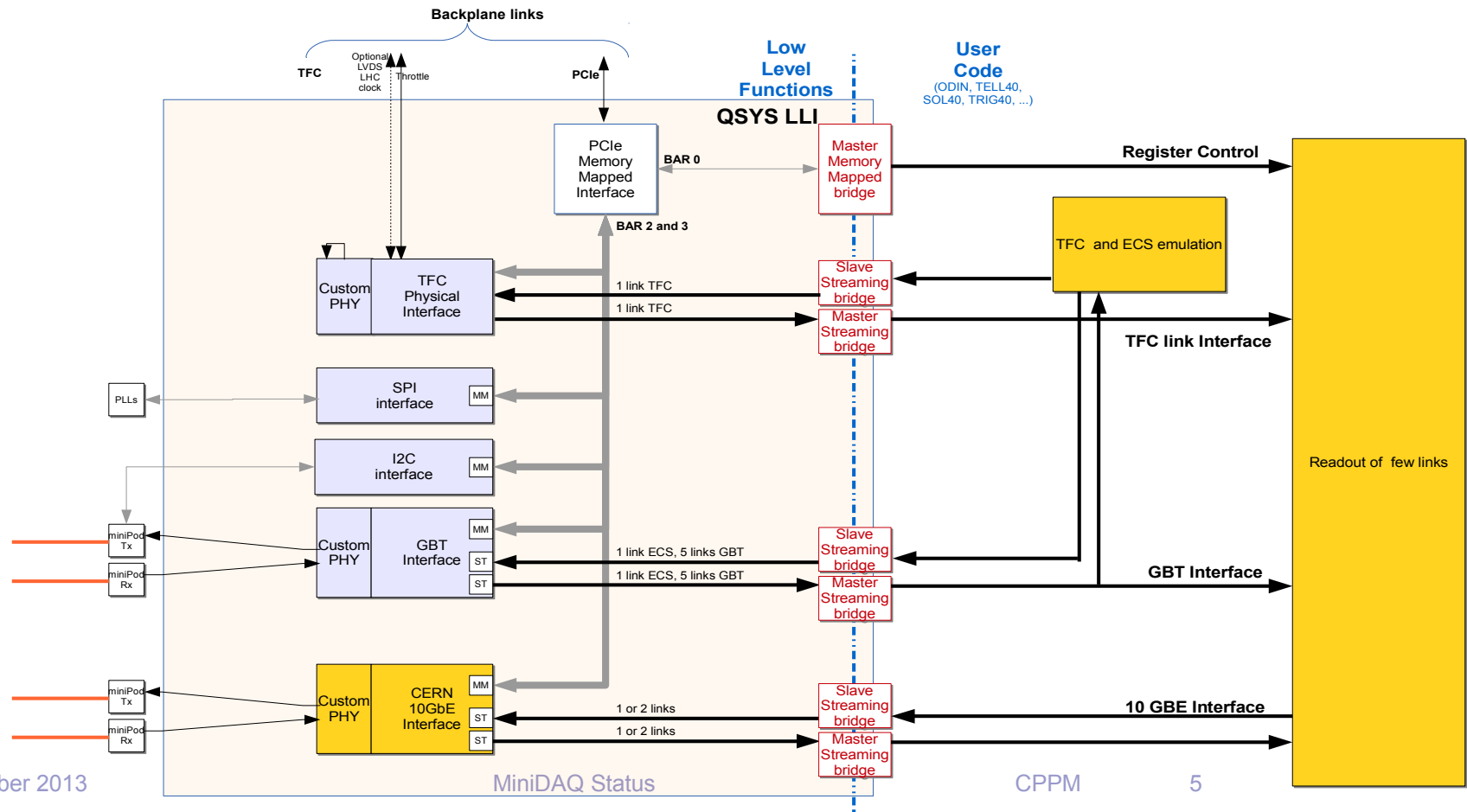


# Firmware status

## Minimum LLI in preparation

- Allows to handle 6 GBT links : 1 for ECS and 5 for ACQ and 1 or 2 ten GbE links

► *available by end of year*



# AMC40\_V2 status

## R&D continuation

## New features

- Full implementation of double buffering : 2 banks of 4 Gbytes of DDR3 (bandwidth = 102 Gbits/s par bank)
- Use of  $\mu$ Pods to free some room for DDR3
- PCIe GEN3 x 8 Interface over optics
- Powering tree optimization to decrease board consumption
  - Ongoing routing
  - board **manufactured** (not available!) by end of year



# Conclusion

MiniDAQ hardware for controlling FE ready

Still some firmware/software to integrate with Federico (TFC), Paolo (10 GbE) and Guillaume (Readout) for getting a friendly environment for users

Orders for MiniDAQ clones, if any, to be received before end of January

R&D continues : exploration and test of all available possibilities for the readout board

Will be eventually followed by a PCIe40 board in 2014

Efforts will be made to make firmware/software consistent among the different versions