FE questionnaire

This document is a questionnaire for Front-End (FE) developers on the FE data format which will be used in the sub-detector FE to send data to the Back-End (BE).
Since some studies have shown that the data format could have a lot of influence on the FPGA logic gates resources in the BE but also in the FE FPGA or ASIC, it's important to define precisely all the parameters about the data format for each sub-detector FE.

Here is some documentation to understand better the data format and his influence on the FE and BE FPGA (or ASIC for FE) logic gates resources. **Please read those documentations before answering the questions.**

- Data format documentation : https://lbredmine.cern.ch/documents/7
  You will find here all the information about the data format rules required between FE and BE.
- 2 talks about the influence of the FE data format on the FE and BE FPGA (or ASIC for FE) logic gates resources
  - Guillaume Vouters's talk : https://indico.cern.ch/getFile.py/access?contribId=1&sessionId=0&resId=0&materialId=slides&confId=254741
  - Federico Alessio's talk : https://indico.cern.ch/getFile.py/access?contribId=5&resId=1&materialId=slides&confId=225753

TO DEFINE:

Front End

- FE encoding data format
  - Manpower: who is in charge?
- Technology : ASIC or FPGA or both
- Data Format
  - Header **BCID** field width
  - Header **information** field width
  - Header **data_length** field width
  - unit value of Data Length
  - GBT width (80 or 112 bits)
    - If 112bits: error detection/correction/recovery system?
  - NZS possible?

    - max of data after one header for NZS and ZS for one fiber
    - Are data time-ordered by BCID?
- Data format compliant with the specs?
    - If not: why?
- Sync command integration and synch-frame definition
- What is the data latency? Is it fixed or variable?
- Will the front-end transmit frames containing non-valid-data that can be ignored by TELL40 ? How will these be flagged? (eg the dataValid input signal to the GBTX, which changes the GBT-frame header)
- What special running modes are required?
- Data emulation available?
- Estimated bandwidth (how many AMC40 and inputs links by AMC40)
- Estimation resources FE encoding for the ASIC or FPGA
- Bit ordering. See page 8 and 9 (section 1.b.) on the Data format documentation (https://lbredmine.cern.ch/documents/7) and tell which solution would be more convenient and why. Compare with how you will fill a GBT frame.
- Comments on the Data format documentation

Back End

- Data Processing
    - Generic or Specific
    - Manpower: who is in charge?
- Status
- What output interface would you need for the data processing block and which frequency?
- DSP block for the data processing needed?