VELO UPGRADE FIRMWARE

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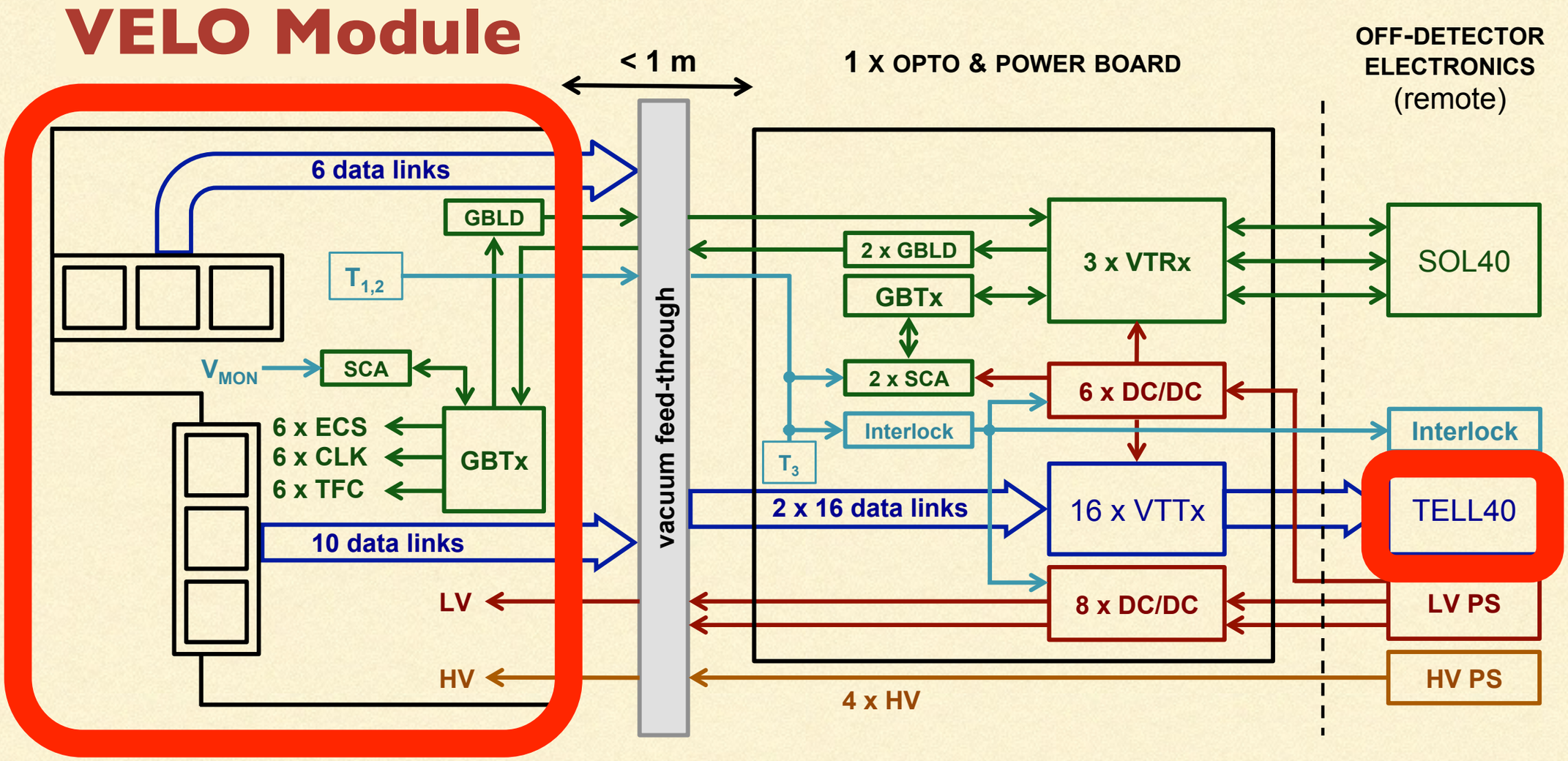
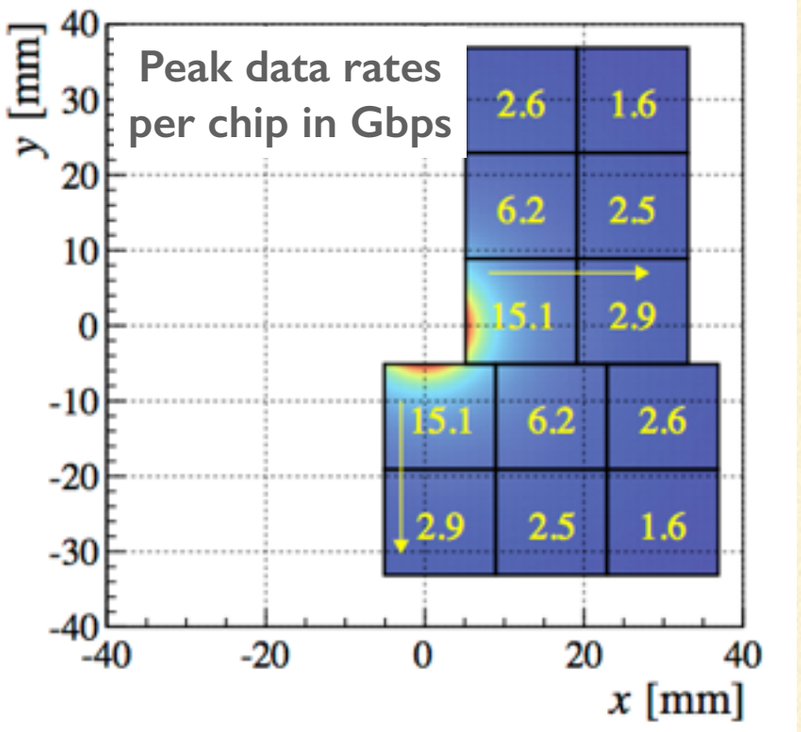
VELO DAQ

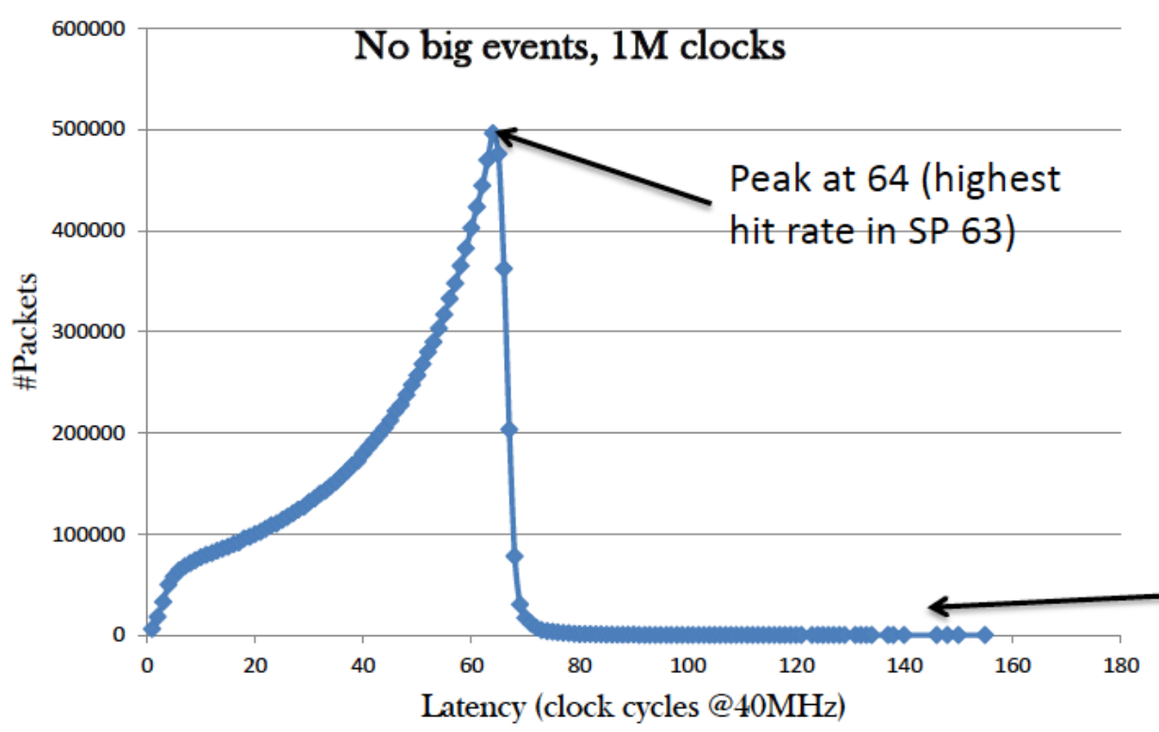


- Installed bandwidth = 32 GWT links @ 5.12 Gbps = 163.8 Gbps
- Required Peak rate = 61.2 Gbps
- Considering reducing to 20 GWT links => 102.4 Gbps installed bandwidth (cannot reduce further)

VELOPIX

- 256x256 pixel ASIC
  - 12 chips per VELO module
- Data driven readout
  - data arrives "out-of-time"
- Preferred option is to use Gigabit Wireline Transceiver (GWT) serialisers rather than GBT.
  - Main advantage is much lower power consumption by the serialisers in the ASIC
  - Slightly higher bandwidth - 19.2 vs. 17.9 Gbps.



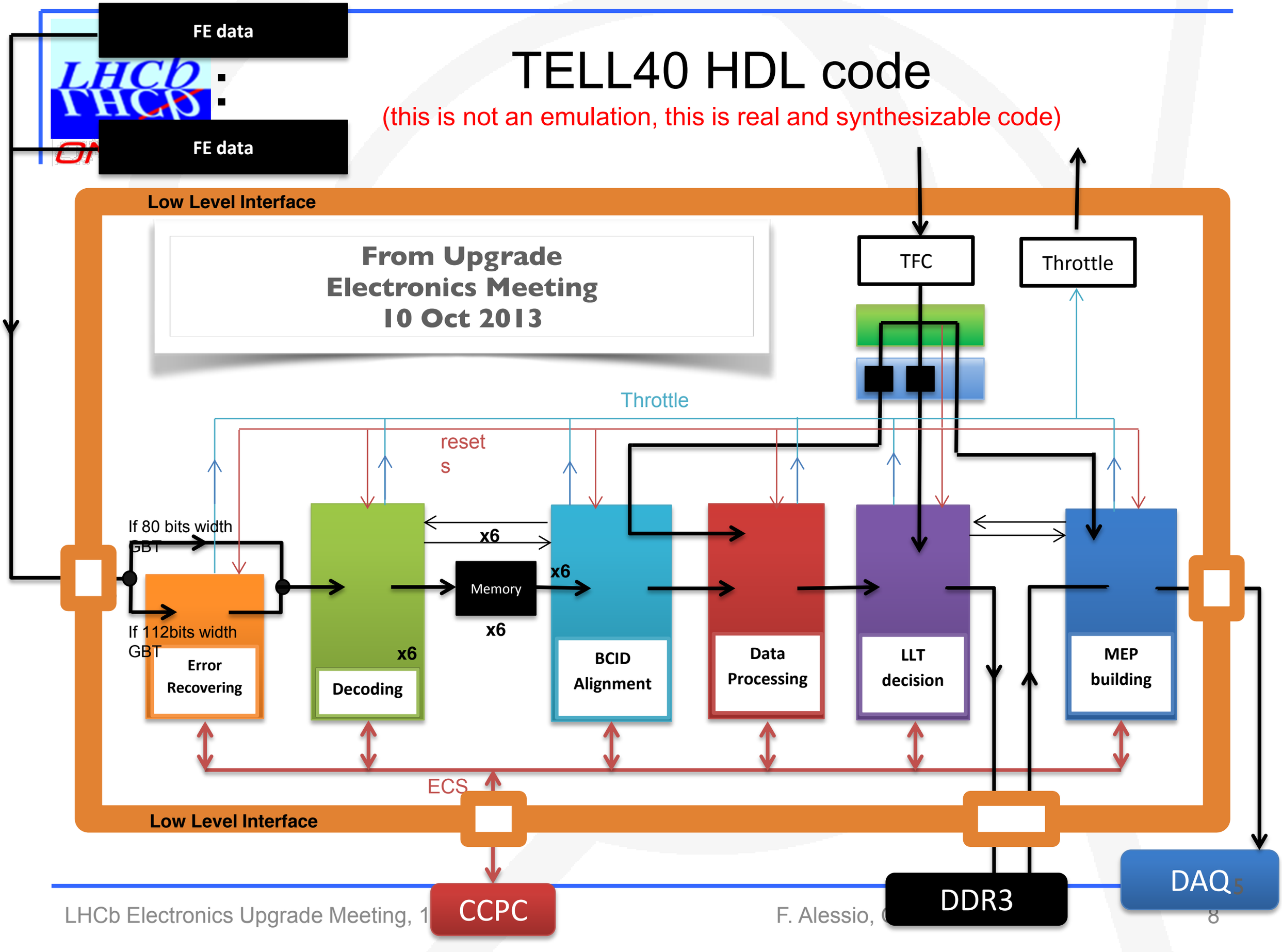


VELO FIRMWARE

- Main challenge - time ordering data whilst coping with high input rate from hottest chips.
- Two critical items to ascertain the firmware resource utilisation
  - GWT decoding - similar to GBT decoding?
  - Time (BCID) ordering
- Independent development of VELO specific firmware elements to assess resource utilisation

TELL40 HDL code

(this is not an emulation, this is real and synthesizable code)



TELL40 HDL code

(this is not an emulation, this is real and synthesizable code)

FE data

FE data

Low Level Interface

From Upgrade Electronics Meeting 10 Oct 2013

TFC

Throttle

Throttle

reset

s

Marco

Pablo

If 80 bits width GBT

If 112bits width GBT

Error Recovering

Decoding

x6

x6

Memory

x6

x6

BCID Alignment

Data Processing

LLT decision

MEP building

LLI +GWT decoder

BCID Alignment

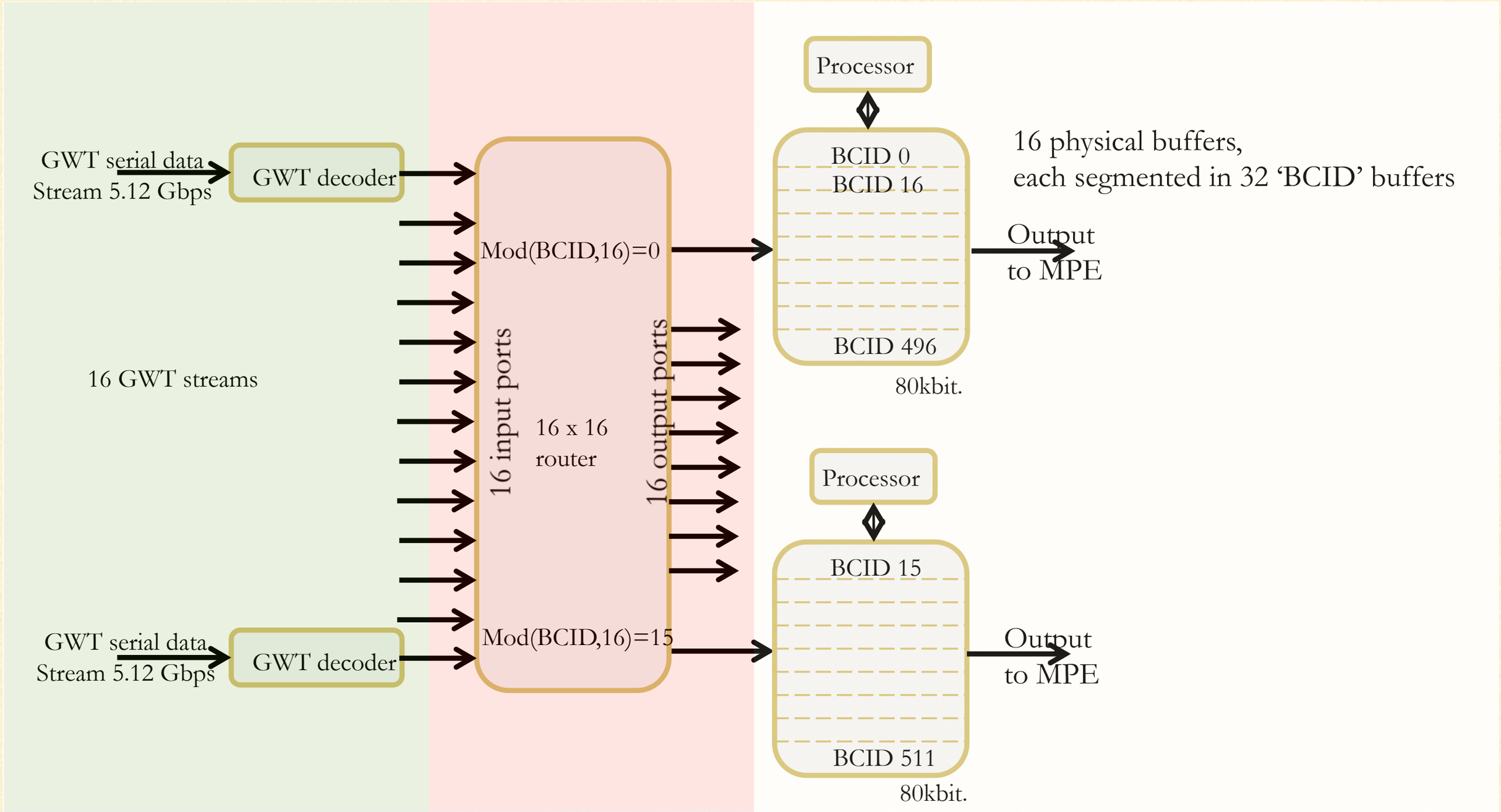
ECS

CCPC

DDR3

DAQ 6

VELO FIRMWARE BLOCKS



PROTOTYPING PLAN

- Stage 0
  - Prepare a first version of VELO-only firmware and examine resource utilisation and simulation performance.
- Stage 1
  - First prototype board should run first version of firmware integrated with LLI
  - find bugs not found by simulation
  - Develop a front-end emulator that runs on a similar/same chip
- Stage 2
  - Approach a final version of firmware

BACKUP

LINK SCHEME & DATA FORMAT

- Evaluating half- or full-module per FPGA (depends on resources)
  - Half module (TDR) - 16 readout links per FPGA
  - Full module - 20 readout links (removing redundant links from low occupancy VeloPix ASICs)
- Fixed length (30 bit) and fixed position VeloPix packets from 128 bit GWT words (instead of 120 bit GBT)