The LHCb Muon architecture upgrade review: a summary

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on behalf of

The LHCb Muon Upgrade Group

Summary

- The review was held at CERN on Oct. 9th
- Reviewers: Ken Wyllie, Federico Alessio, Jan Buytaert
- Very constructive meeting, lot of questions asked/answered
- Received reviewers' comments on Nov. 5th , provided feedback on Nov. 13th
- "Procedure" completed (milestone)

The Muon System Upgrade in brief

- Phase 1: get ready for the 40 MHz readout
  - Muon detector will not be modified, but M1 will be removed
  - nODE (with nSYNC ASIC) for an efficient detector readout by TELL40
  - Muon LLT Low level trigger (LLT) implemented on muon system TELL40
  - nPDM and nSB for an efficient chamber pulsing and control using GBT through GBT-SCA
  - Ready @ LS2
- Phase 2: new high readout granularity detectors for high-luminosity regions equipped with a new highly-integrated FEE ASIC
  - Baseline planning: new detectors and electronics prototypes ready @LS2, then construction, to be installed @ LS3
  - This will is not part of this review and will not be discussed today

Review's Outline

1. The new readout architecture and its implementation with the nODE board [S. Cadeddu, P. Ciambrone]
2. The nSYNC ASIC [S. Cadeddu]
3. The Muon Detector specific part of the TELL40 firmware [E. Santovetti]
4. The new control and pulsing systems for the Muon Detector [V. Bocci]
5. Project Schedule, manpower and responsibilities [A. Cardini]

The Muon detector

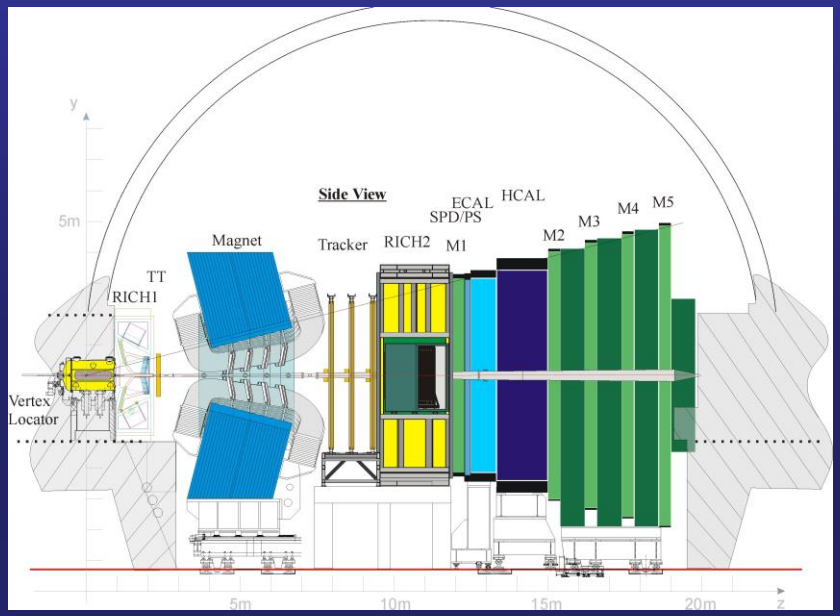
Crucial role in the first Trigger level (L0 Muon trigger)

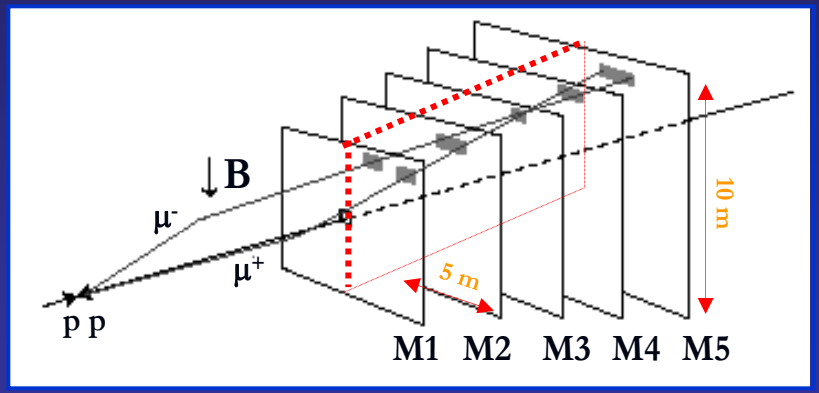
Provide an high PT muon trigger at the L0 with the 95% efficiency

5 Stations: 1380 detectors (MWPC & 3-GEM)
- 20 different types of detectors, with different time response
- Different dimensions: M1 (24x20cm2), M5 (151x31cm2)

120k Front-end channels combined to have 26k read-out channels
- Space point binary information within the bunch crossing
- Phase inside the bunch crossing

About 50,000 LVDS signal cables of different length

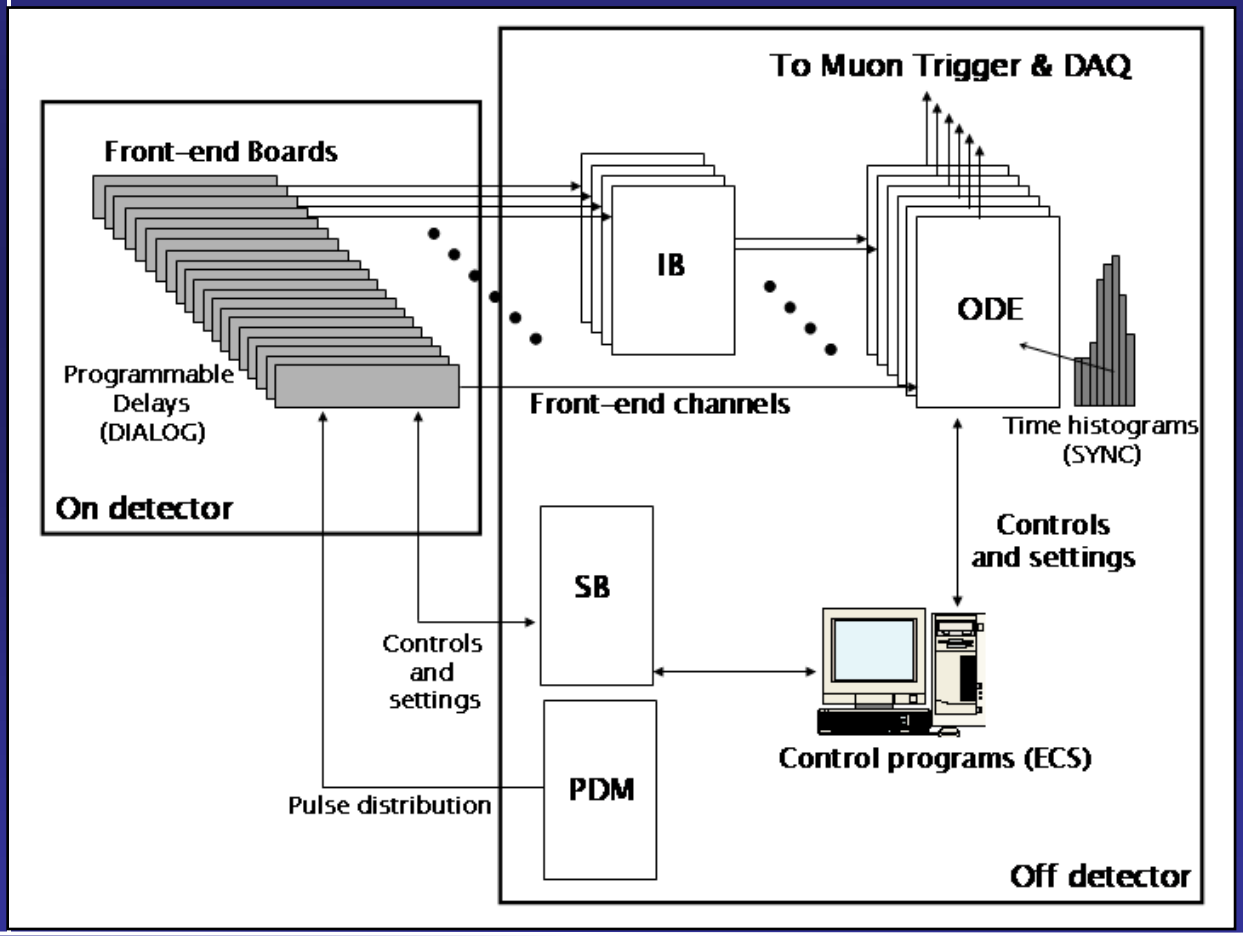




Muon Detector: the Read-out system

7632 Front End boards (CARDIAC):
Two ASIC:
CARIOCA (ASD chip)
DIALOG (time alignment and monitoring)

168 IB (Intermediate Boards) make a logical combination of the front-end channels (~122k) to obtain the read-out channels (~26k)



14 Tell1 of Muon DAQ acquire the data after the L0 yes

152 ODE:
Synchronous with LHC Clock.
Collect data from FE and send it to L0μ trigger and to DAQ.
24 SYNC ASIC:
- Measure of time
- BXid association
- L0 pipelines

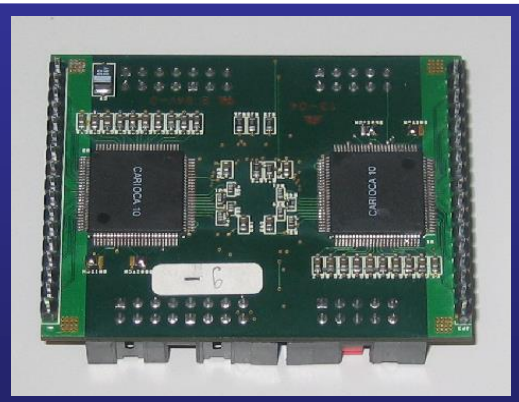
Electronic Chain: 10÷21 m of LVDS cables

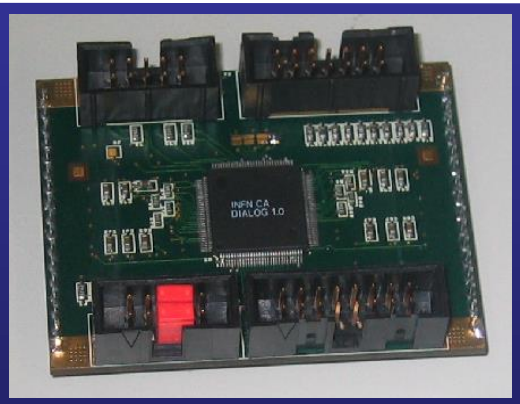
156 SB (Service Boards): Control the Front-End Boards

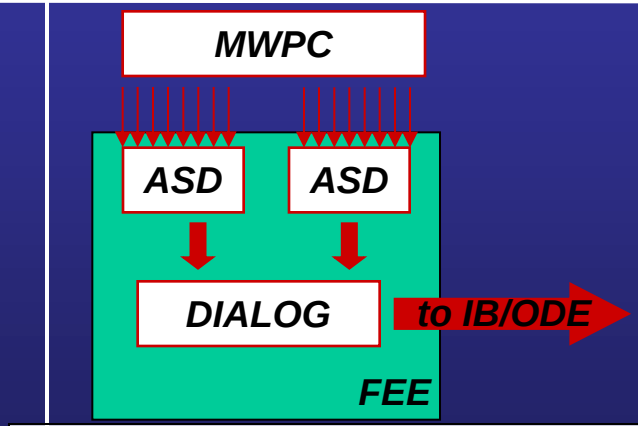
10 PDM:
Pulse the FEB synchronously to a given BXid

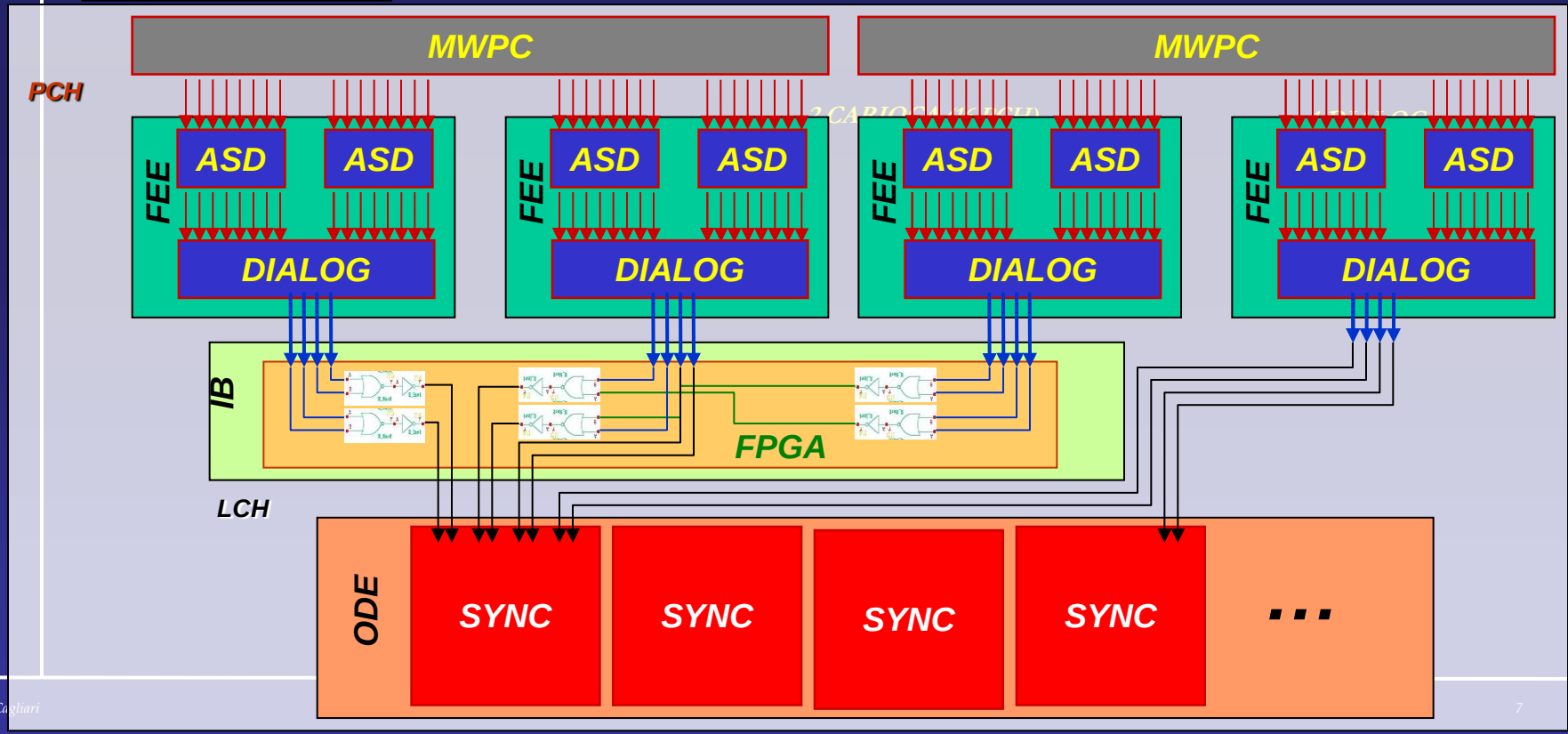
All boards are controlled through ECS-PVSS

The Front-End Electronics and its connectivity



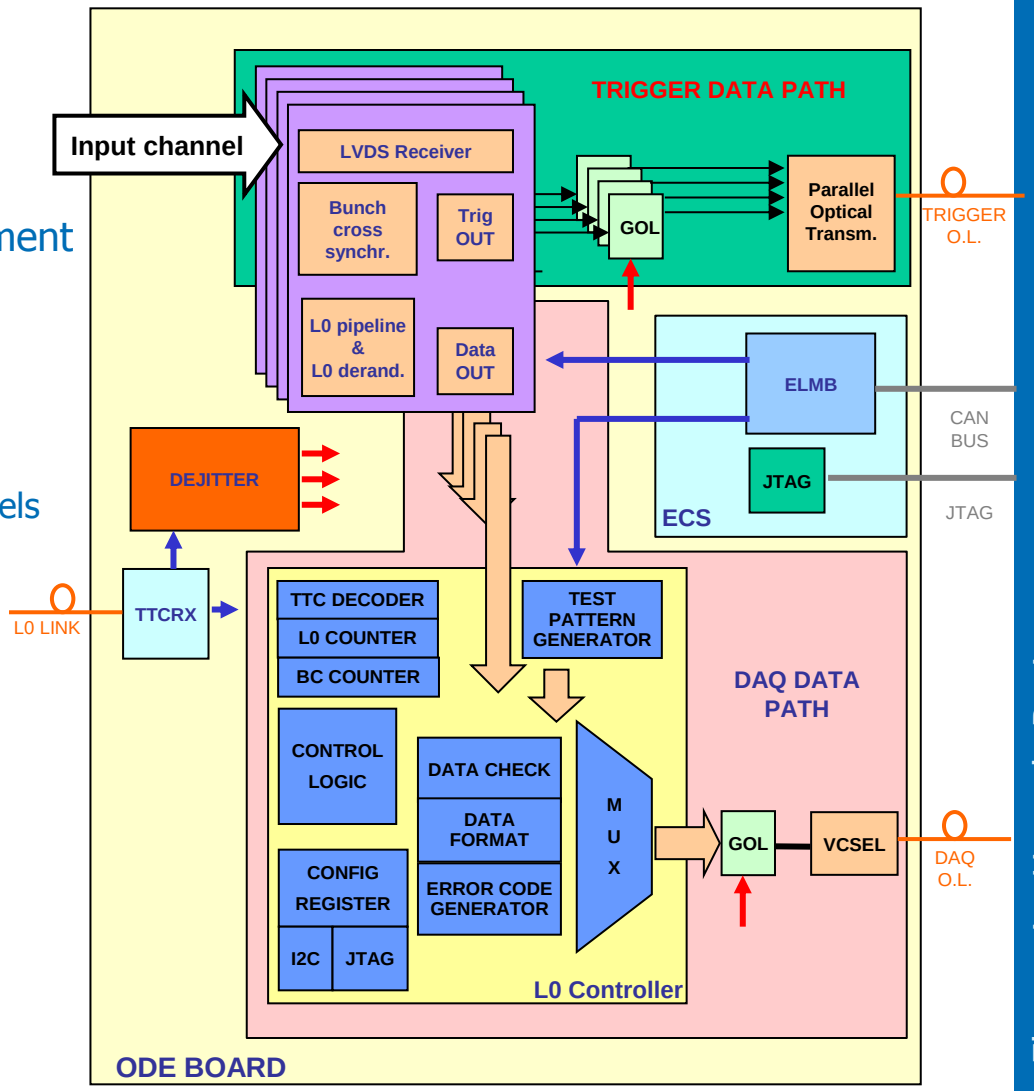






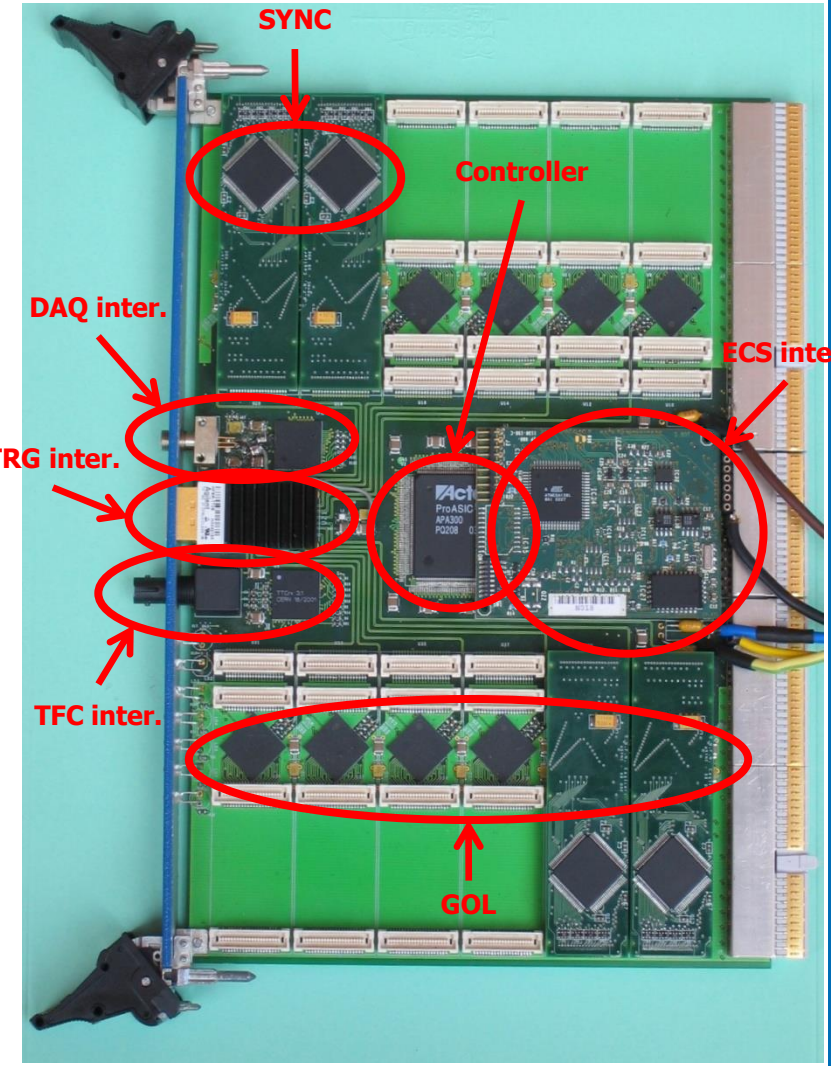
Present ODE architecture

- L0 front-end electronics stage
  - Clock synchronization and Bx alignment
  - Time measurements
  - L0 pipelining and buffering
- TFC system interface and clock management
  - Master LHCb clock
  - L0 trigger and reset signals
  - Clock de-jitter and distribution
- L0 trigger interface
  - Trigger Unit production from logical channels
  - Data transmission @ 40 MHz
- L1 DAQ interface
  - TDC Data formatting
  - Data transmission @ 1 MHz
- L0 board controller
  - TFC commands decoder
  - Interfaces controller
  - Test facilities and diagnostic
- ECS interface
  - Initialization, monitor and debug



Present ODE implementation

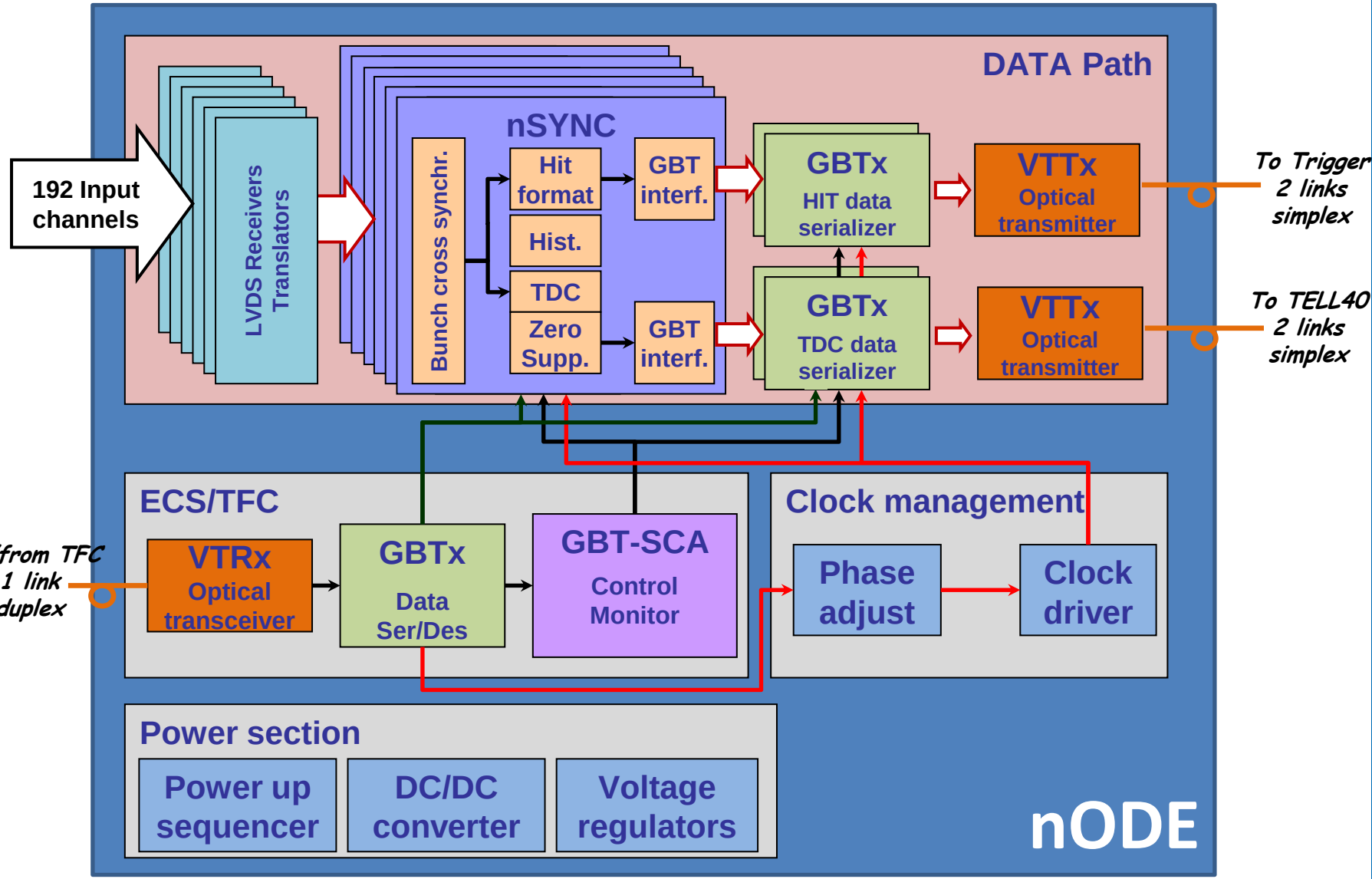
- L0 front-end electronics stage
  - 192 LVDS input signals
  - 24 SYNC chips (on 3 types of piggy board)
- TFC system interface and clock management
  - 1 optical receiver + 1 TTCrx chip
  - 1 QPLL chip
  - Tree network based on MC100LVEP family
- L0 trigger interface
  - 12 GOL chips + 1 parallel optical transmitter
  - Valid data transmission @40MHz
- L1 DAQ interface
  - 1 GOL chip + 1 VCSel diode
  - Valid data transmission @1 MHz
- FPGA board controller
  - Flash RAM based Actel FPGA (ProAsicPlus)
  - 3 buses (32 bit) for SYNC and GOL interfaces
- ECS interface
  - 1 ELMB board
    - CANbus link on the backplane
    - 2 I2C internal buses
- 6U Compact PCI card
  - 10 layers motherboard with controlled impedance
  - Mixed 5/3.3/2.5 V devices



Present architecture remarks

- Obsolescence of components could be an issue
- No flexibility to match feature run conditions (occupancy, granularity, …)
- The 4 bit TDC information is extremely (absolutely) useful to monitor and fine tune the time alignment of the Muon Stations
  - This information is sent from ODE boards to the Muon TELL1 via GOL
    - @ max 1 MHz (~900 ns are needed to read-back the complete event from all SYNC chips)
    - the events are selected by the L0yes, received via the TTCrx from TFC system
    - no zero suppression implementation is possible
- Need to maintain (emulate) the present TFC system
  - Master clock, synchronization signals, L0 trigger
- Need to maintain the present ECS system

nODE architecture



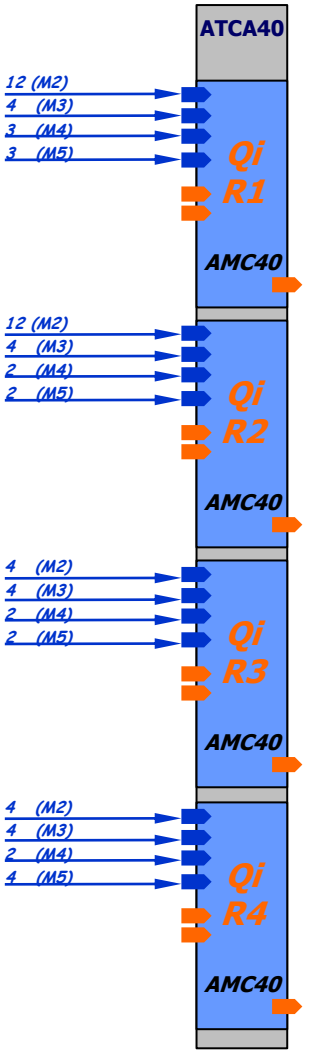
TELL40 x HIT info

- The number of O.L. for each region of a quadrant (4 stations) is compatible with AMC40 inputs
  - max 22 links in R1

	O.L per quadrant				
Region	M2	M3	M4	M5	tot
R1	12	4	3	3	22
R2	12	4	2	2	20
R3	4	4	2	2	12
R4	4	4	2	4	14

- If the resources of each AMC40 and/or ATCA40 were enough, 1 TELL 40 could elaborate the data of a entire quadrant
  - 4 TELL40 in total for the MUON hit (and LLT)

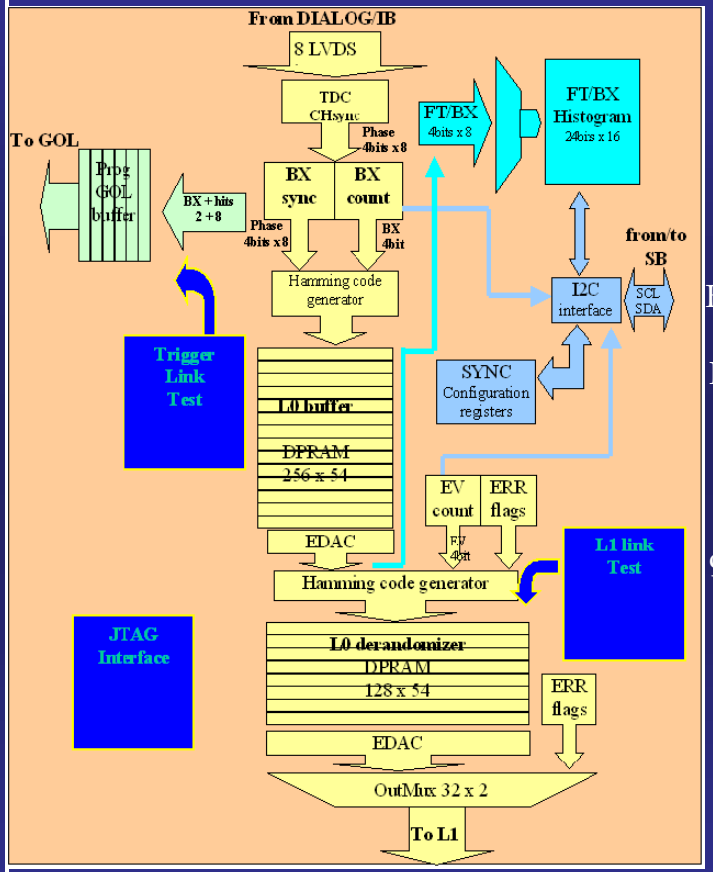
Same requirements for TDC links



Summary

- A new boards (nODE) almost "plug & play" with current ODEs is foreseen
  - No re-cabling
  - Use a new custom ASIC (nSYNC) to integrate all the required functionalities
  - Use new GBT and versatile link components to implement trigger, DAQ, TFC and ECS interfaces
    - Separate links for trigger and DAQ data
    - Reduced number of links to the L0 Muon trigger
      - 2 links per board
      - GBTx in Wide bus mode
    - Read TDC data @ 40 MHz rate
      - 2 links per board
      - GBTx in Wide bus mode
  - Discharge present TFC and ECS systems
  - Enough flexibility to reduce channel occupancy
  - Present power system compatible with minimal maraton re-configuration

SYNC 1.0 vs nSYNC



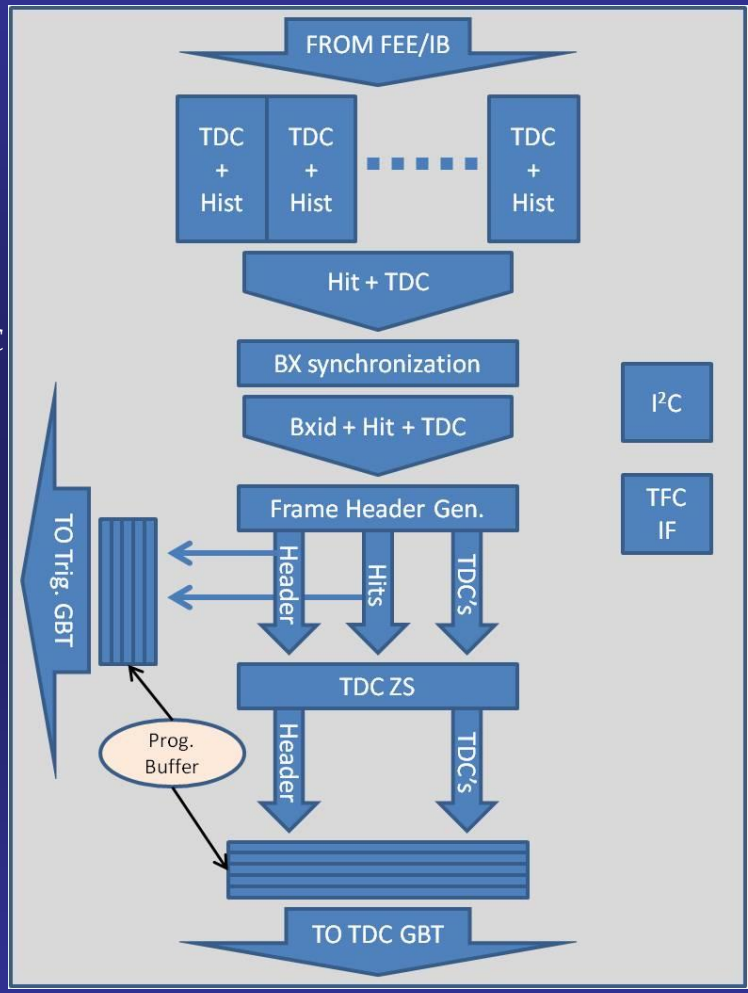
8 ch vs 32 ch

Histo for each TDC

No more needs for RAM's + EDAC

TDC data ZS

97 pins vs 220 pins



Why an asic

- Modularity: we are thinking at three possible modularity (32, 48, 96 channels), to best fit the requirements for:
  - Power consumptions (less then 20mA per channel)
  - Best ZS for TDC data

- An eye on LS3 stage: If we go to design a new detector with higher granularity for at least M2R1 and M2R2 (and maybe for the same regions of M3 too), we have also to design a new front-end electronics and a new front-end board where we can integrate the nSYNC direct on the detector.

Technologies

IMEC DARE (Design Against Radiation Effects) technology:

- Radiation-hardened-by-design libraries in standard commercial technology
  - DARE180 well supported (UMC .18)
  - DARE90 small core & IO library available(UMC 90nm)
- Manufacturing, Packaging, Testing, Characterization (lot) Qualification & Radiation test up to FM is supported by imec's ASIC Services
  - Through subcontractors (Microtest, Maser, MAPRAD)
- Flexible solution
  - DARE allows for mixed signal design
    - Can add specific analog blocks; designed by customer, design house or imec
    - Encrypted models of library cells can be used in analog design environment.
  - Cells can be added to the library
  - IO pads can be customized ...
- Imec has expertise on the full DSM design flow
- They tested DARE digital blocks up to 1 MRad without failures or leakage current increases.
- SEU performance is in the order of a LET cross-section of 48/60 Mev.

The muon firmware now

- 24 (max) ODE boards per tell1
- Zero suppression
- Data packing
  - Logical channel address inside tell1 (12 bits)
  - TDC value (4 bits)
- Logical pad coordinates for HLT1
  - Logical pad reconstruction and address packed in 16 bit word

The muon firmware for the tell40

- 48 (max) nODE boards per tell40
- Zero suppression done in the nODE boards
- Data packing with only TDC info (baseline)
  - TDC value (4 bits)
- LLT trigger signal managing (if any)
- Logical pad reconstruction
  - possible only in the trigger tell40 board (useful ?) or if we send also the geographical address of the hits (foreseen only in the trigger tell40)

Very preliminary…
work just started

Tell40 for the muon LLT trigger

- Actual L0 looks for aligned hits with high pT
  - Search done dividing the detector in 192 pointing towers
  - M3 fired pads are the starting points (seeds) to build the track
- Data received without zero suppression: 1 bit per channel, in a fixed structure (no change respect to now)
- Trigger tell40 can houses some useful logic
  - Logical pad formation and other ….
- In case the “TDC” tell40 write only the TDC words (without address) the trigger tell40 must write all the fired hits (logical channels). In this case a zero suppression could be necessary

FEB control and pulse distribution

Up to 8 Cardiac Board for each lvds i2c branch

12 x (I2C+TST signal)

I2c LVDS signals:SCL,SDAin,SDAout

LVDS TST pulse,TTL Reset

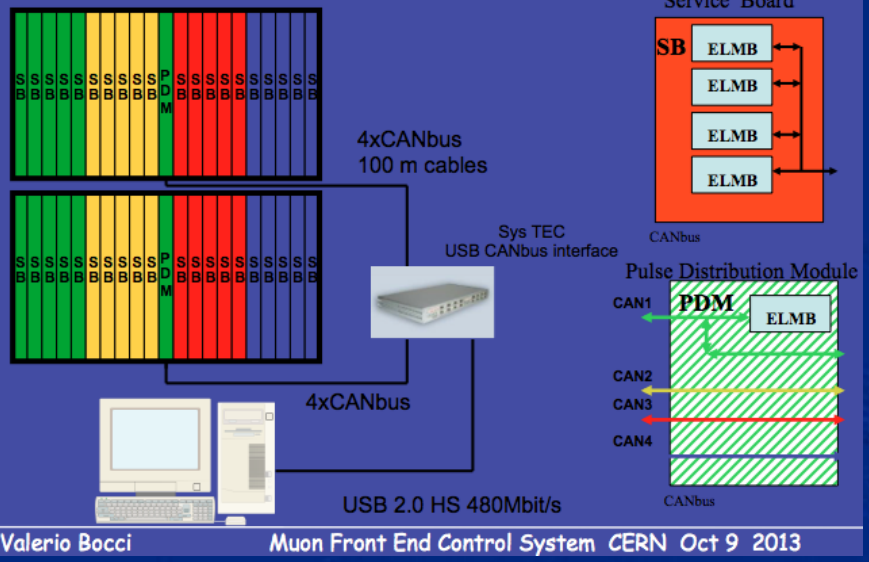
Read Write Dialog Registers

Send pulse to measure rate, calibrate DLL,sync pulse, RESET FEB

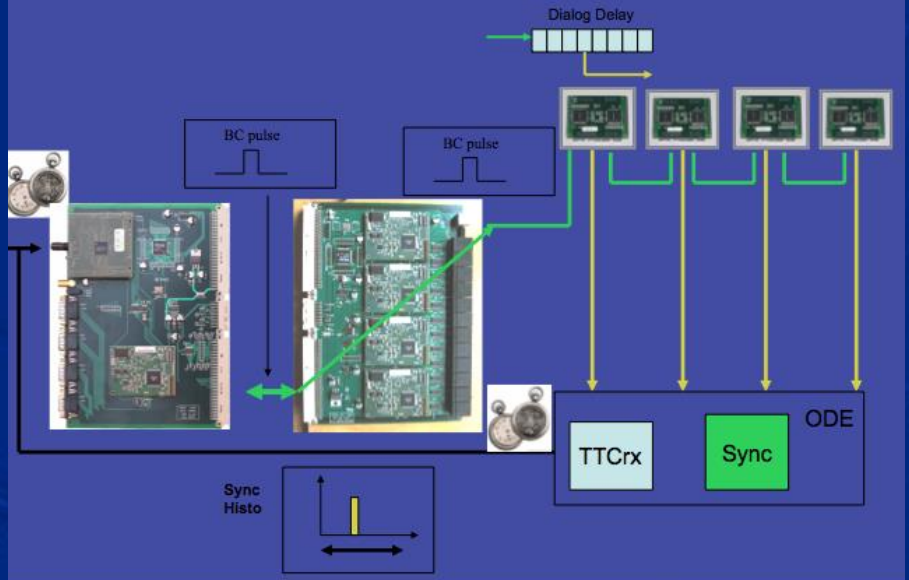
Service Board

- **Service Board**
  - 12 Long distance I2C Like LVDS line
  - 4 ELMB with ATmega 4 Mips processor
  - Flash ACTEL FPGA Timing Pulse generation, control signals
  - CANBus Module

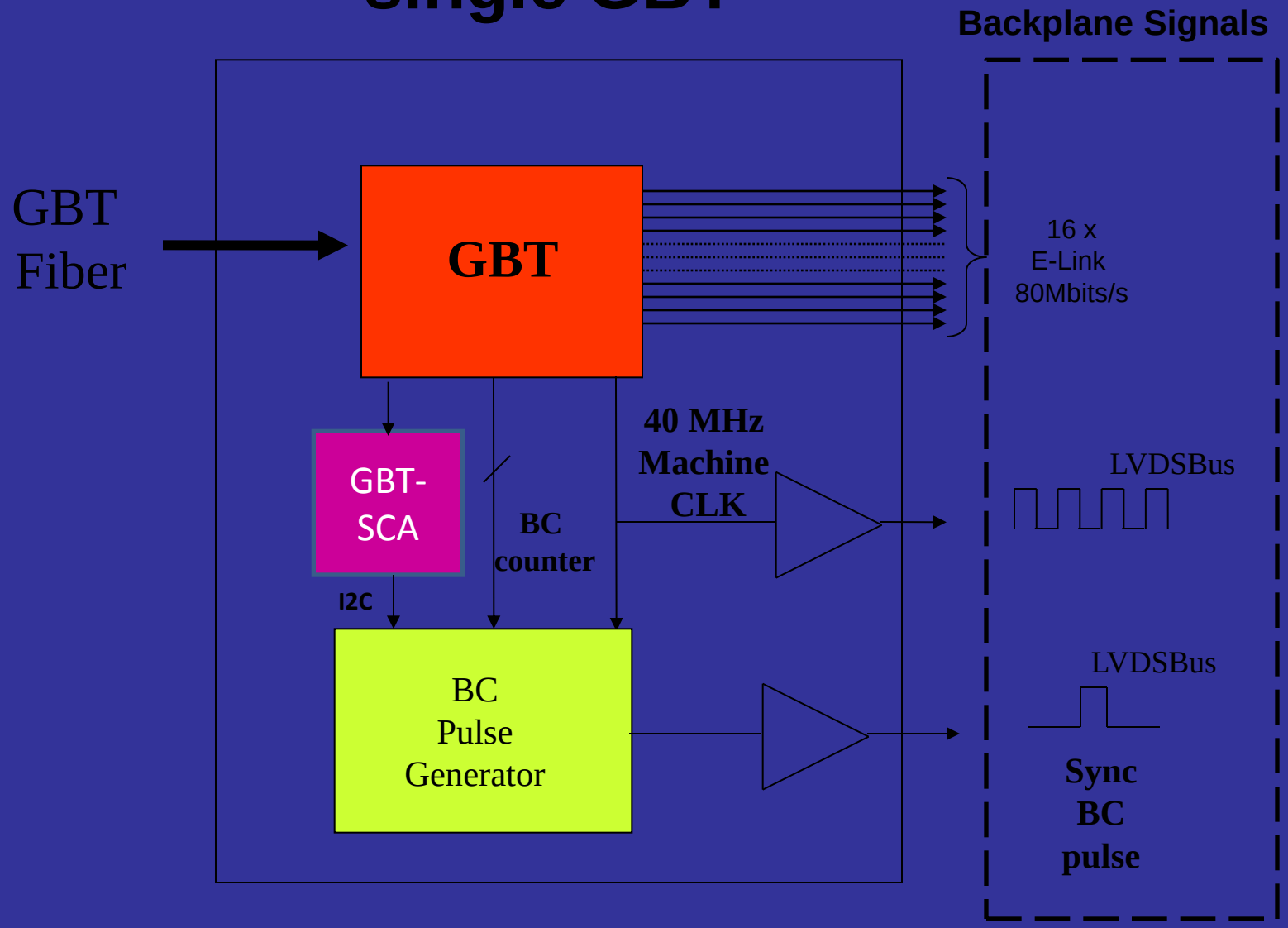
Service Board System



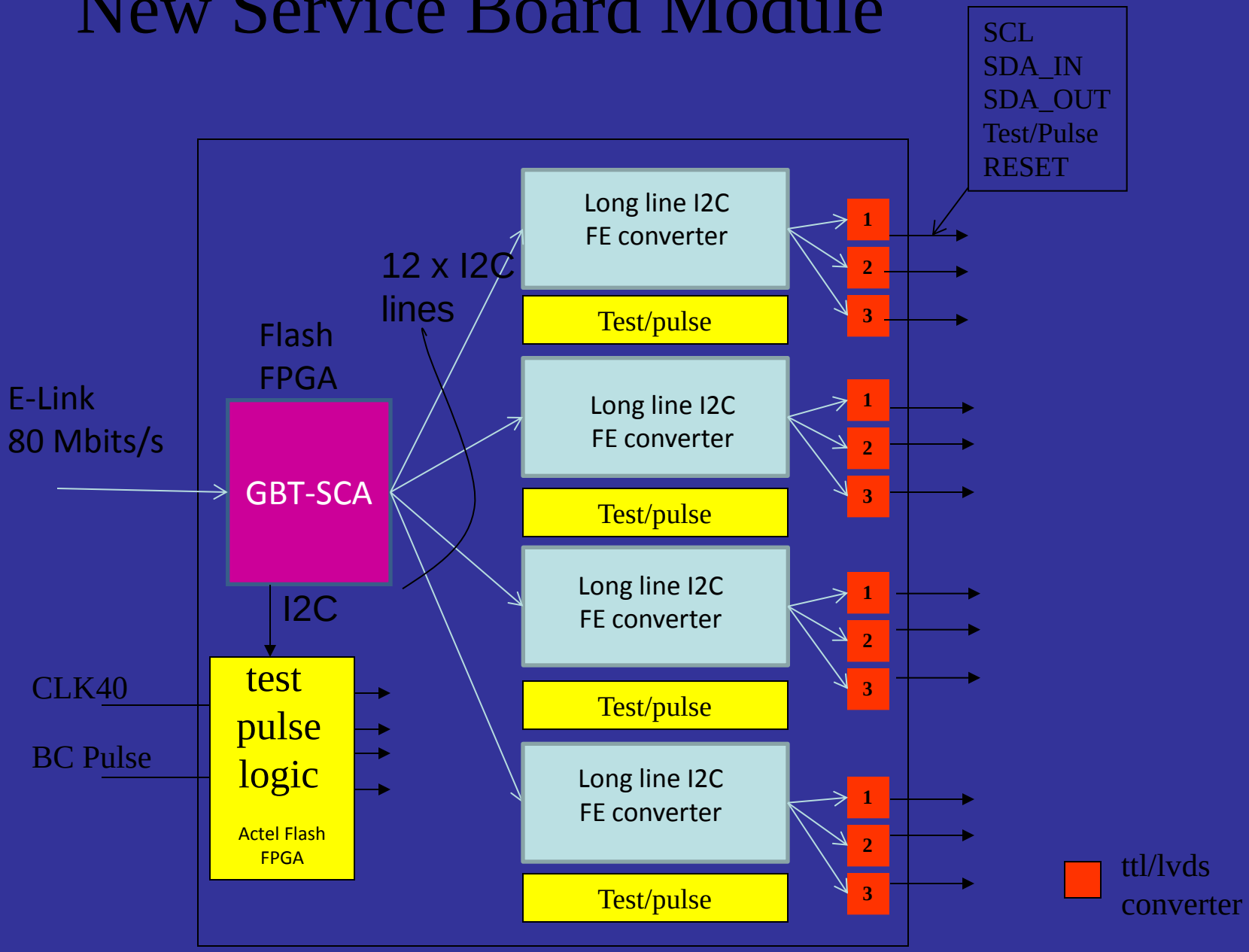
Fast coarse Time Alignment (Without physics)



New Pulse Distribution Module single GBT

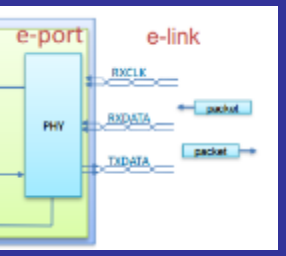


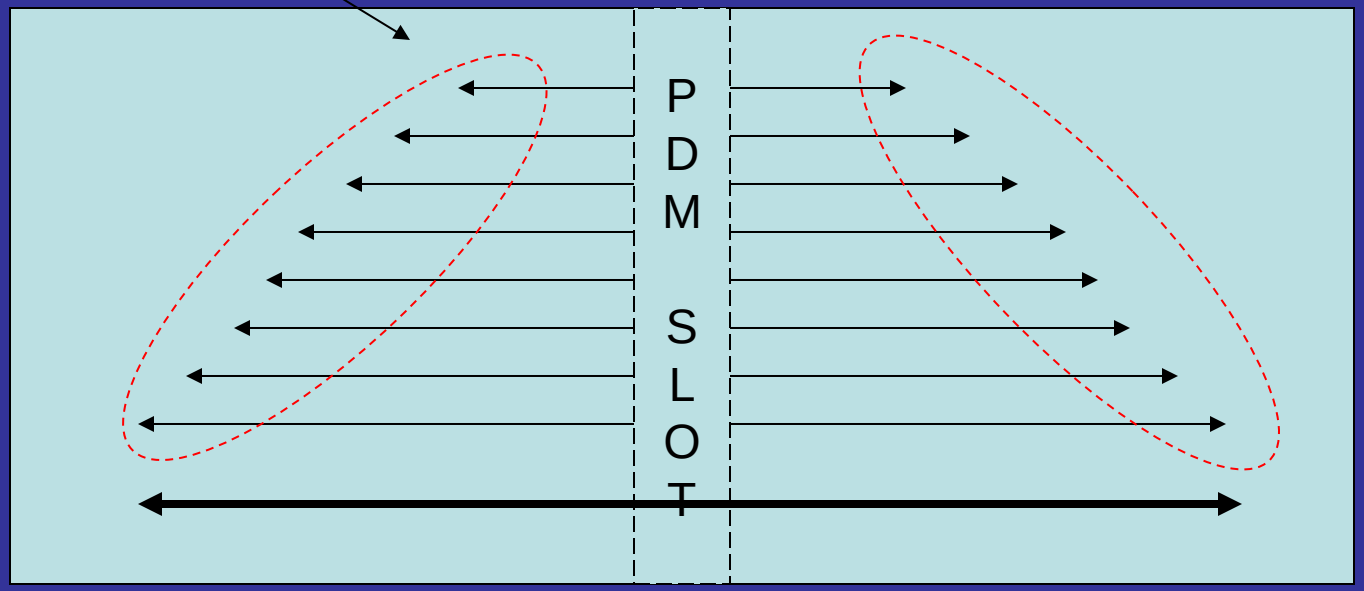
New Service Board Module



New Custom Backplane

80 Mbits/s E-LINK





New Custom Backplane routing 80 Mbits/s E-Link Lines
And Service line

Reviewer's Report - General

- Very constructive review
- Careful monitor contacts' signs of oxidation
- Evaluate radiation level for upgrade
- Improve current ECS "features" in the upgraded system
- Documentation
- Test the new architecture using occupancies from simulation

Reviewer's Report - Readout

- Confusion of link names used during the review – agreed to use HIT and TDC (LLT only uses HIT info)
- Is it necessary to transmit TDC data at 40 MHz?
- ZS of TDC info: issues and possibility of NZS
- Consequence of using WideBus in our environment
- TDC resolution: changes foreseen?
- Include TDC info in HIT stream
- Use GBTX functionalities for clock management
- How to fan-out TFC commands to nSYNC chips
- Use TFC link to upload extra info
- Carefully consider nSYNC technology

Reviewer's Report – back-end, ECS, …

- HIT binary information: used for LLT but need to be acquired
- nPDM: suggested to already think of having 2 bidirectional links
- Configuration/monitoring timing issue: is there a bottleneck on the nSB?
- ECS rewriting
- Test eLink on a backplane
- Radiation tests could be needed on commercial components
- Schedule is aggressive, nSYNC development should start ASAP

Conclusions

- Very helpful review!
- Suggestions / comments taken – thanks!
- Activity on nSYNC planned to start in early 2014
- Push ECS development to proceed in parallel as much as possible
- PID TDR ready ➔ now we can work!