IN2P3
Les deux infinis

Firmware integration and compilation status

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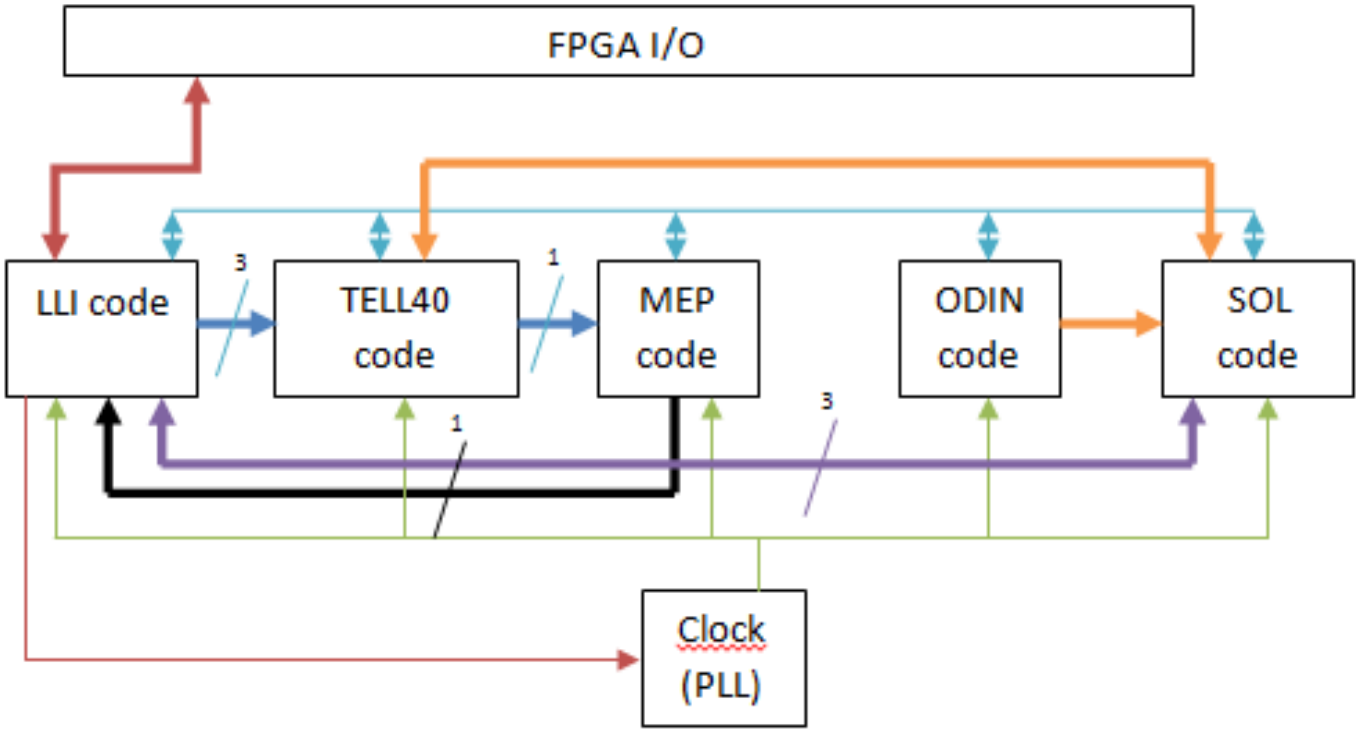
Outline

- Architecture
- Integration
- First results
- Next steps

Firmware architecture for compilation



Clock generation :

- Clock from AMC40 quartz
- PLL Clocks

LLI code interfaces:

- All FPGA interface (PCIe, GBT, 10GbE, SPI, clock ...)
- BAR0 memory interface: Avalon MM
- 3 Links : FE data: 84 bus + data_valid signal

TELL 40 code interfaces:
(Data processing)

- 1 Link : FE data: 84 bus + data_valid signal

MEP Code :

- MEP data

TFC : ODIN and SOL code

3 Links to control the 3 FE :

- data: 84 bits bus + data_valid signal

TFC backend and frontend links

- TFC data : 32 bits bus (80MHz)

Firmware integration

Firmware integration occured from 2 to 6 december at Annecy and CERN :

- Each designer came with a part of the firmware :
  - LLI from Marseille (Fred)
  - TELL 40 from Annecy (Guillaume)
  - MEP from CERN (Paolo)
  - ODIN and SOL from CERN (Federico)

- 10Gbe module has been integrated into the LLI code
- VHDL top level of the MiniDaq and a common tcl script that sources alls the vhdl files and assigns the FPGA pins have been written.

The last two days, in CERN, a first compilation was launched :

- Few VHDL mistakes were corrected
- At the end of the week, full compilation of the MiniDaq was successful.

Firmware compilation first results

FPGA ressources and compilation time depend on the data format :

			Parameters								
Data Format			***(bits)***	***Header (bits)***							
Header length	***data length***		***GBT frame***	***BCID***	***Info.***	***length***	***data length unit value***		***logic resources ****	***memory ressources ****	***Time ****
variable	***variable***		80	12	1	7	4		37%	8%	1h
variable	***variable***		80	4	1	4	4		35%	8%	1h
variable	***variable***		80	4	1	4	8		35%	8%	1h
fixed	***variable***		80	12	1	7	4		12%	8%	32
fixed	***variable***		80	8	4	4	4		12%	8%	32
fixed	***variable***		80	8	4	4	16		11%	8%	31
fixed	***fixed***		80	7	9	X	X		5%	1%	25min

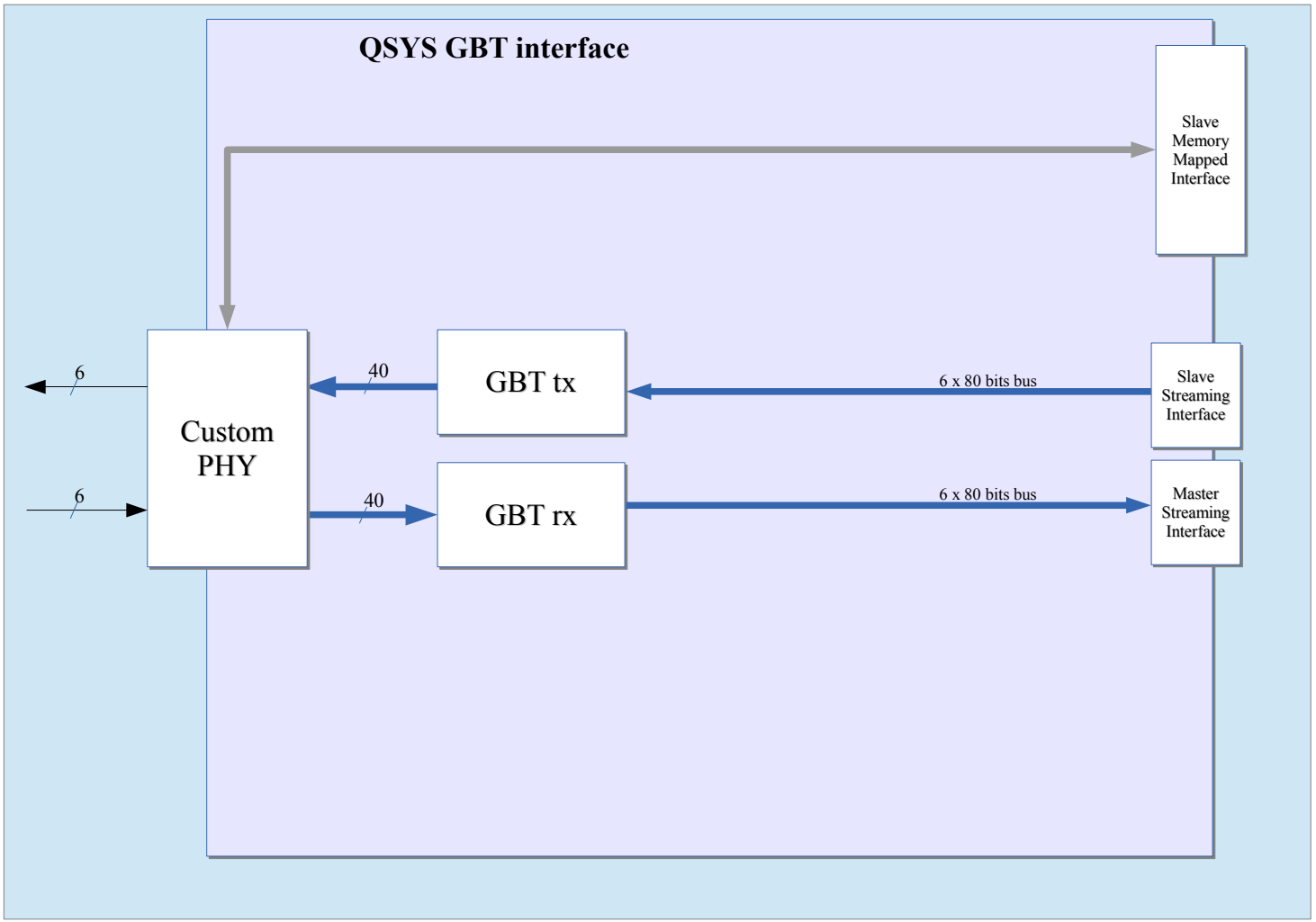
Resources and compilation time increases when ***Header length is variable***
To reduce the ressources, a ***fixed header*** length should be used.

** These first results are priliminary : The compilation warnings must be checked to have consolidated values*

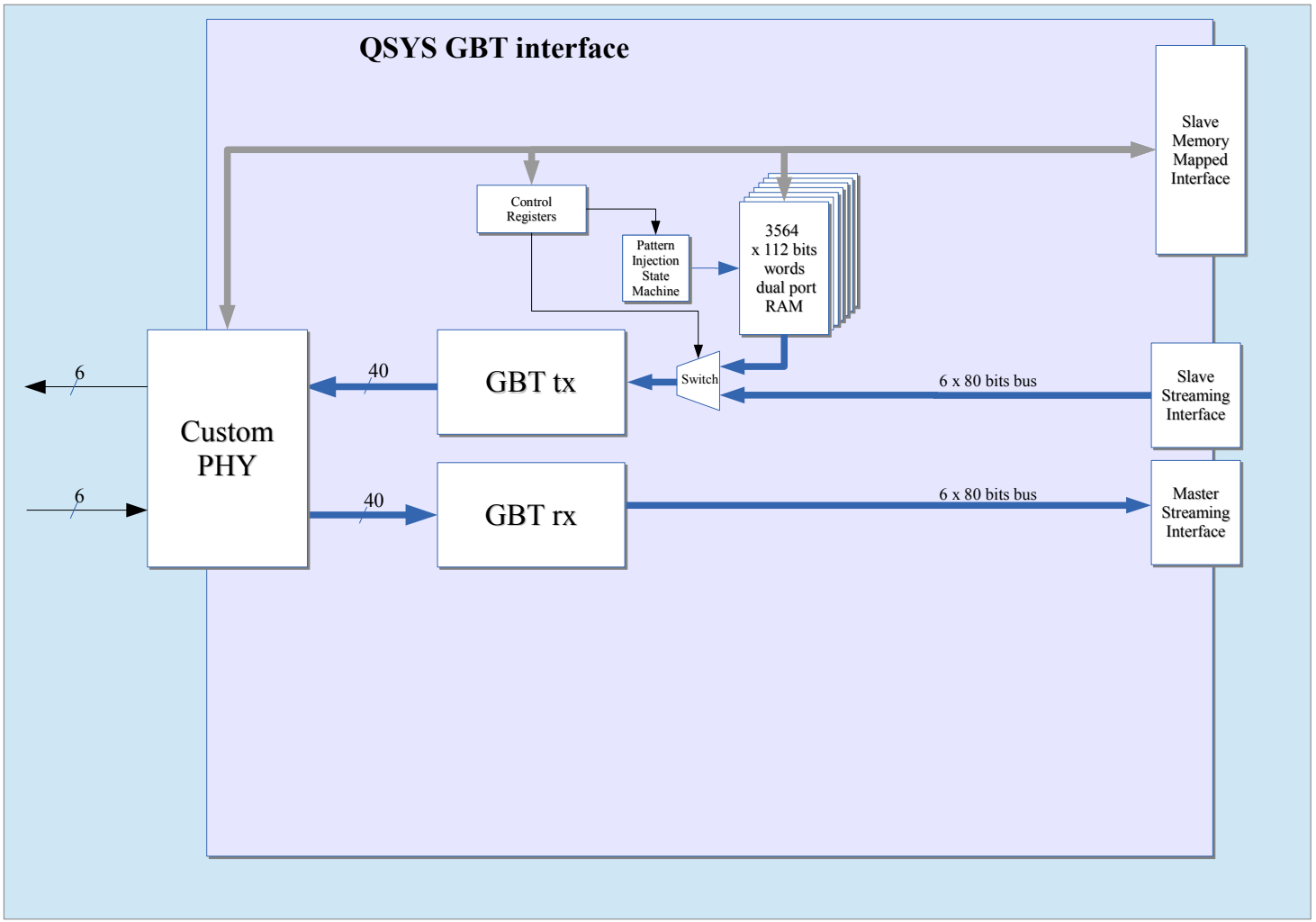
Next steps

- Each designer has to check the warnings from compilation
- Timing constrainsts have to be applied
- An important period of test and validation begins with hardware and software
- Marseille has to implement a memory to inject stimuli using ECS

Current GBT interface in MiniDaq



Next GBT interface in preparation: injection memory on the TX side



Conclusion

Header type should be chosen in taking FPGA ressources into account.

The steps above and the injection memory will be available at the next Electronics Upgrade WG

In the meantime simulation is available and operational.