FONDAZIONE BRUNO KESSLER

Silicon Buried Channels for Pixel Detector Cooling

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Outline

- Introduction
- Microchannel fabrication: process flow, different geometries and hydraulic diameters
- Thermal and structural characterization
- Conclusions and perspectives
- Further technological tests

Introduction

Detectors require a **cooling system** able to evacuate the power dissipated in the active region by the front-end electronics

We propose the **integration of the cooling system within the** detector based on **embedded microchannels made by DRIE** technology

Advantages: optimization of thermal bridges, transparency to the incident particles and minimizing the material budget

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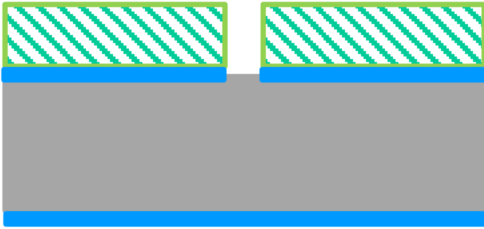
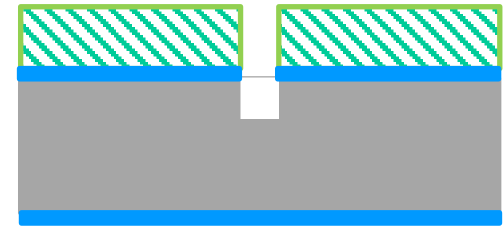
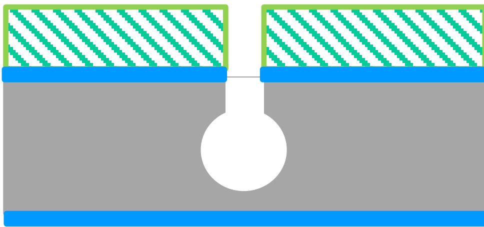
Process flow



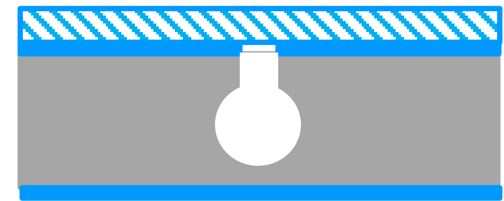
1) Define & etch SiO_2



2) DRIE anisotropic process



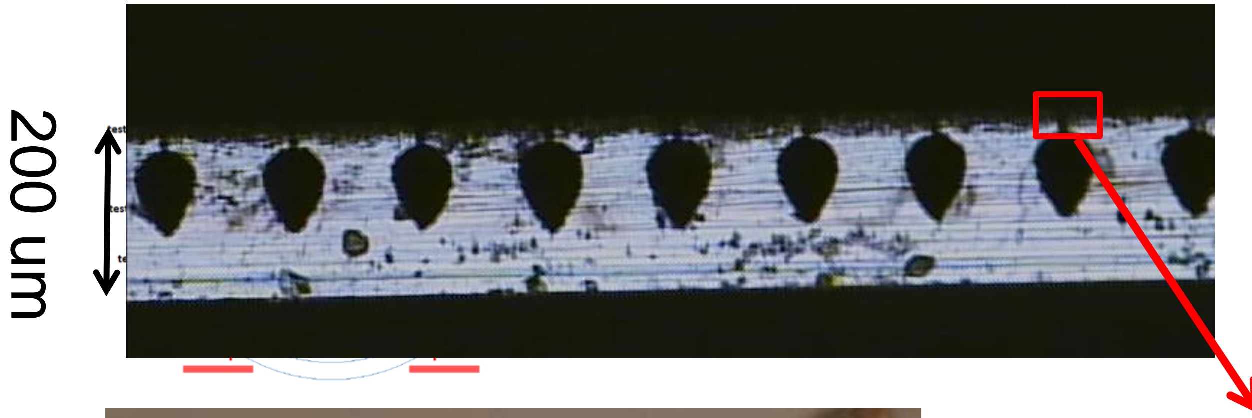
3) DRIE isotropic process



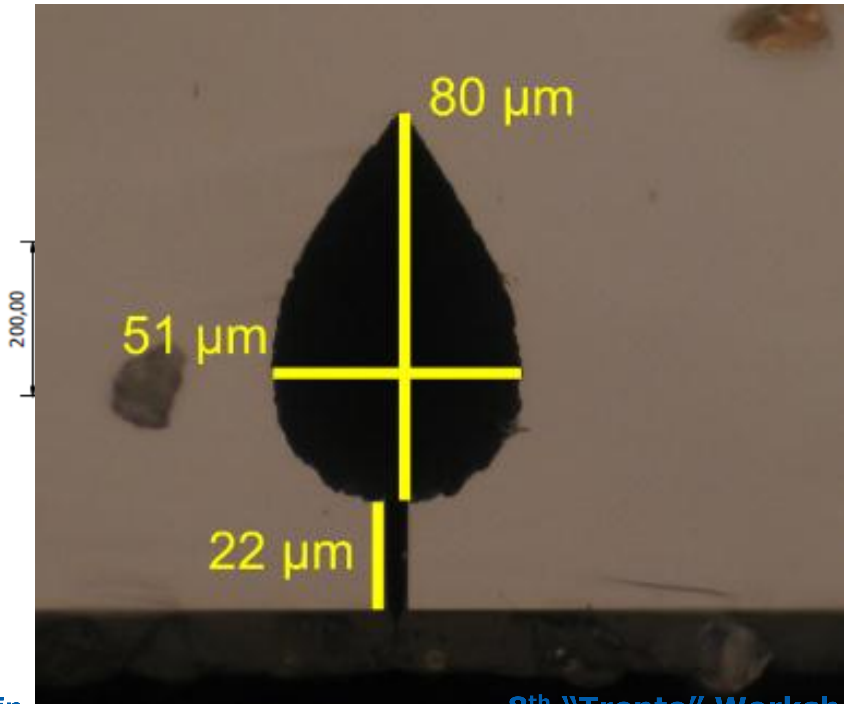
4) Sealing: PECVD deposition

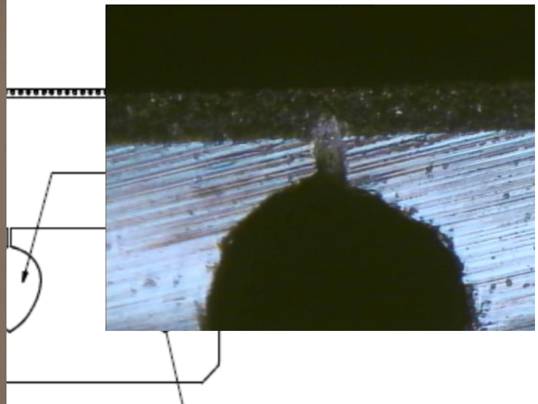
Avoiding high temperature steps, the process is in principle compatible with a CMOS device.

Channels made with individual holes:



Layout 1

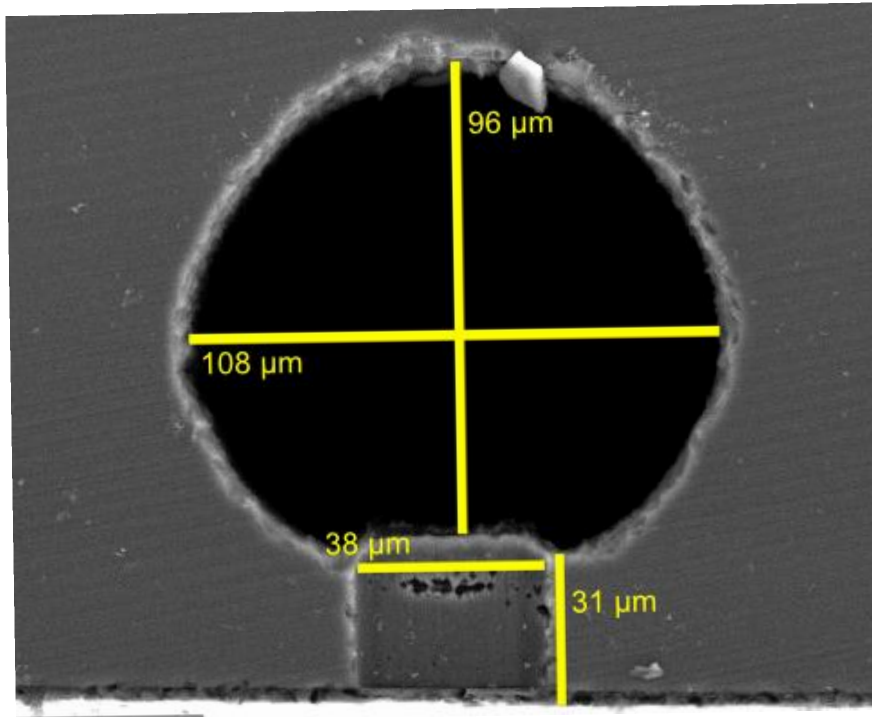


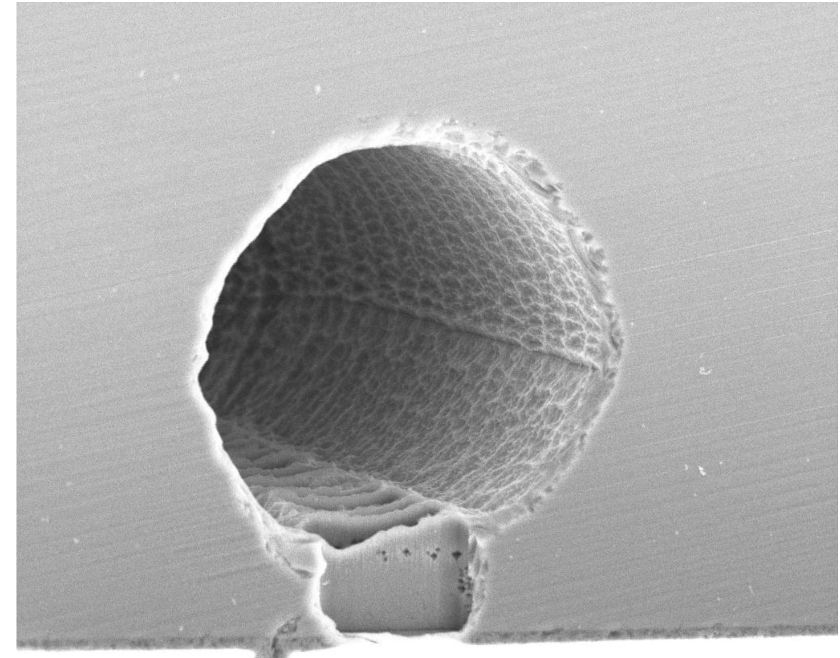


Section related to the DRIE process and the width of the surface channel, the length by the layout

Channels realized as a sum of individual holes:

Layout 2





Round section and increased diameter

Channel diameter related to the length of transversal channel and not to the width

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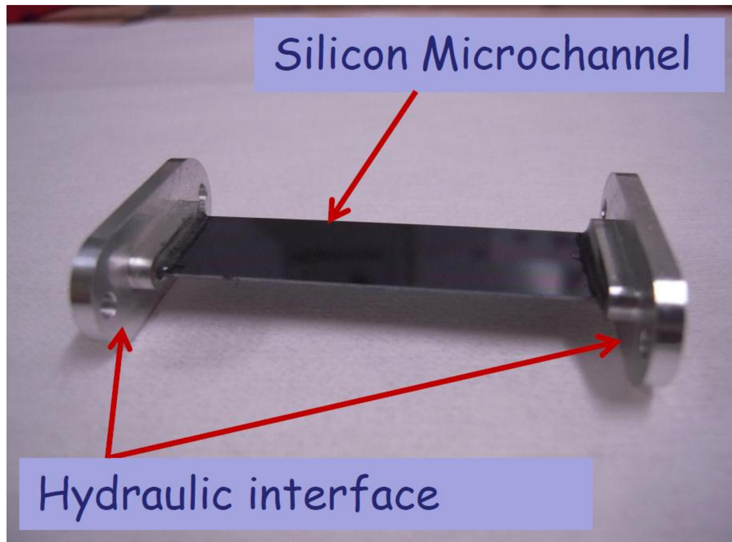
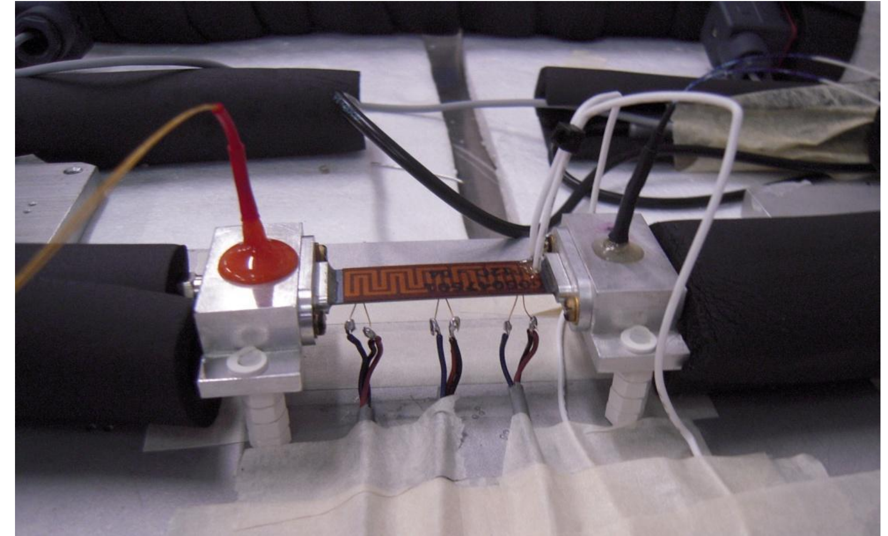
Hydraulic test set-up

tests made in the TFD Laboratory @INFN-Pisa





Hydraulic diameter of channel: from 50 up to 100 µm
Channel length: 60 mm

Thermal tests (1)

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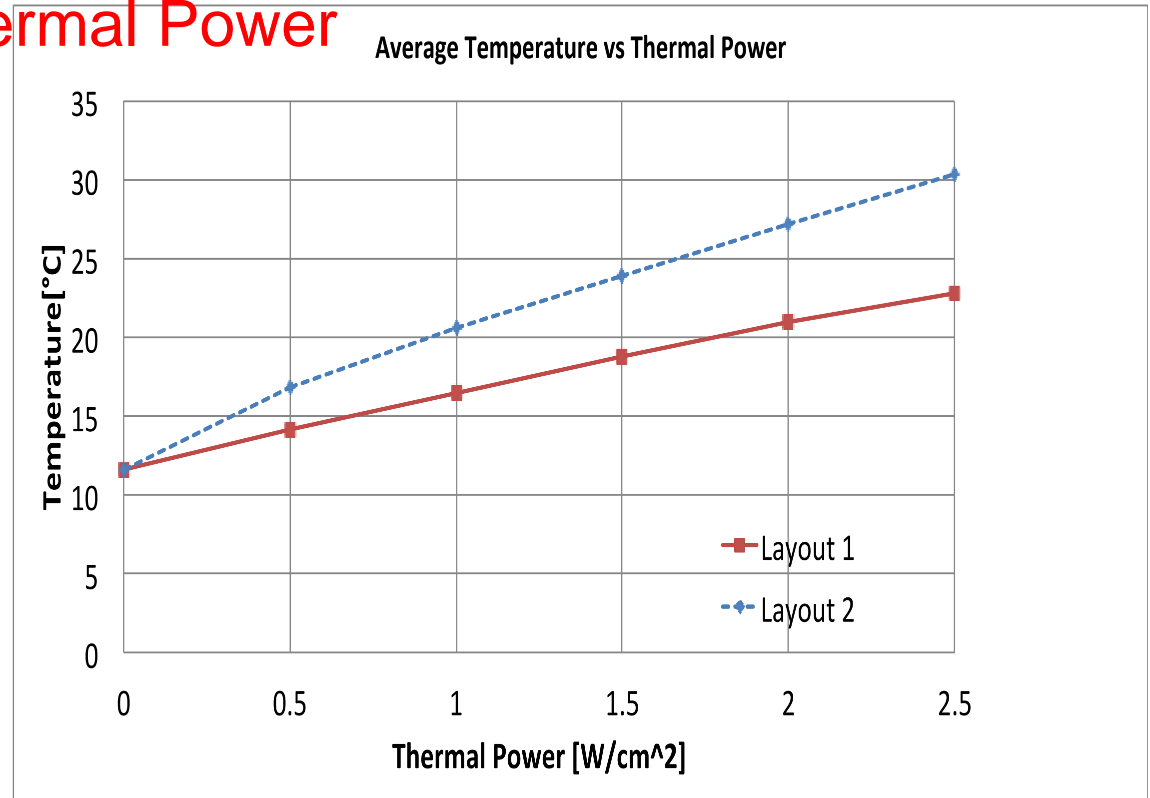
Temperature vs Thermal Power

Hydraulic diameter of channel: 70µm
Channel length: 60 mm

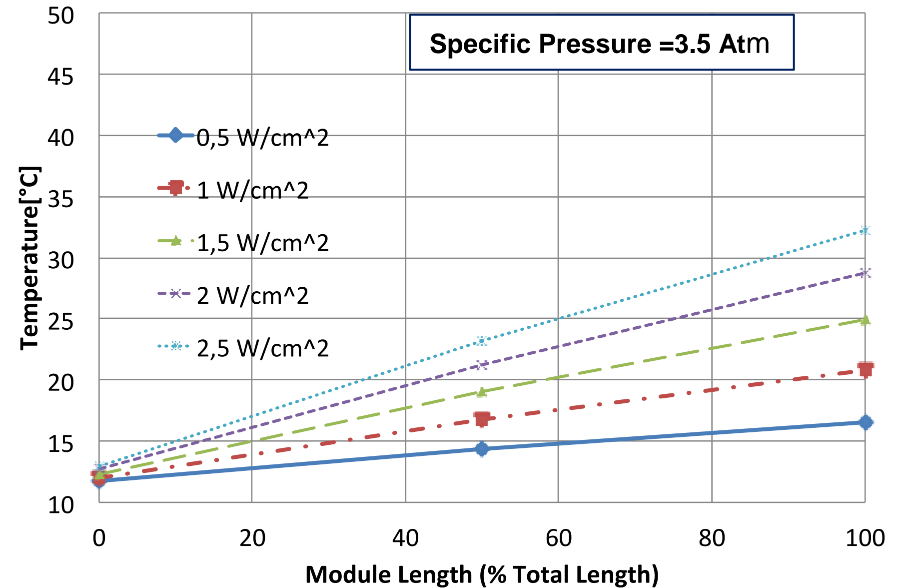


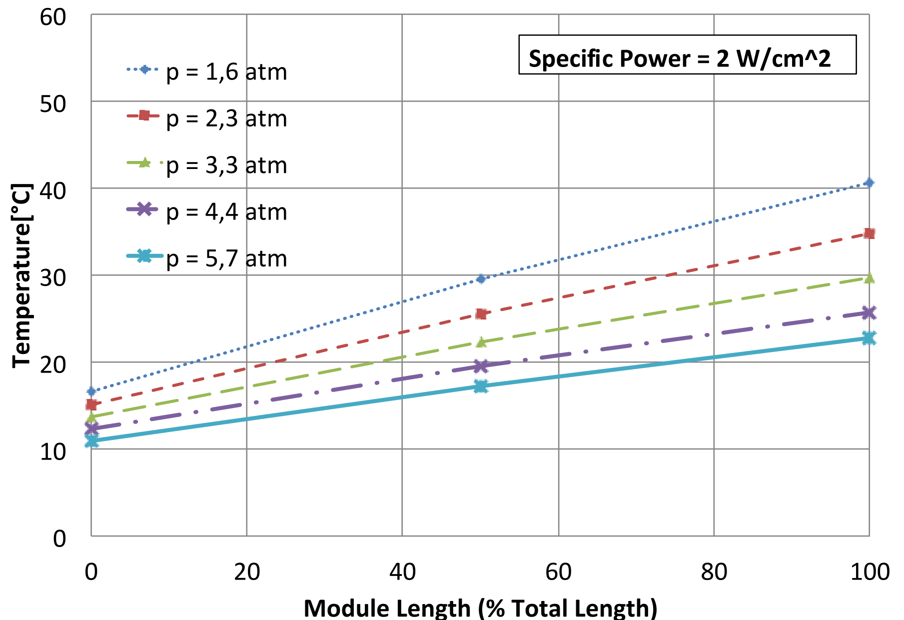
Test: to transfer thermal powers up to 2.5 W/cm² on sample cooled by water-glycol mix. 50% @ 10° C at the inlet :

→ temperature **< 25-30ºC** with a dissipated **power up to 2.5W/cm²** and a **pressure of 6.9 atm** of cooling liquid

Thermal tests (2)

Temperature along the silicon module





Layout 1 (die 12.8 x 60 mm^2):
- 80 channels/ hydr. ∅ ~70um
- step 150um

Structural Test: Mechanical resistance

Dedicated set-up for high pressure structural tests (oleodynamic connections and instrumentation suitable for the measurement of high pressures)

Test: Pressure increased in step of 10 atm every 10 minutes and to remain for 1.5 h at the reached pressure

→ Microchannels resist at pressures **greater than 100 atm** (limit of the pump) for both layouts. No damage is observed on the sample.

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Conclusions and Perspectives

Achieved capability to realize microchannels into silicon wafers, using DRIE technology to dig the channels and PECVD to seal them. The tests show:

- ✓ **Efficient cooling of power up to 2.5W/cm^2**
- ✓ **Mechanical resistance up to high pressures (100 atm)**

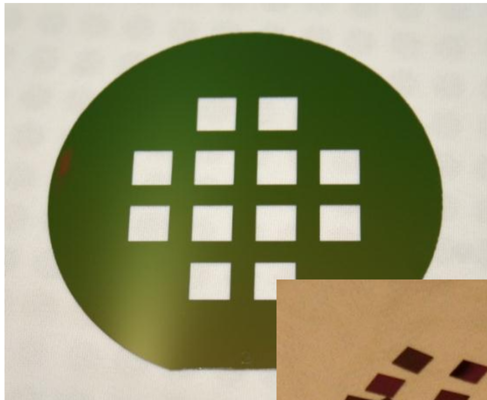
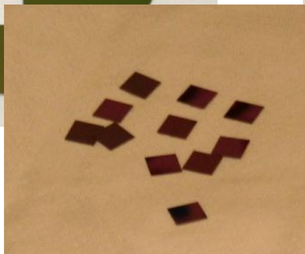
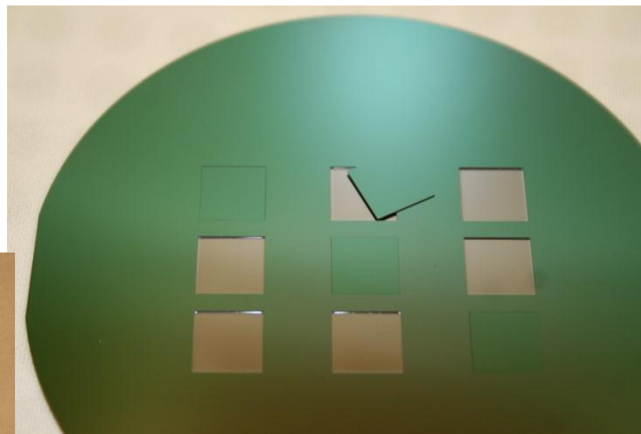
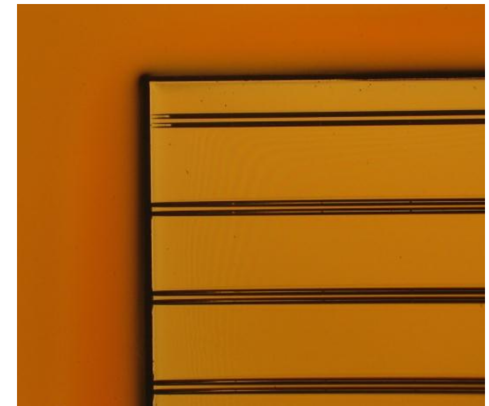
Further developments:

- ✓ Optimize microchannel design: hydraulic diameter/pitch
- ✓ Special **microchannels with bidirectional flow** to be used to improve performance (decrease the temperaure gradient along the module)
- ✓ Realize **microchannels on single silicon die**
- ✓ Electrical characterization of microchannel-cooled CMOS FE chip

Further technological tests

- "Simulation" of channel formation on single cutted device by using silicon square samples with same size than real chip:

- 1- realization of square samples by DRIE etching through a silicon wafer
- 2-realization by DRIE of a support wafer with "pools" to contain square samples
- 3- litho and DRIE etching on square samples inserted in the squares pools of support wafers

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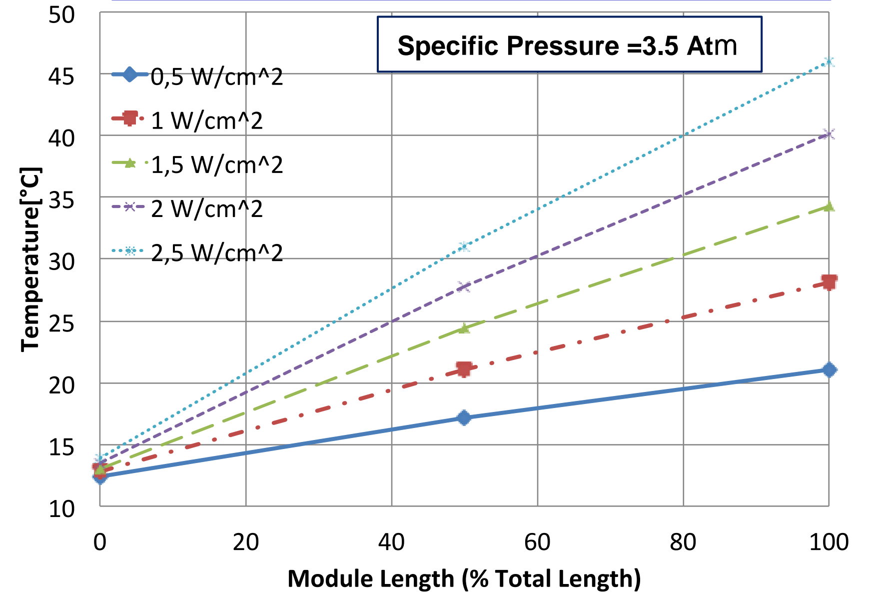
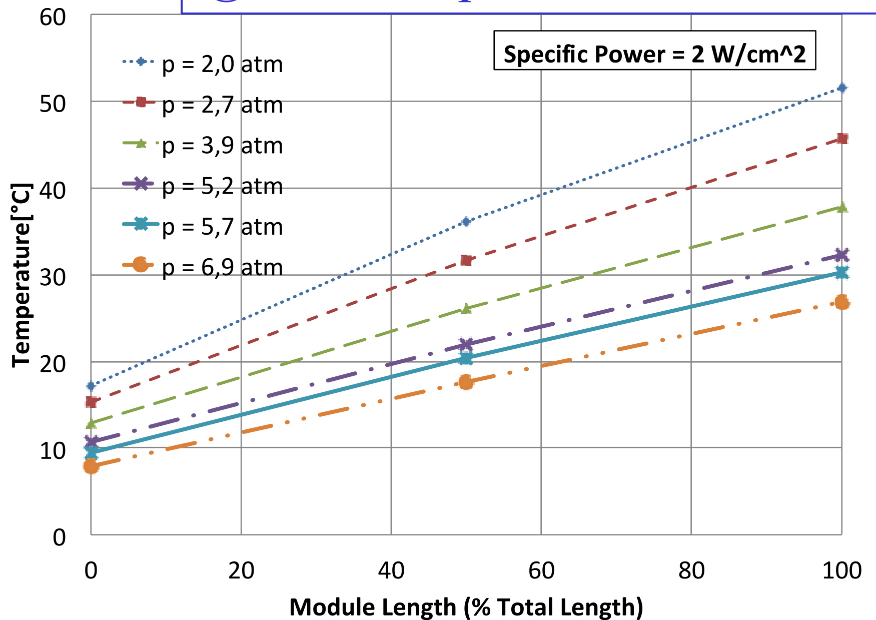
Thermal tests (2b)

Temperature along the silicon module





Layout 2
(die 12.8 x 60 mm^2):
- 80 channels/hydr. ∅ ~70um;
- step 150um