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A thin and fully depleted monolithic pixel sensor in SOI technology

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The Silicon On Insulator (SOI) technology is one of the leading technologies for the realization of monolithic pixel sensors on high resistivity wafers. A commercial, deep-submicron SOI process by LAPIS, coupled with high-resistivity silicon substrates, is made available through KEK. In this process, a full CMOS circuitry is integrated in a 40 nm thick layer on top of each pixel. Thanks to the realization of vias through the 200 nm thick Buried Oxide (BOX), pixel implants can be created and the 260 μm thick substrate can be reverse-biased and depleted to improve charge collection.
In the framework of an international collaboration between INFN and University of Padova, LBNL and UC Santa Cruz, we have realized monolithic and depleted pixel sensors in SOI technology, both for charged particle detection and for imaging applications. In this contribution we will review the latest chip produced, the so called SOImager3, a matrix of 256×256 pixels of 13.75 μm of pitch. This chip has been thinned down to 70 μm, back-processed and successfully tested with soft X-ray photons in back-illumination at the Advanced Light Source (ALS) of LBNL and with 300GeV pion- at the CERN SPS. These results show that a thin, fully-depleted SOI pixel provides charged particle detection capability with large signal-to-noise ratio and detection efficiency and achieves a single point resolution of the order of 1 μm.

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