The ATLAS Insertable B-layer (IBL) project

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on behalf of the ATLAS Pixel Collaboration

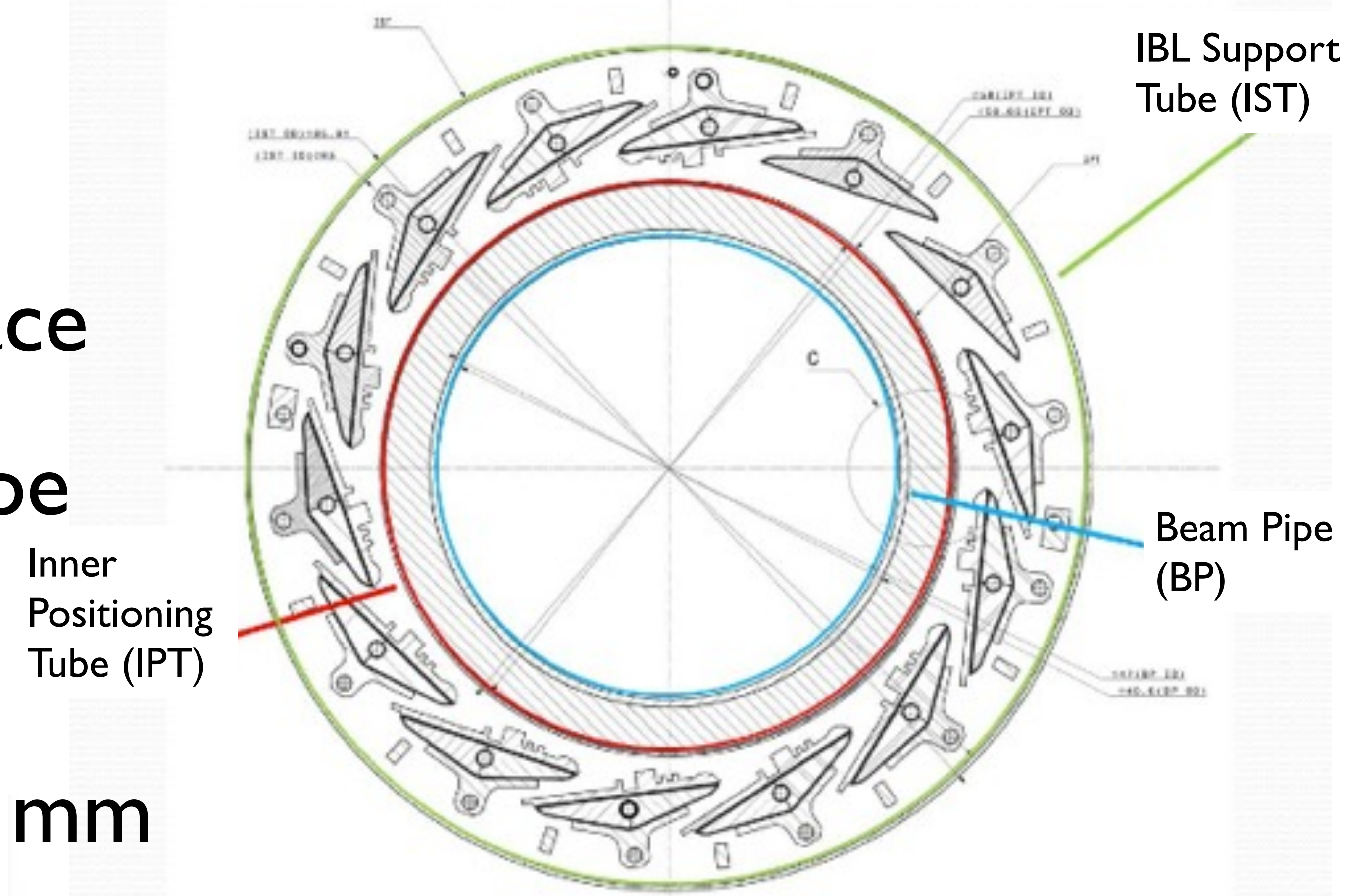
8th Trento Workshop on Advanced Silicon Radiation Detectors (3D and P-Type Technologies).
Trento, Italy. February 18th, 2013.

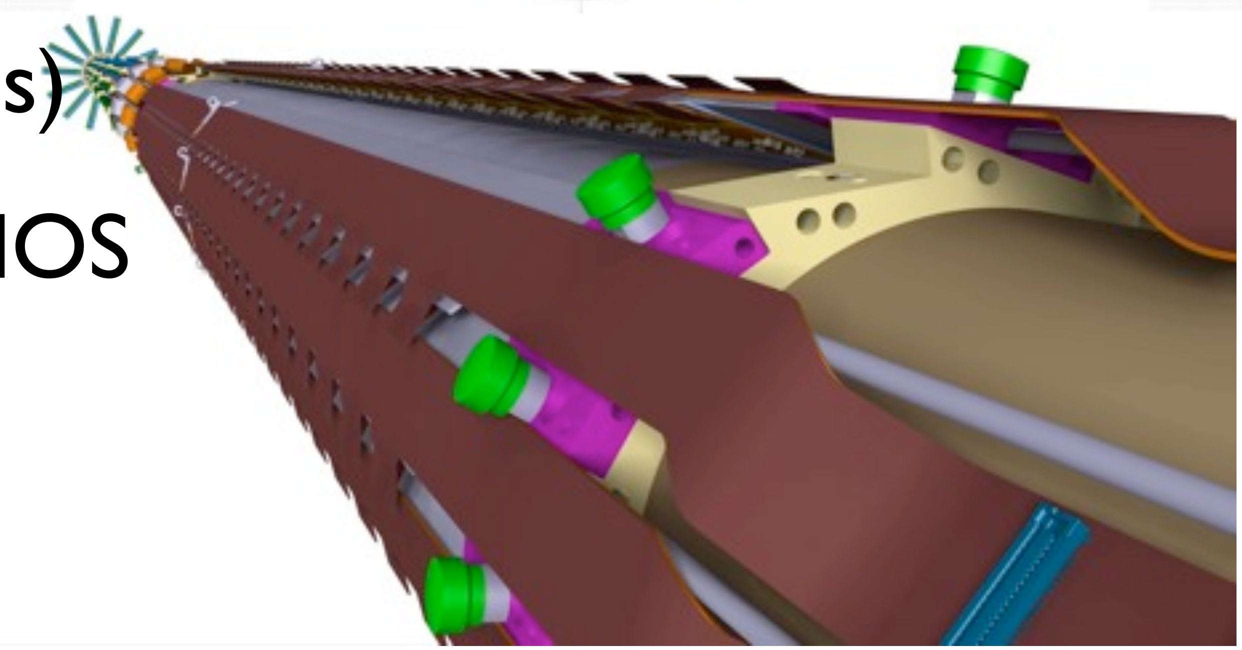
The Insertable B-Layer (IBL)

- ***Motivation***:
  - Excellent vertex detector performance is crucial
    - improve heavy flavor tagging, primary and secondary vertex reconstruction/ separation
  - Additional innermost layer will boost tracking performance
    - adds additional redundancy of the detector in case of radiation damage
- Originally scheduled for LS-2 (2016) then LS-2 was postponed to 2017-18, so that: advance the IBL project schedule and instal it in LS-1(2013-14)

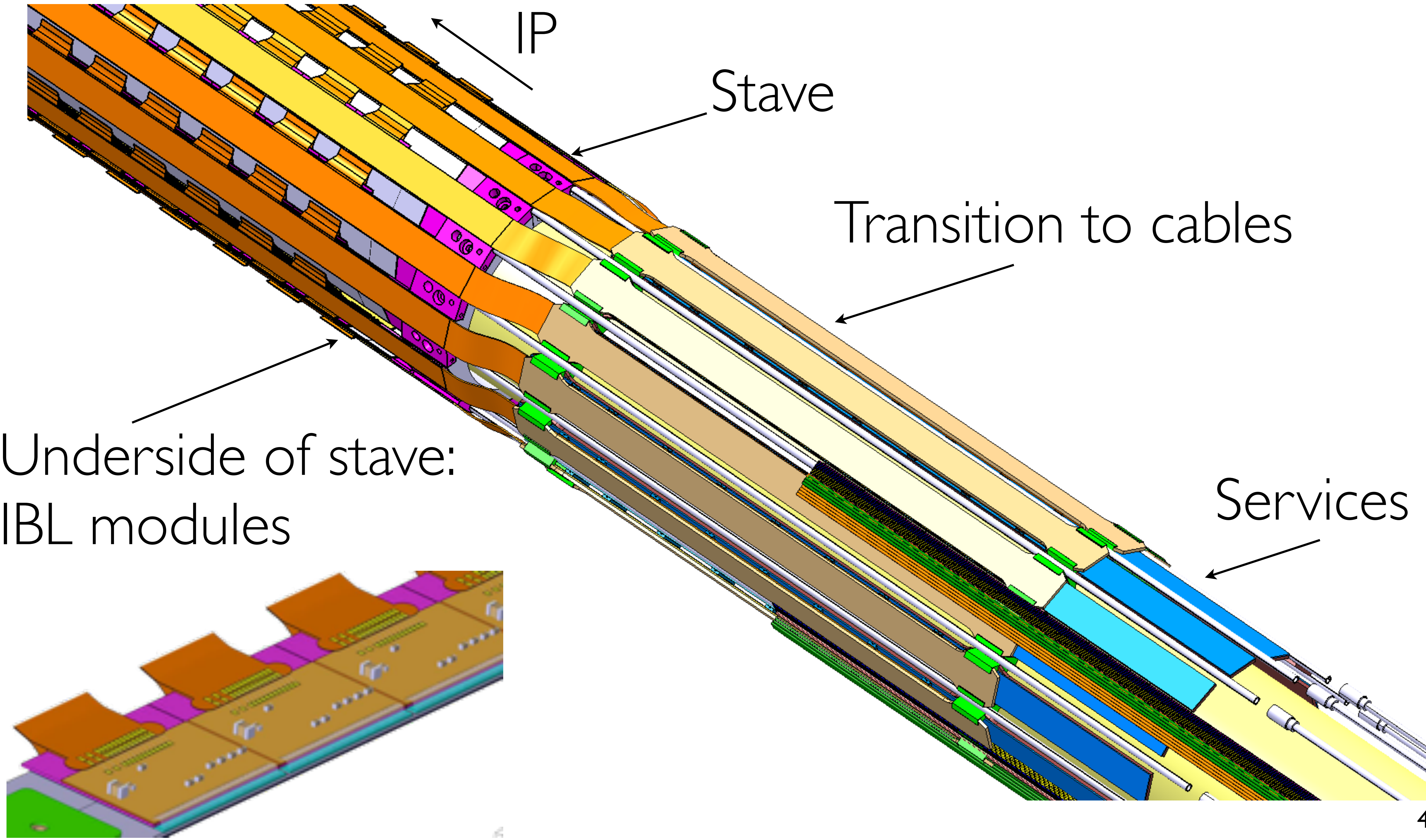
The Insertable B-Layer (IBL)

- Layout based on performance studies in G4 and available space
- IBL mounted on new beam pipe
- Length: ~ 64cm
- Envelope: R_{in}=31 mm, R_{out}=40 mm
- 14 stave (each stave 32 FEI4 chips)
- FEI4 R/O chip in IBM 130nm CMOS
  - cell size: 50um x 250um
  - 80 (col) x 336 (row) = 26880





Stave and module arrangement

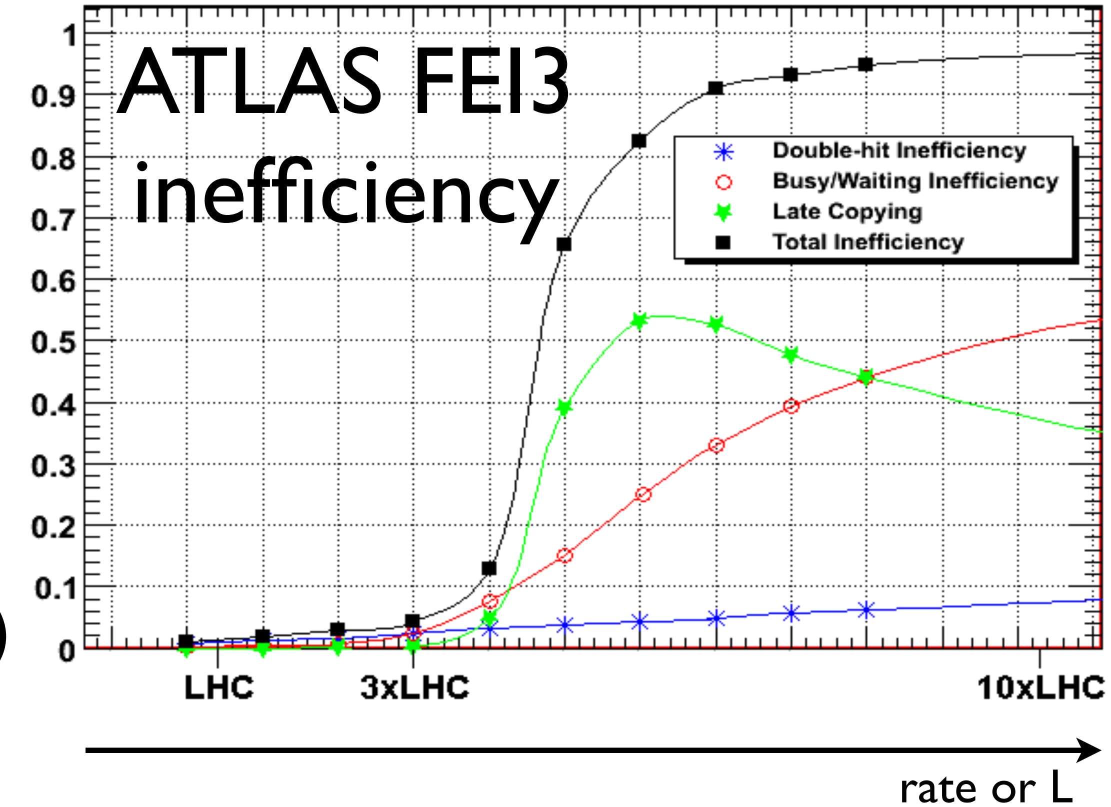


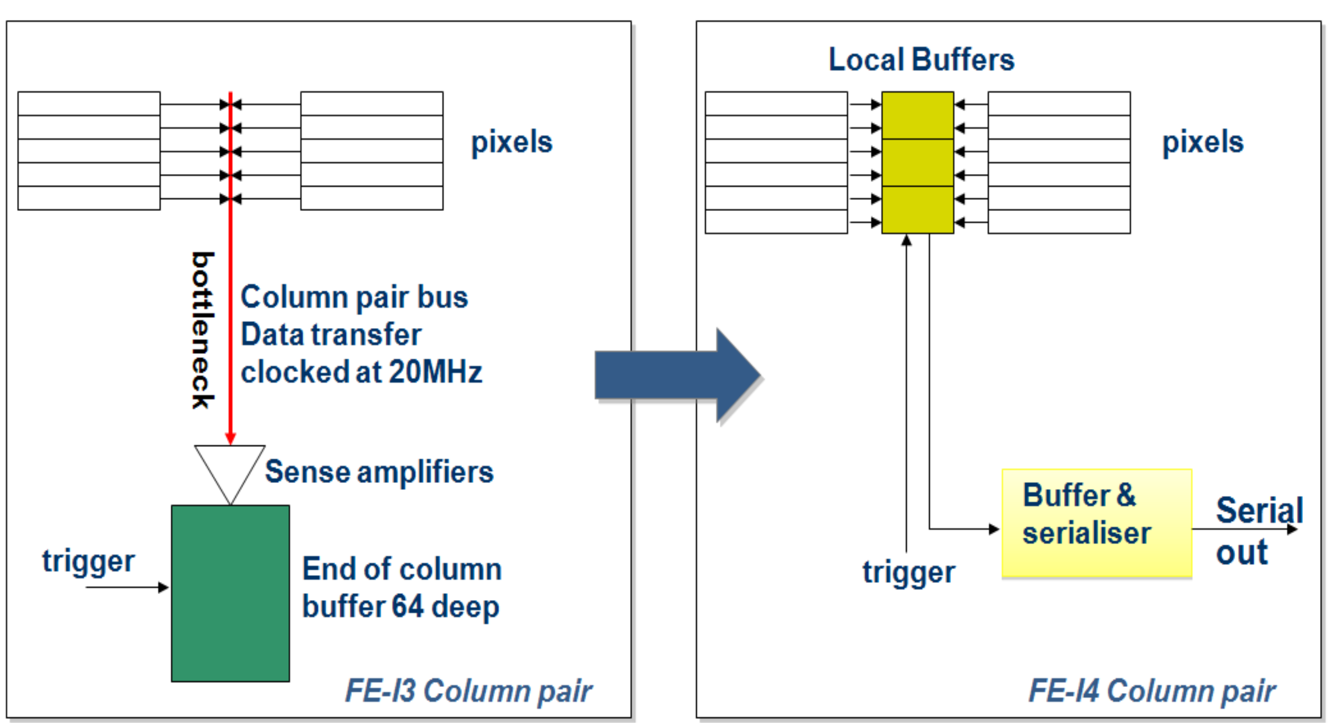
IBL is also a tech step to HL-LHC

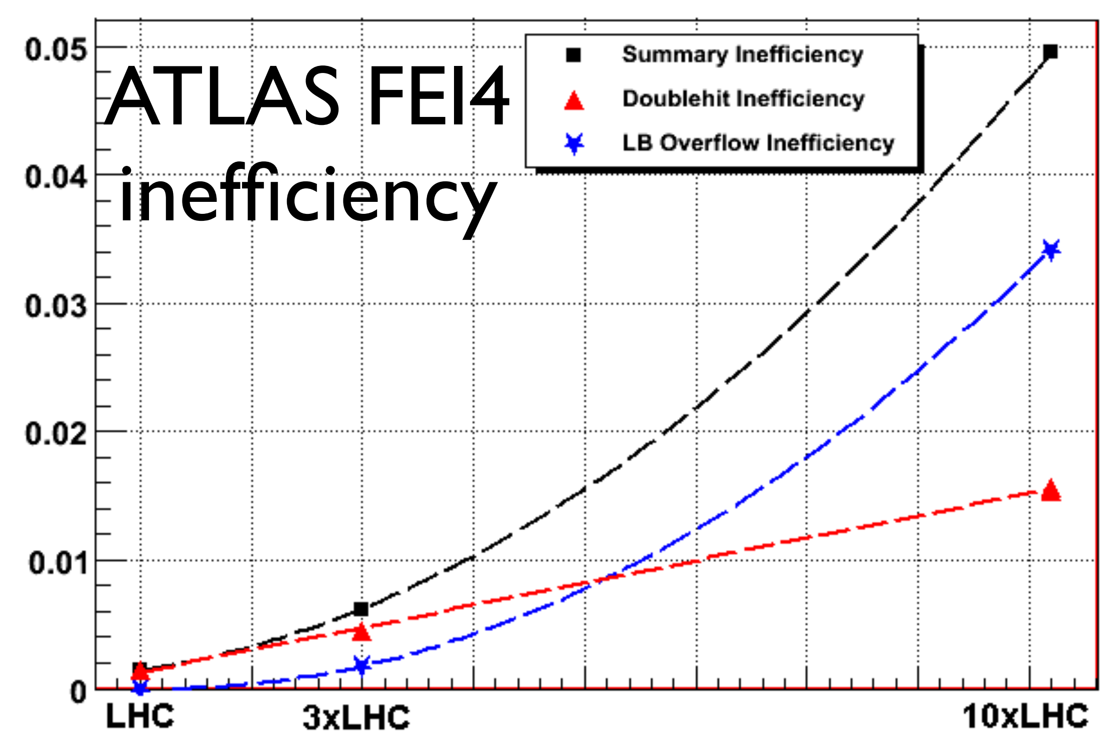
- Sensor with an higher radiation hardness
  - 5×10^{15} n_{eq}/cm^2 NIEL (improved radiation hardness by factor 5)
- New readout chip (FEI4) with finer segmentation, larger active fraction and increased hit-rate capability
  - new readout architecture and smaller cell size 250x50 um^2
  - large single-chip (21x19 mm^2)
- Lighter detector: less radiation length in support and cooling
  - improve radiation length per layer from 2.7% to ~1.9% to minimize multiple scattering in closest layer
  - high efficiency CO_2 cooling at -40 °C coolant temperature
- New off-detector readout system
  - matched to FEI4 pixel chip
  - increase readout speed by a factor 2

The FEI4 readout chip

- Motivation
  - FEI3 inefficiency rises steeply with the hit rate.
  - bottleneck: congestion in double column readout ~> way-out:
    - more local in-pixel storage (130nm)
    - data storage made locally at the PXL level unit until triggered

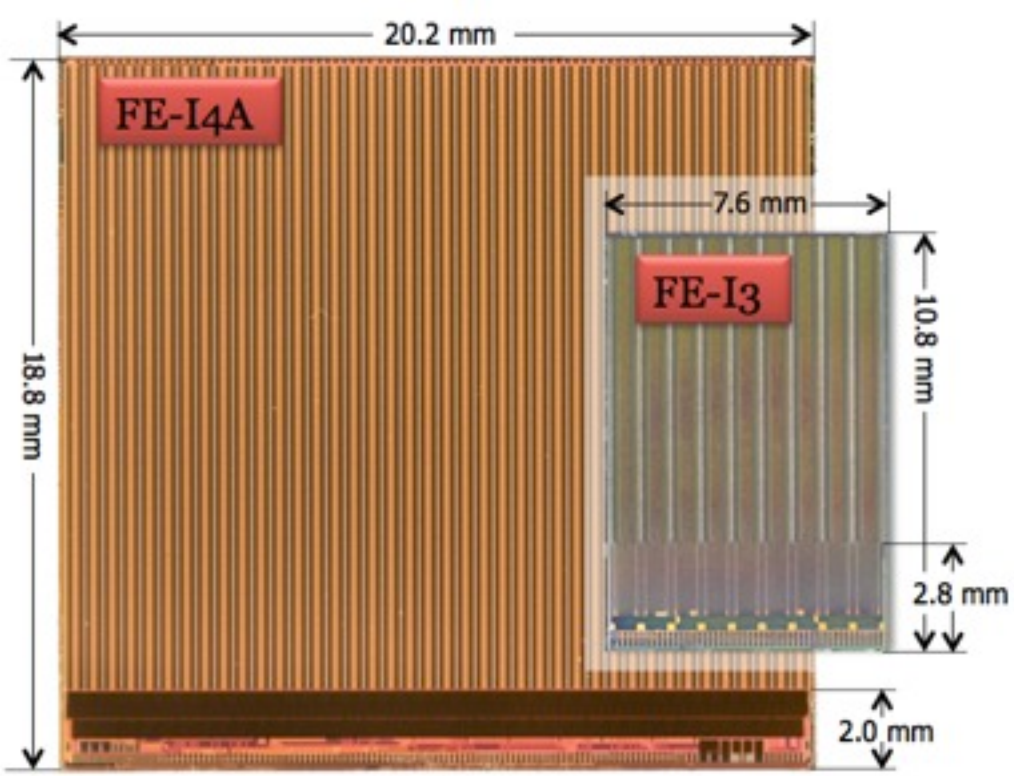






The FEI4 readout chip

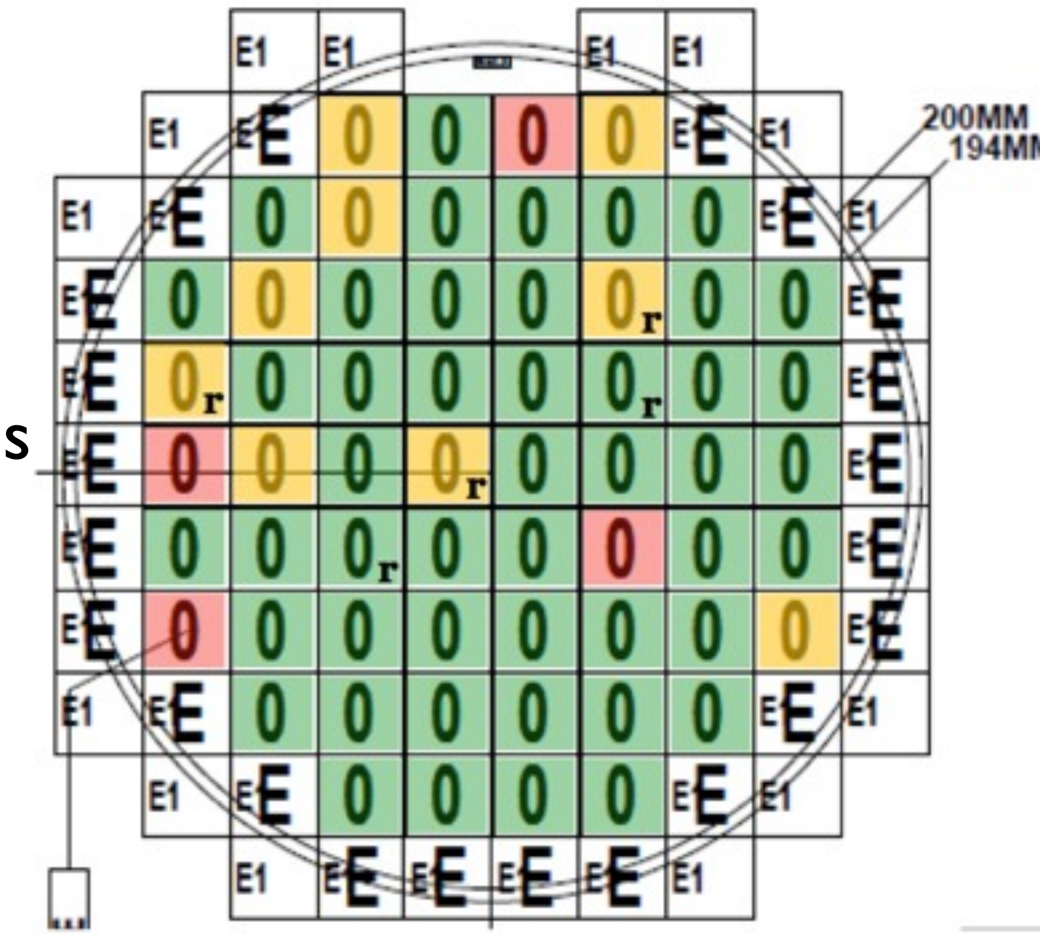
- FEI4 in IBM 130nm CMOS
  - array size: 80 (col) x 336 (row)
  - average hit rate at 1% inefficiency = 400 MHz/cm^2; max trigger rate: 200kHz
  - Fully qualified up to 250 Mrad (few samples irradiated to 750 Mrad and working!): after receiving 3x lifetime expected dose, some dead/noisy pixel were observed, most of which were recovered by retuning the FE
  - extensive use of *dual interlocked storage cells* (DICE) for critical configuration information. Tests performed at CERN PS w/ 24 GeV protons. The SEU cross-section of hardened cells are ~10^{-15} cm^{-2} per DICE bit



	FE-I3	FE-I4
Pixel size [μm^2]	50x400	50x250
Pixel array	18x160	80x336
Chip size [mm^2]	7.6x10.8	20x19
Active fraction	74%	89%
Analog current [μA/pix]	26	10
Digital current [μA/pix]	17	10
Analog Voltage [V]	1.6	1.4
Digital Voltage [V]	2.0	1.2
Total power [μW/pix]	75	26
Pseudo-LVDS out [Mb/s]	40	160

FEI4 pre-production

- FEI4-A wafers received in late 2010 and used as first chip-test, IBL module prototyping and sensor/ module qualification throughout all 2011/2012
    - the first fully integrated chip was a big success
    - demonstrated good analog behavior with several different sensor technologies (silicon planar/3d and pCVD diamond)
    - demonstrated digital functionality needed for IBL
- Good chip yield approx ⅔ (i.e. ~40/wafer)
- Demonstrated bump-bonding on very large & thin chip at IZM
- Built first IBL modules with full IBL specs !



Based on the prototype studied, minor design changes was implemented for the production FE iteration (FEI4-B)

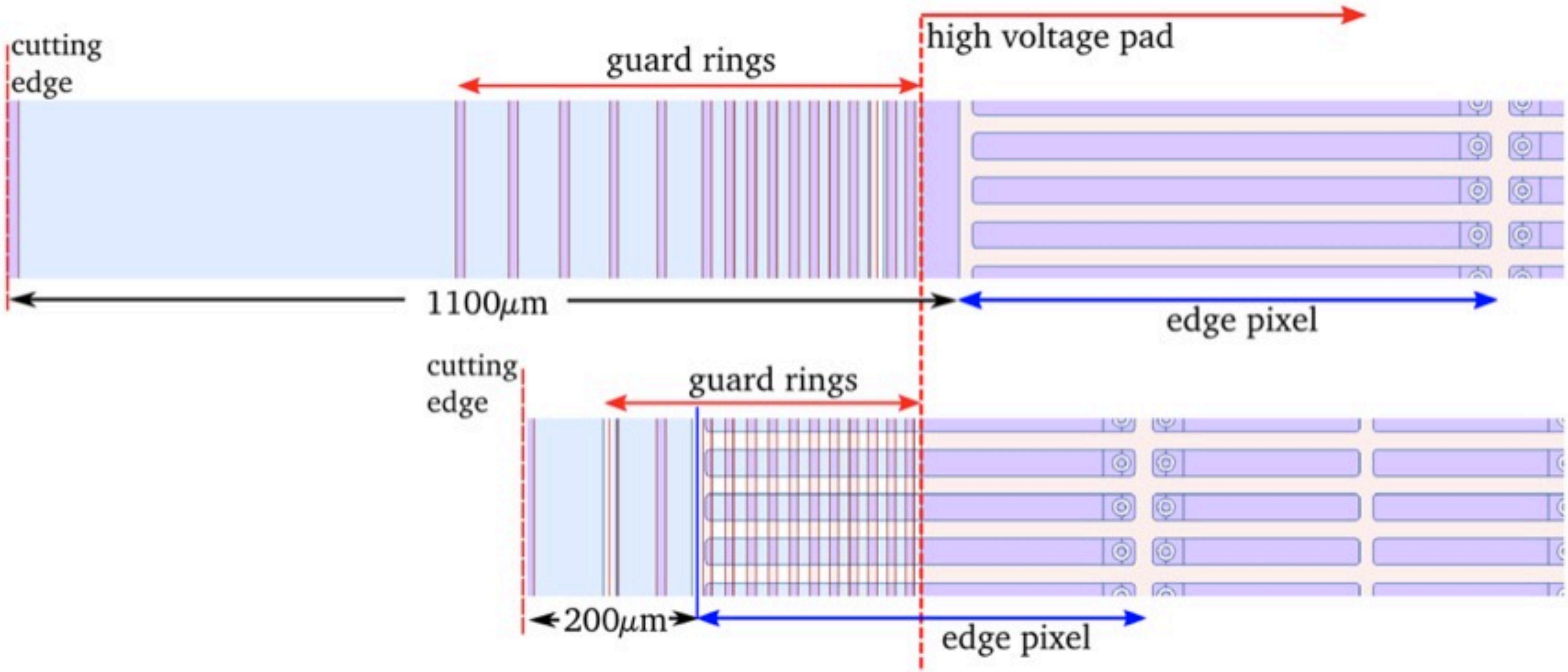
FEI4 production

- Two fabrication runs: Engineering & Production
  - a change was made to one via mask for production run, to patch an ESD protection deficiency in the digital voltage regulator
- Scale of the production: a total of 134 FEI4-B wafers have been purchased & received !!!
  - at 60% yield, that amounts to 1.6m^2 of detector grade active area. This is the same active area as the present pixel detector, and nearly as many channels as ATLAS and CMS combined

The IBL sensor technologies

- Several promising new sensor technologies have been developed so far:
  - Planar n-in-n and n-in-p
  - 3D full & active-edge and double-side & slim-edge
  - pCVD diamond
- Because of the tigh IBL construction schedule, the slime-edge *Planar n-in-n* and the *3D double-side* silicon technologies have been retained for prototyping with the FEI4 in view of the IBL construction
  - pCVD is employed for ATLAS DBM (no covered in this talk)

The IBL Planar n-in-n



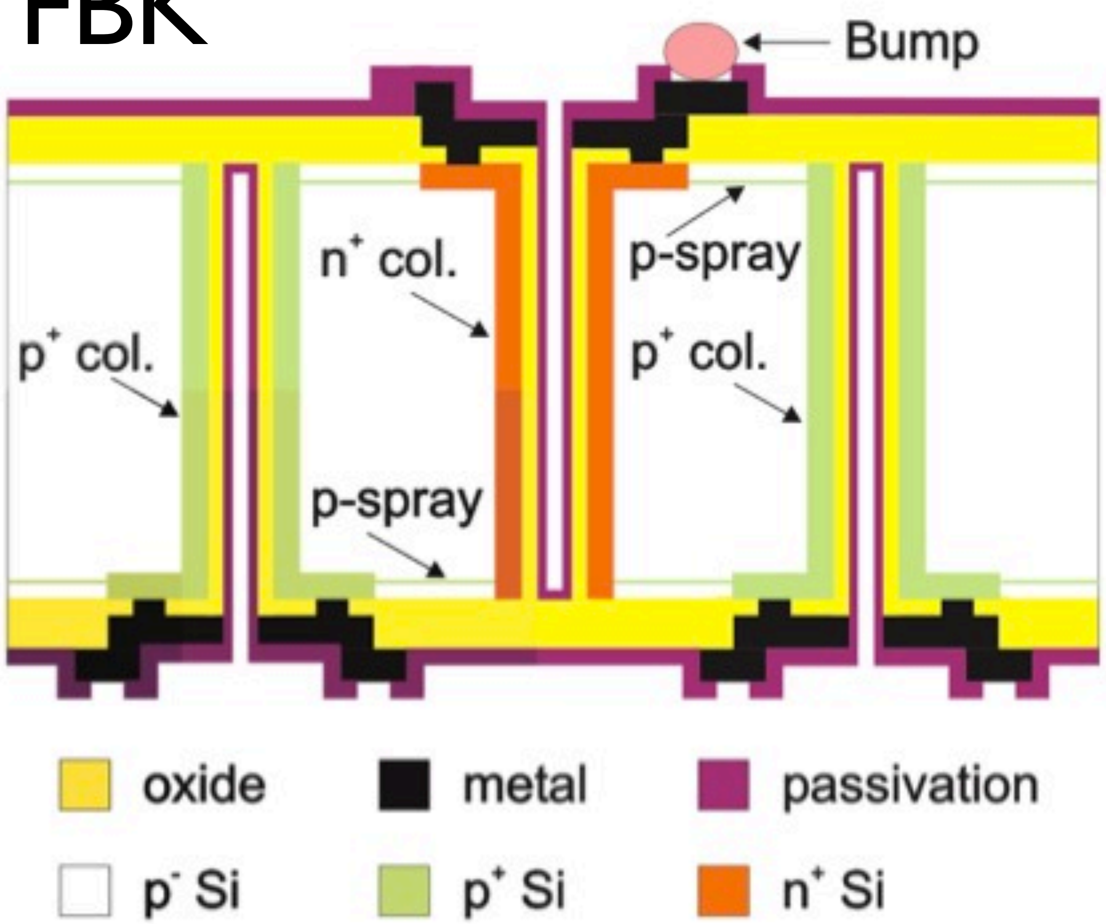
Present Pixel

IBL-like

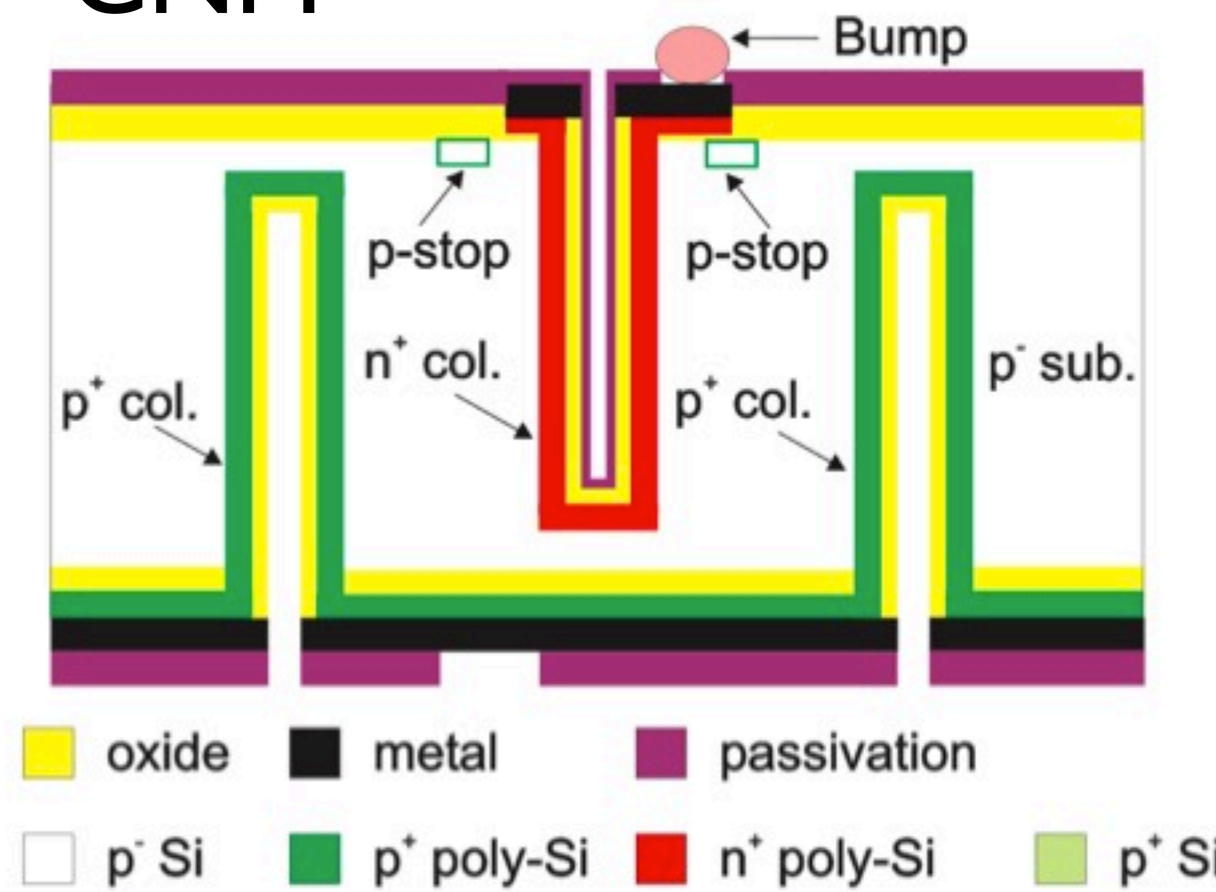
- 200 um thick oxigenated n^+-in-n planar sensor
- inactive edge minimized by shifting guard-rings (13) underneath active pixel region
- manufactured at CiS as the present Pixel sensor

The IBL 3D n-in-p

FBK



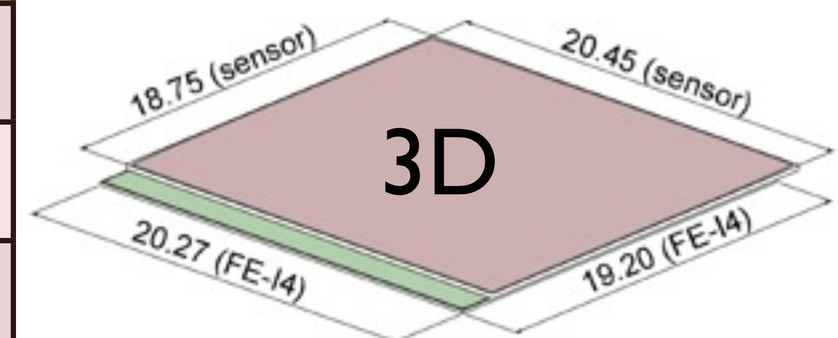
CNM

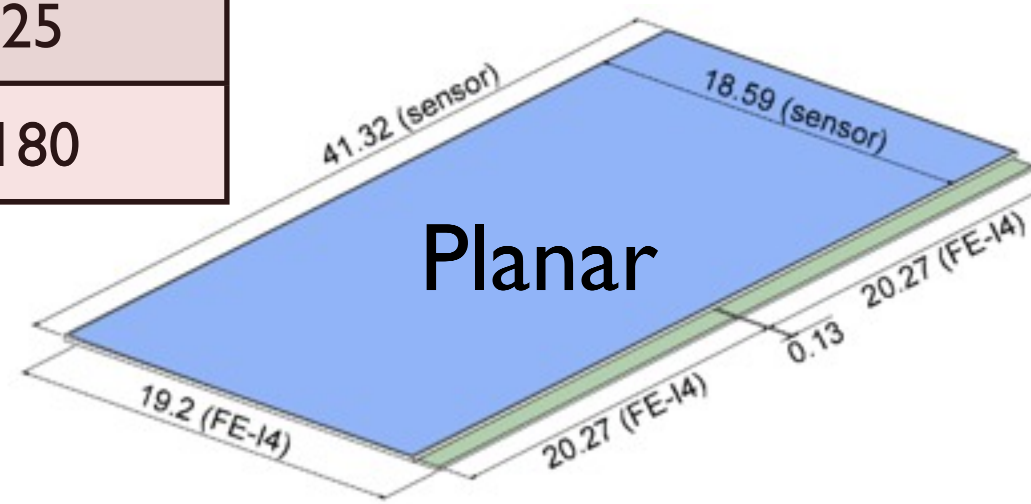


- 230 um thick 3D p-type sensors
- column through ~full bulk with two electrodes per pixel (so called: 2E-type)
- depletion horizontally (short depletion width leads to low bias voltages)
- manufactured at FBK and CNM

The IBL sensors specs

	Planar	3D
Active size W x L [mm^2]	16.8 x 40.9	16.8 x 20.0
Total size W x L [mm^2]	18.59 x 41.32	18.75 x 20.45
Thickness [mm]	0.20	0.23
Typical deplation voltage [V]	< 35	< 15
Typical initial operation voltage [V]	60 (V_{dep} + 30V)	25
At of at end of lifetime [V]	1000	180





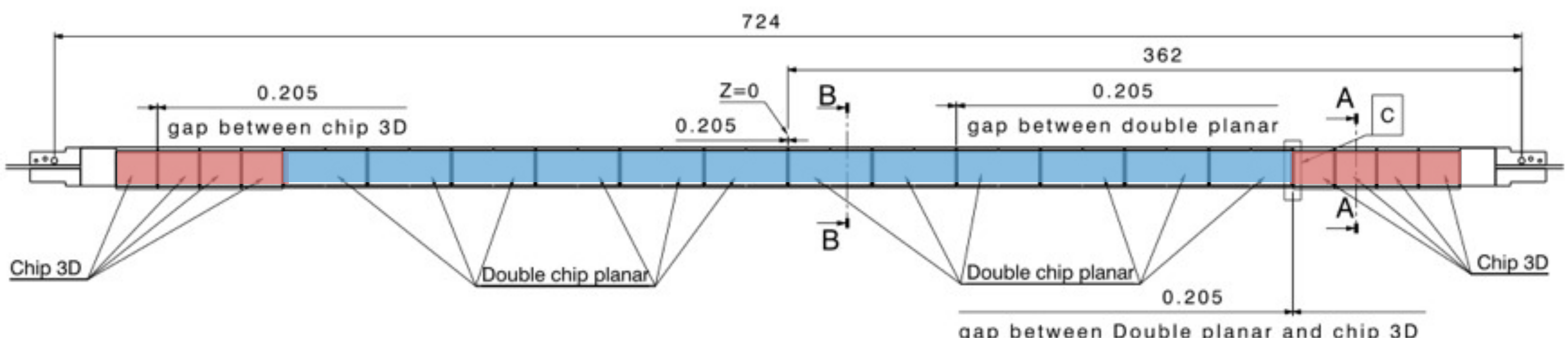
- Sensors specification for IBL
  - qualify to 5×10^{15} n_{eq} cm^{-2}
  - sensor max power dissipation: 200 mW/cm^2 at -15 °C
  - single-hit efficiency > 97%

Module production for IBL

- IBL will build ~2x number of installed modules
- ATLAS Pixel extended Institute Board endorsed the recommendation of the review pannel (July 2011):
  - produce enough Planar sensors to build 100% of the IBL
  - produce 3D sensor to build of 25% of the IBL

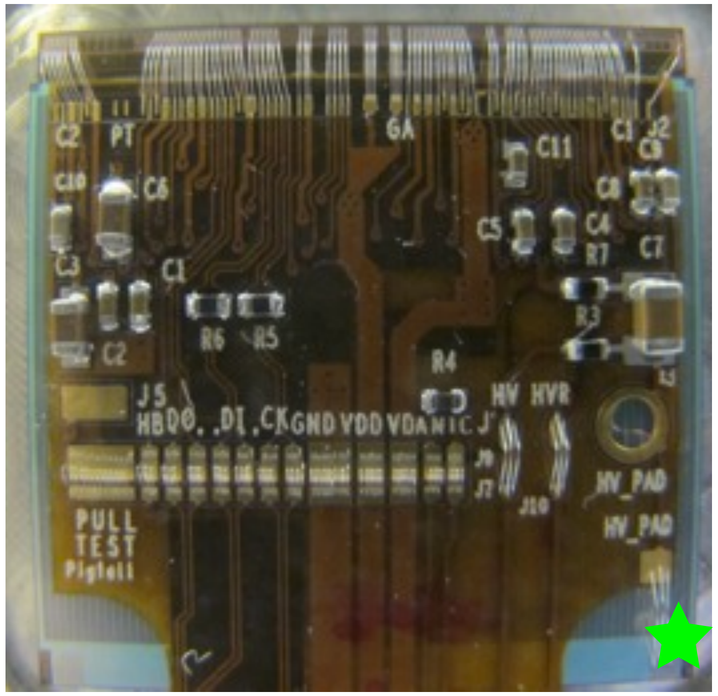
→ Sensor productions completed for both sensor technologies

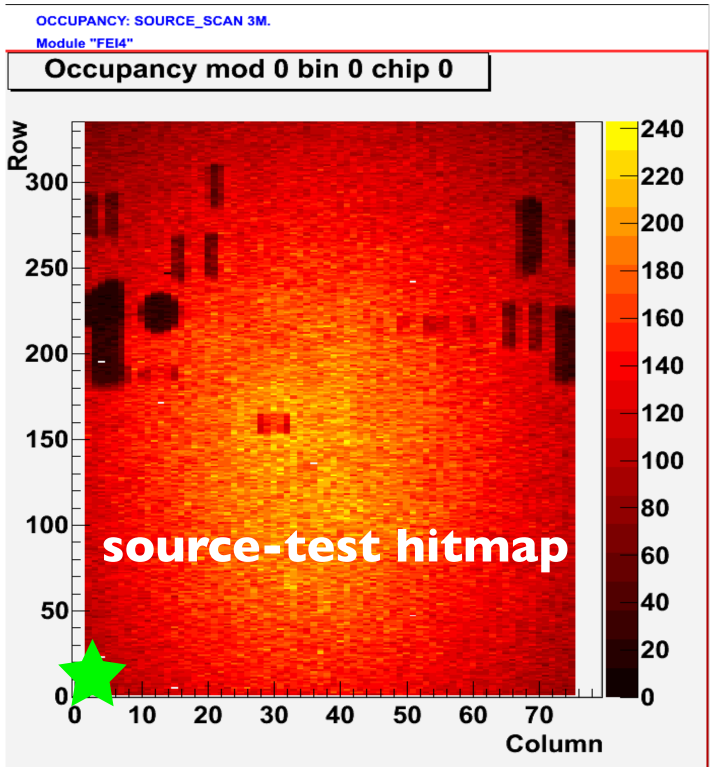
Mixed scenario : Planar (75%) and 3D (25%)

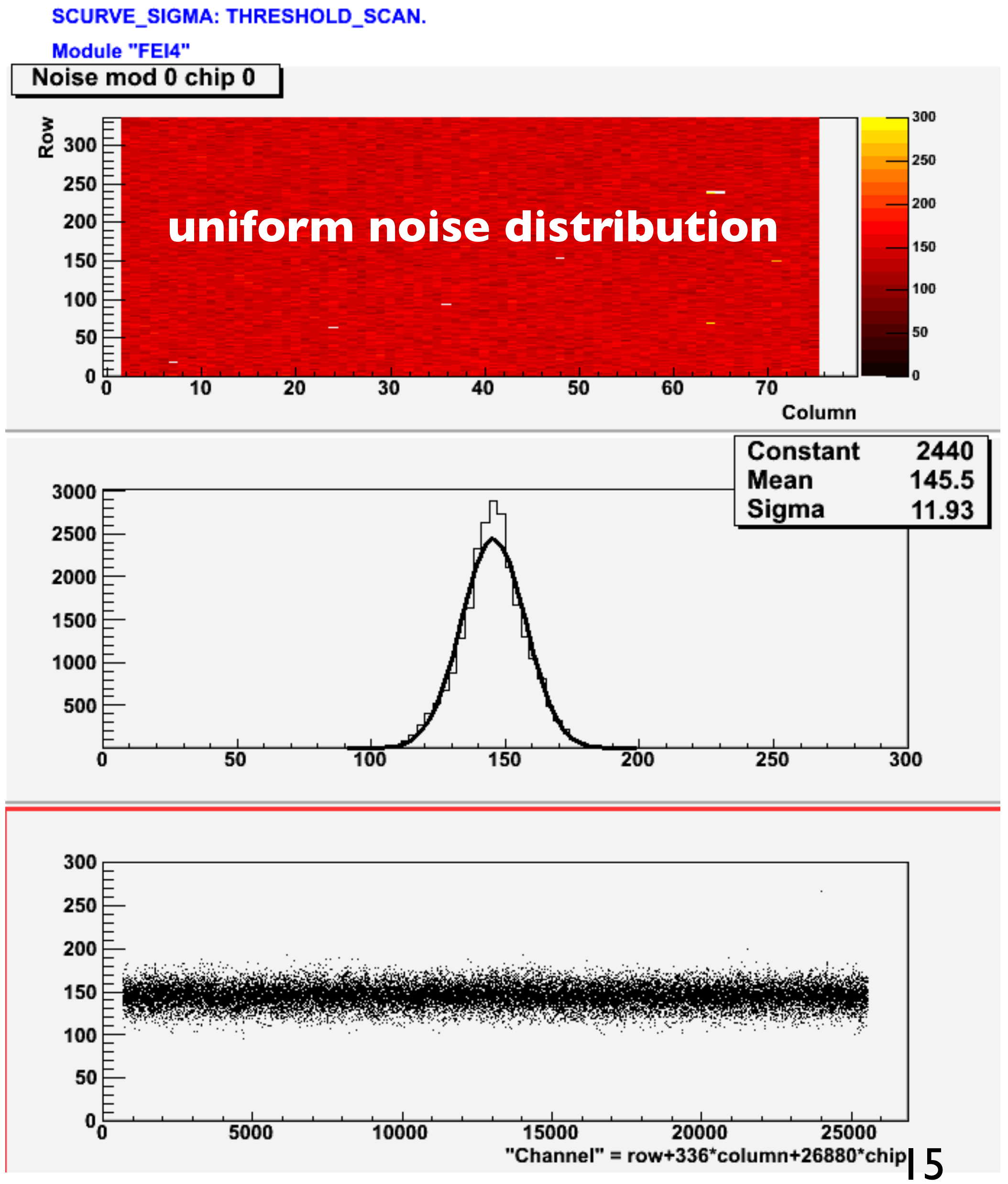


Fully assembled module

- Finished successfully pre-production equipped with FEI4-A&B
  - test final module design
  - prepare and test assembly and QA procedure
  - lab-tests with calibration, Am241 and Sr90
  - good performance so far
- Started production equipped with FEI4-B

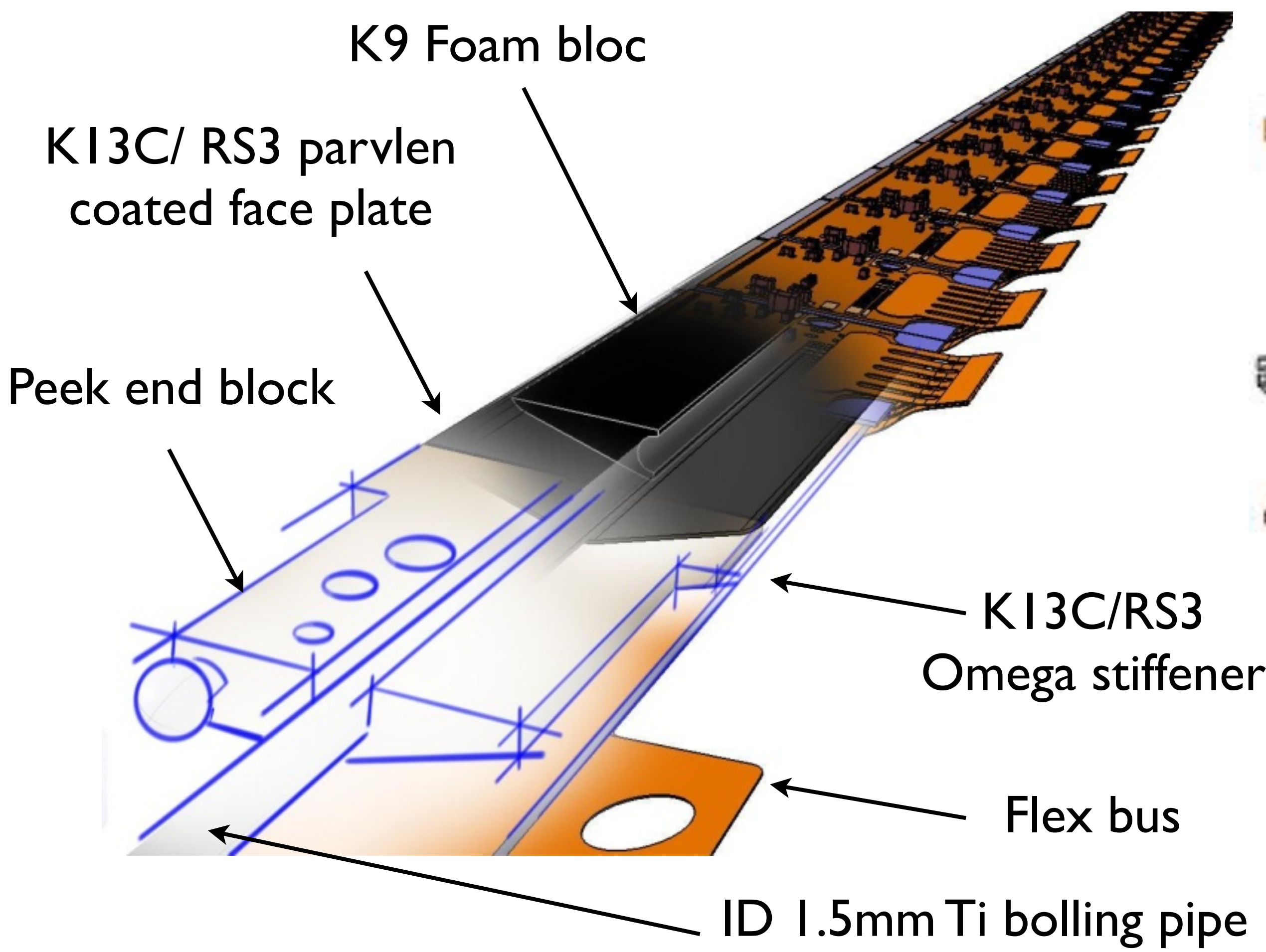


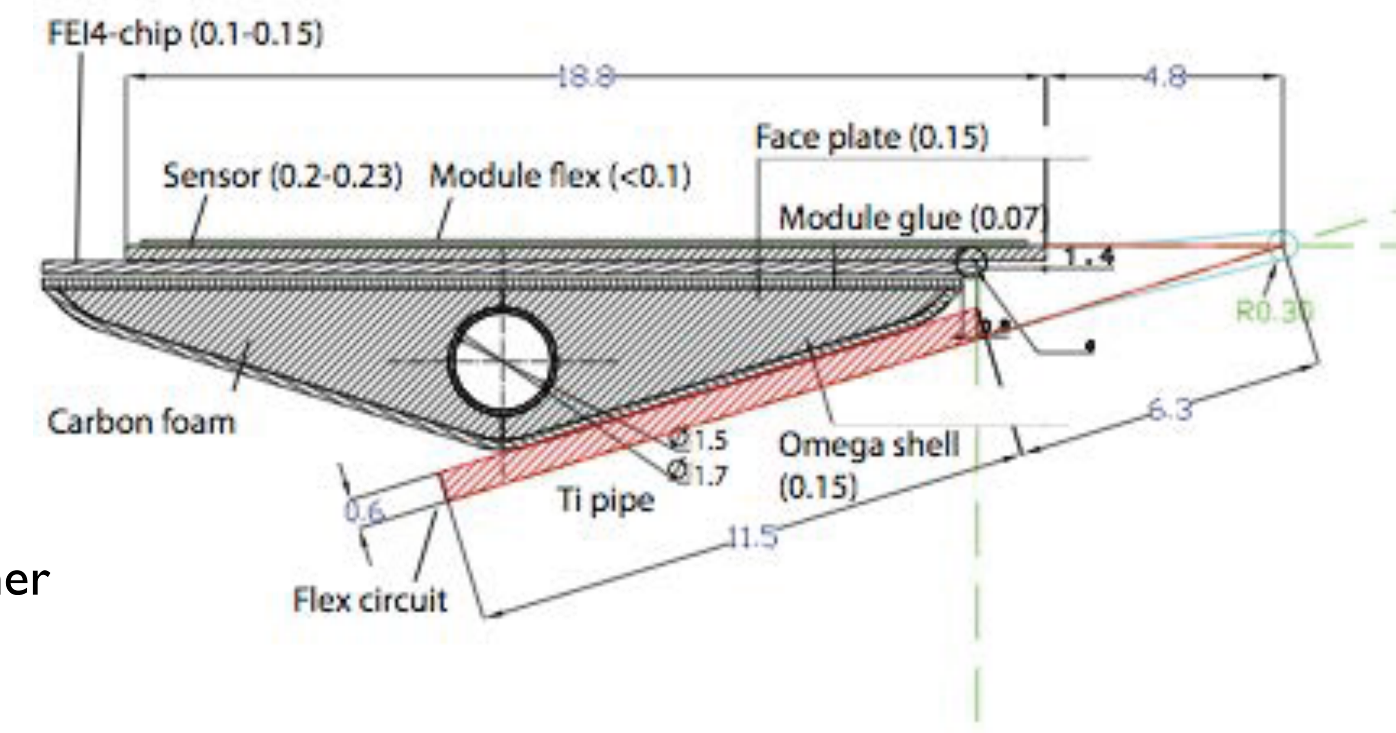




Local support - *Stave*

- Carbon-fiber support structure with minimal material budget X/X_0 ~0.6% for support and cooling
- Optimized stiffness and thermal conductivity
- Match thermal expansion
- Material qualification for use in high-radiation environments (300 Mrad)
- Detector cooling with a CO_2 system working -40°C to minimize the leakage current of the sensors

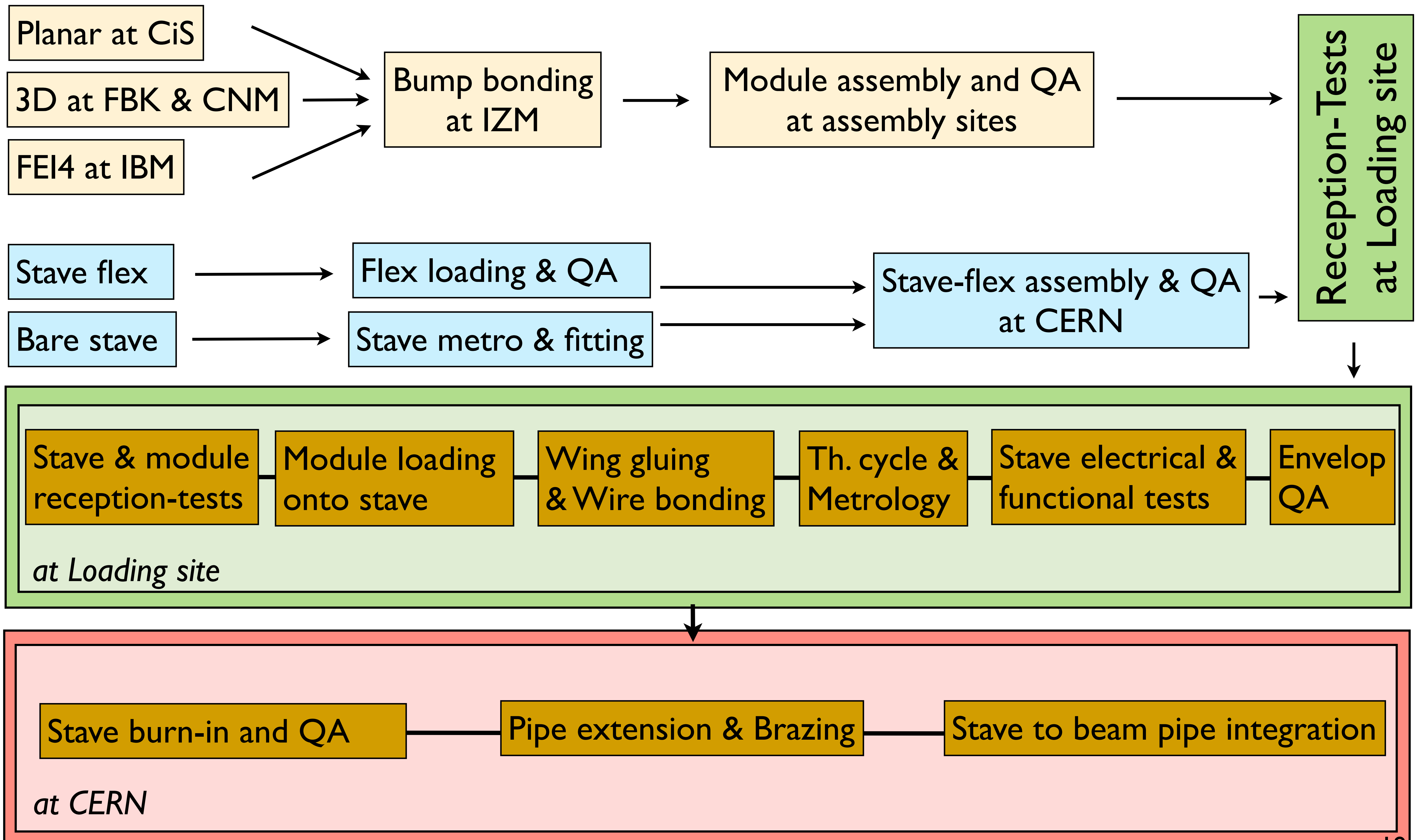




IBL Stave prototypes

- Loaded 3x prototypes and 1x production staves so far:
  - Stave -1: equipped with prototype flex, digital modules (dummy sensors + FEI4-A), temporary services.
  - Stave 0-A: as close as possible to production stave scenario, equipped with real modules with FEI4-A on board.
  - Stave 0-B: very close to the production stave, equipped with real modules with FEI4-B on board.
  - *Stave 1: production stave under loading ...*

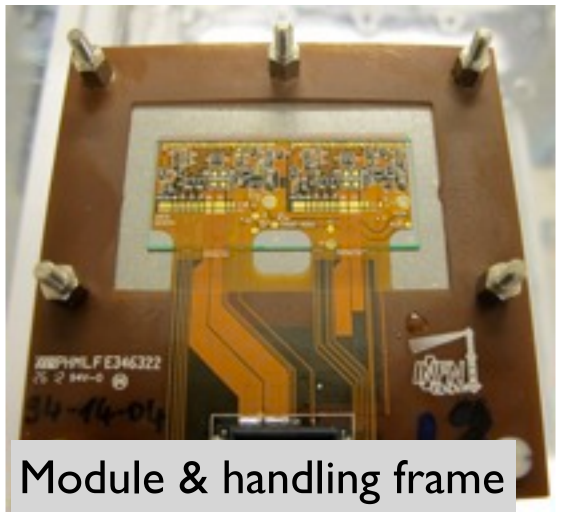
Production flow overview



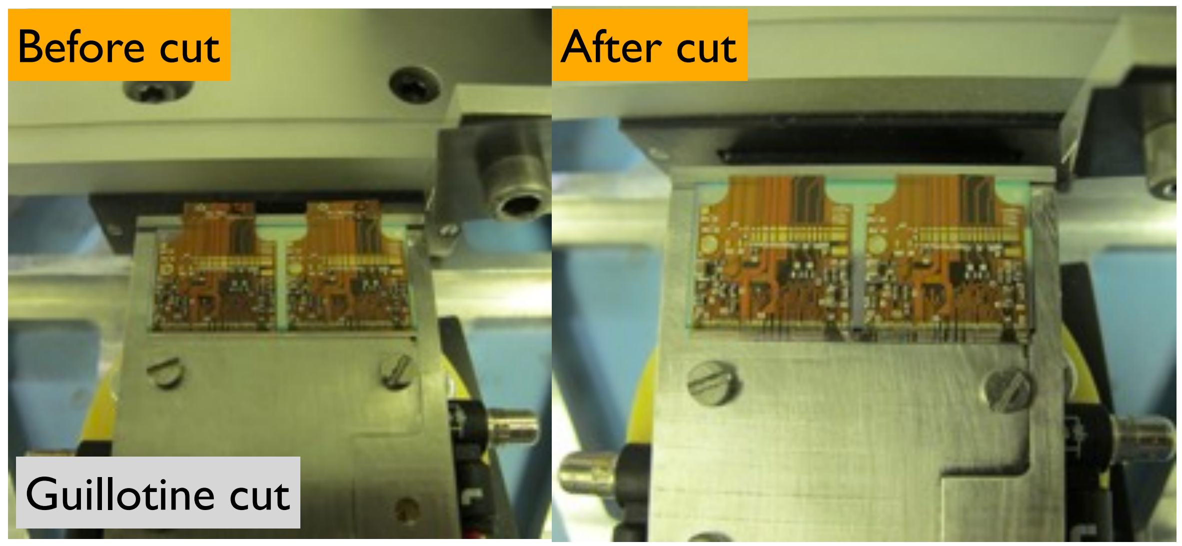
Loading procedure

1. Module reception-tests & module selection
2. Stave inspection, metrology, thermal cycling, metrology
3. Loading - one side after the other
4. Wing attachment
5. HV insulation insertion + spacer for wire bonding protection
6. Wire bonding and pull test
7. Stave electrical/functional tests one side after the other
8. Metrology survey
9. Thermal cycling
10. Metrology survey
11. Final stave electrical/functional tests
12. Stave envelope check
13. Shipment to CERN for QA & Integration

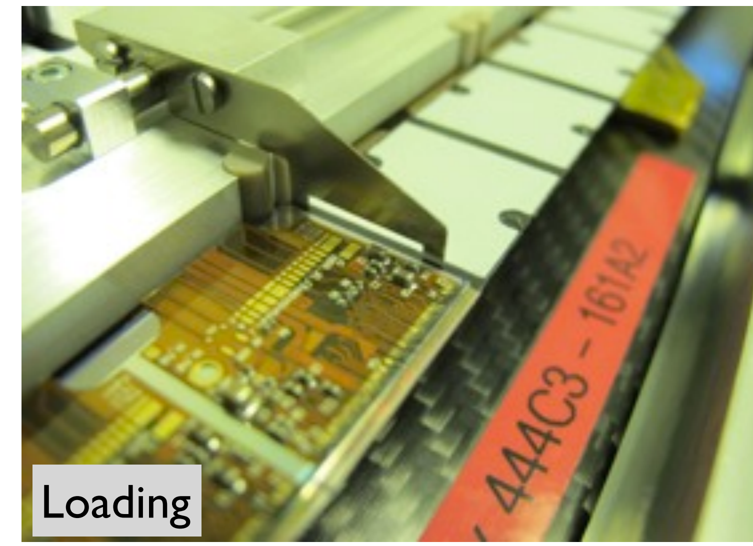
Loading procedure



Module & handling frame



Guillotine cut



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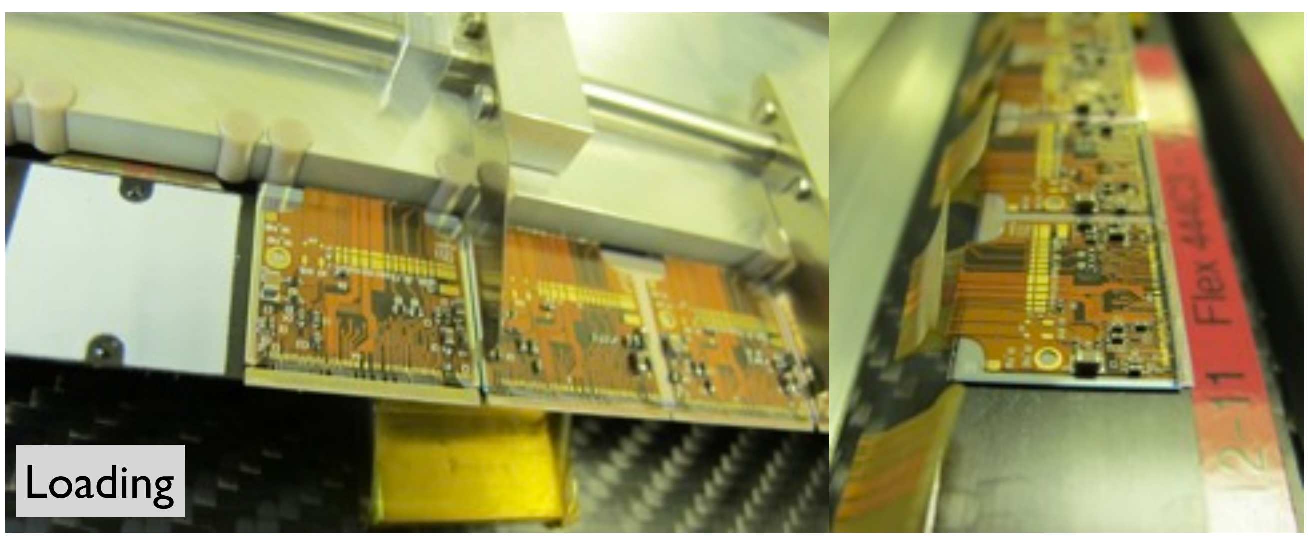

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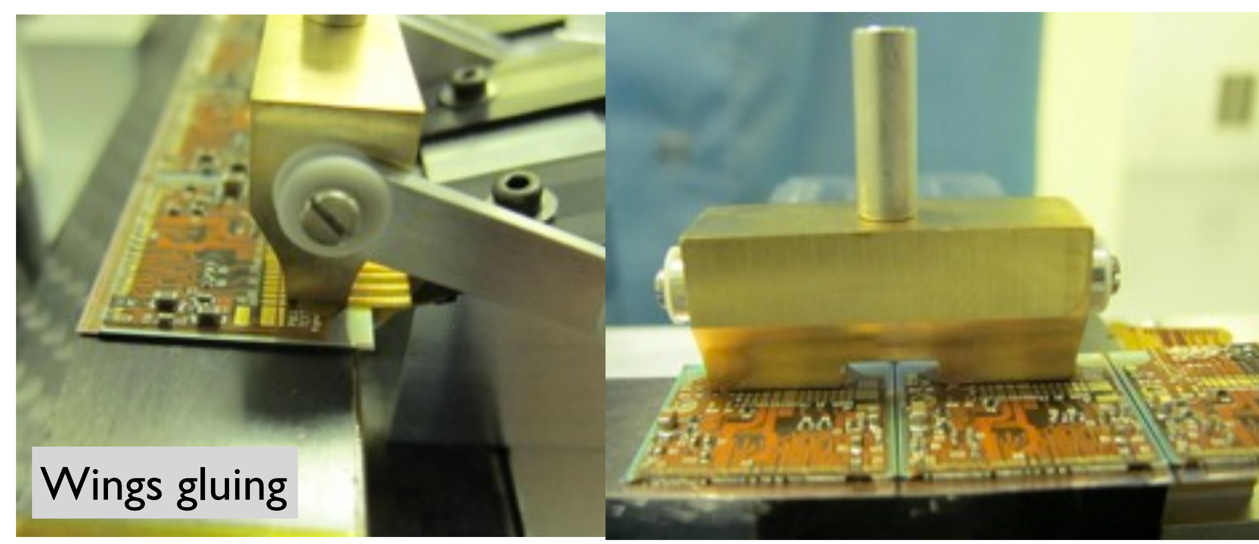
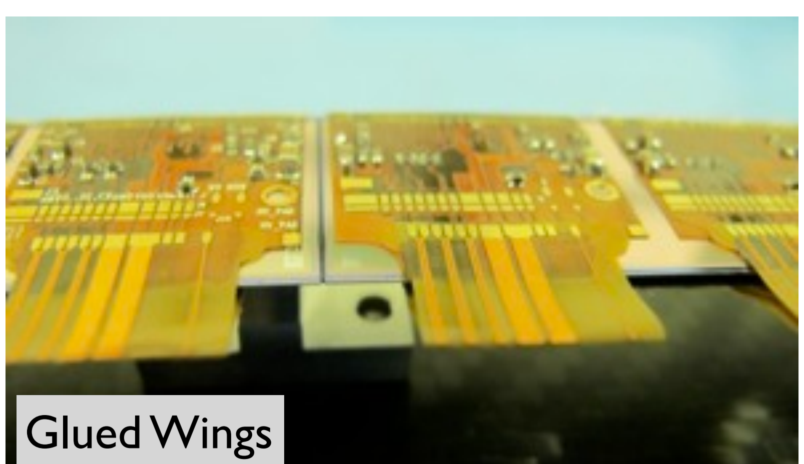
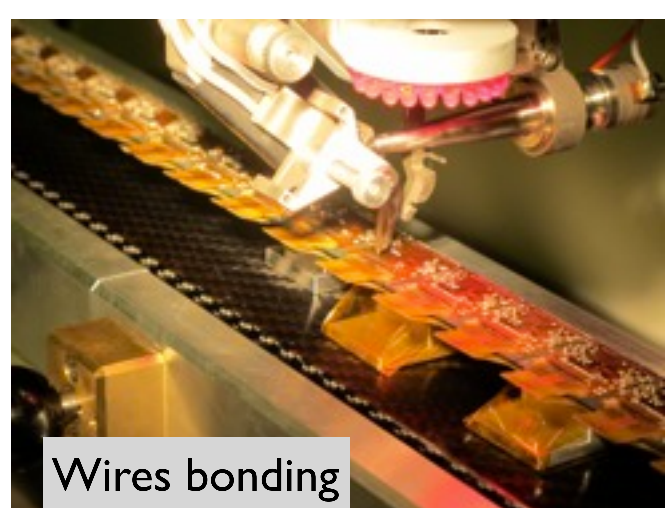


Wings gluing



Glued Wings

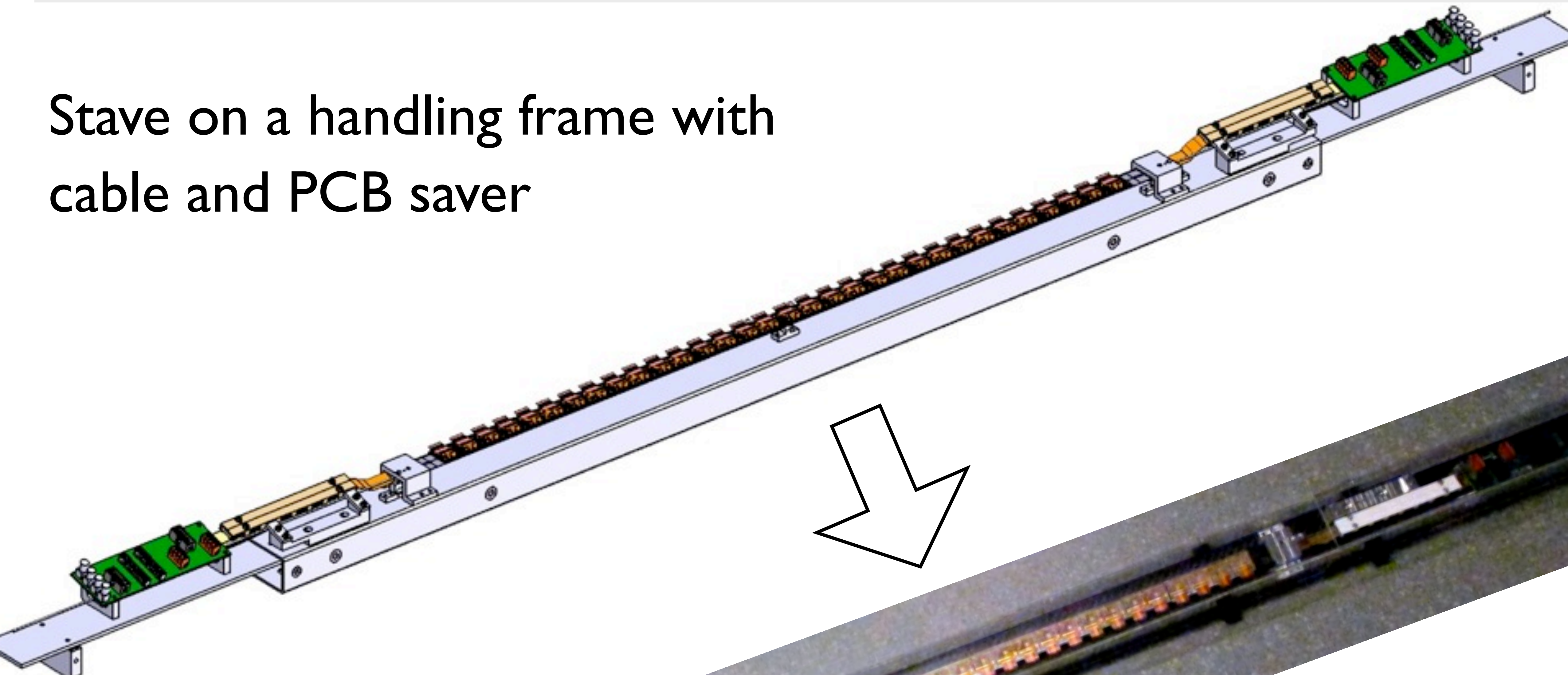


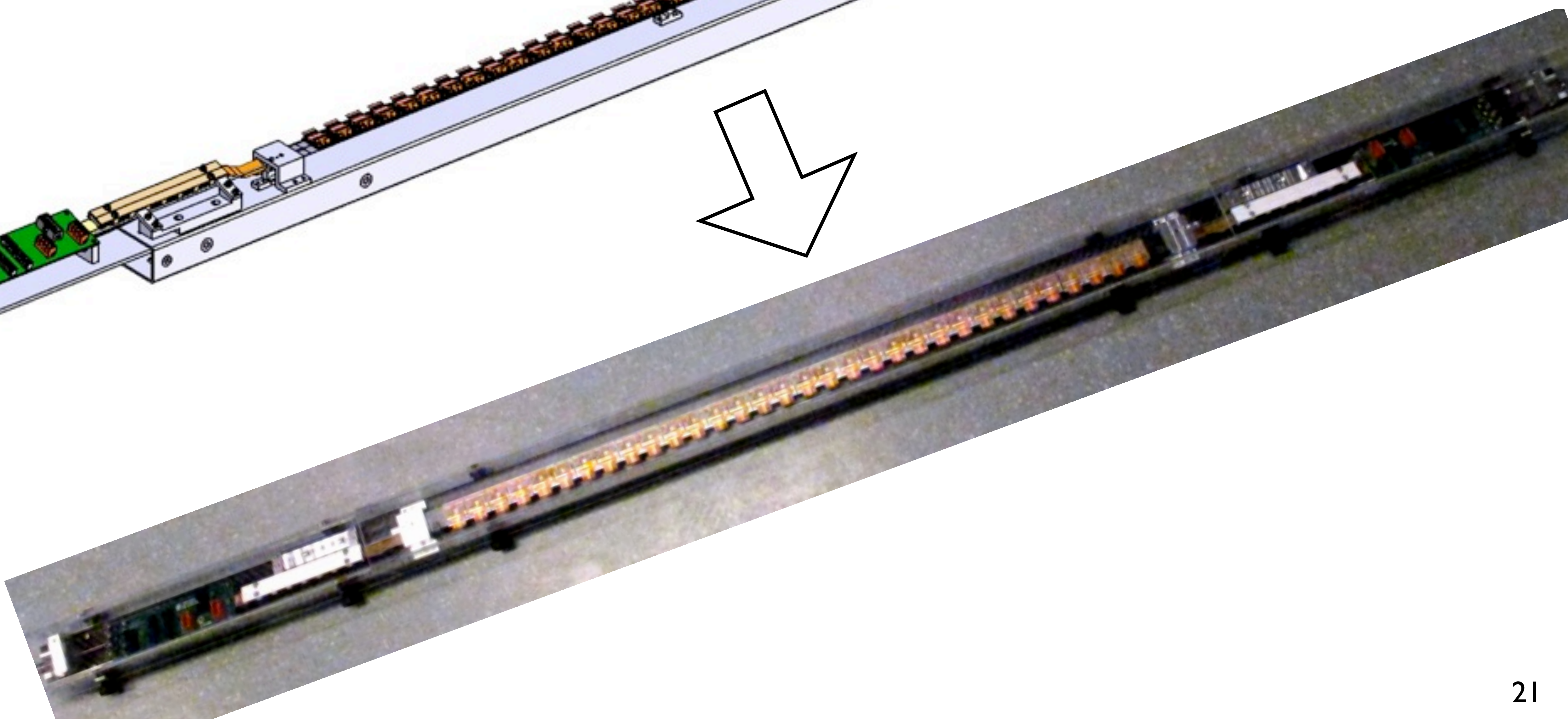
Wires bonding

Pull test

The Stave prototype

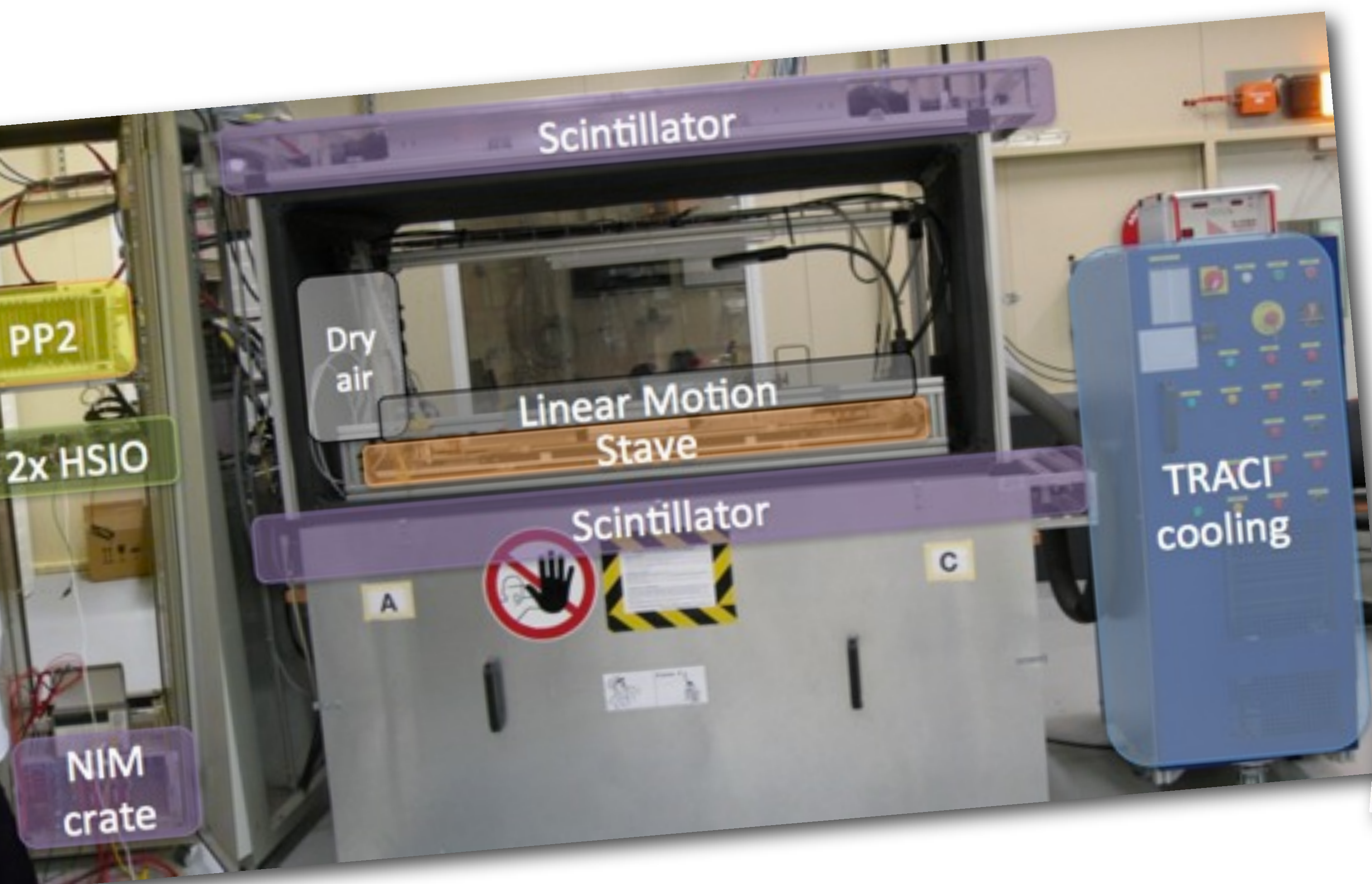
Stave on a handling frame with cable and PCB saver

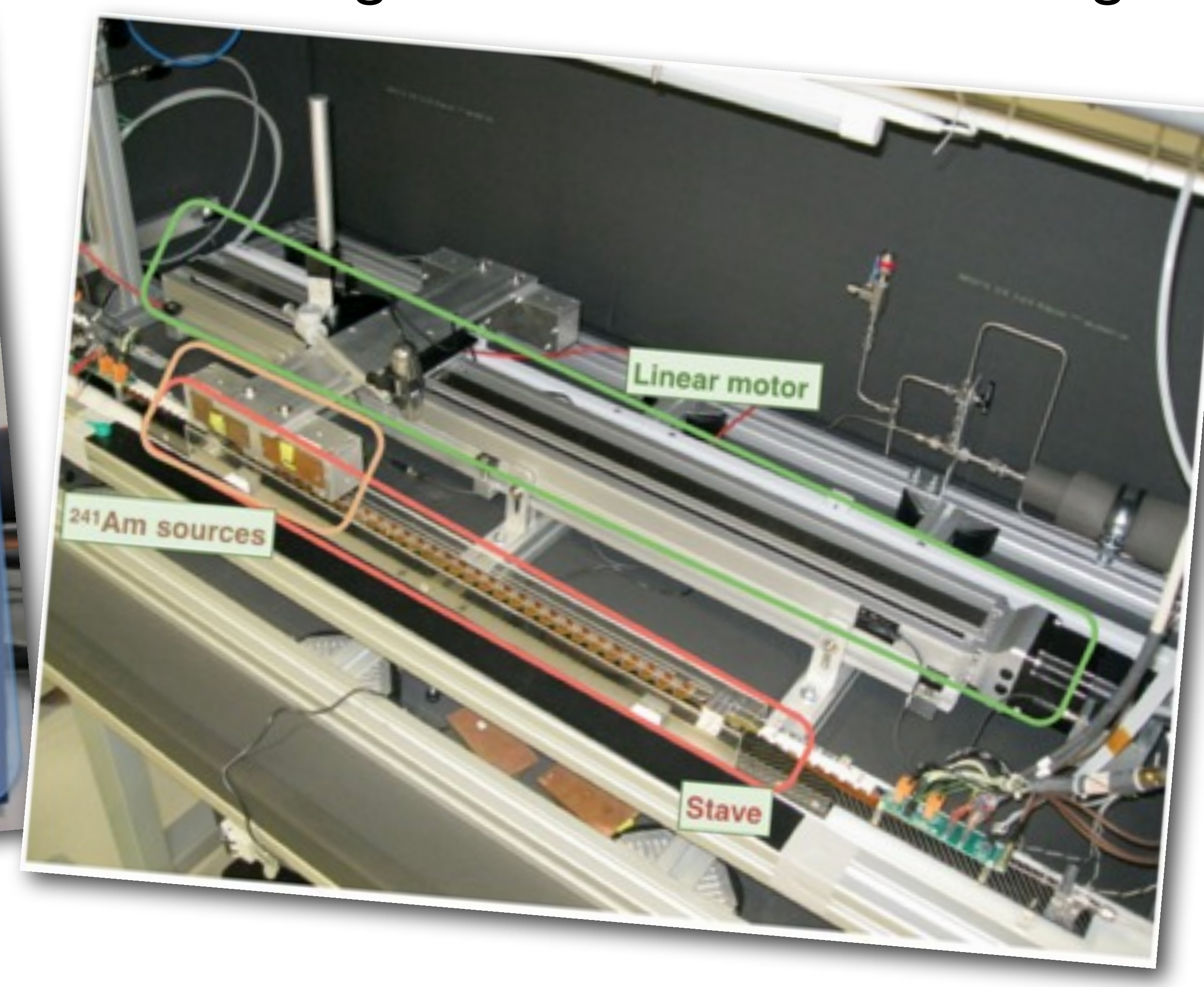




Stave System-test and QA

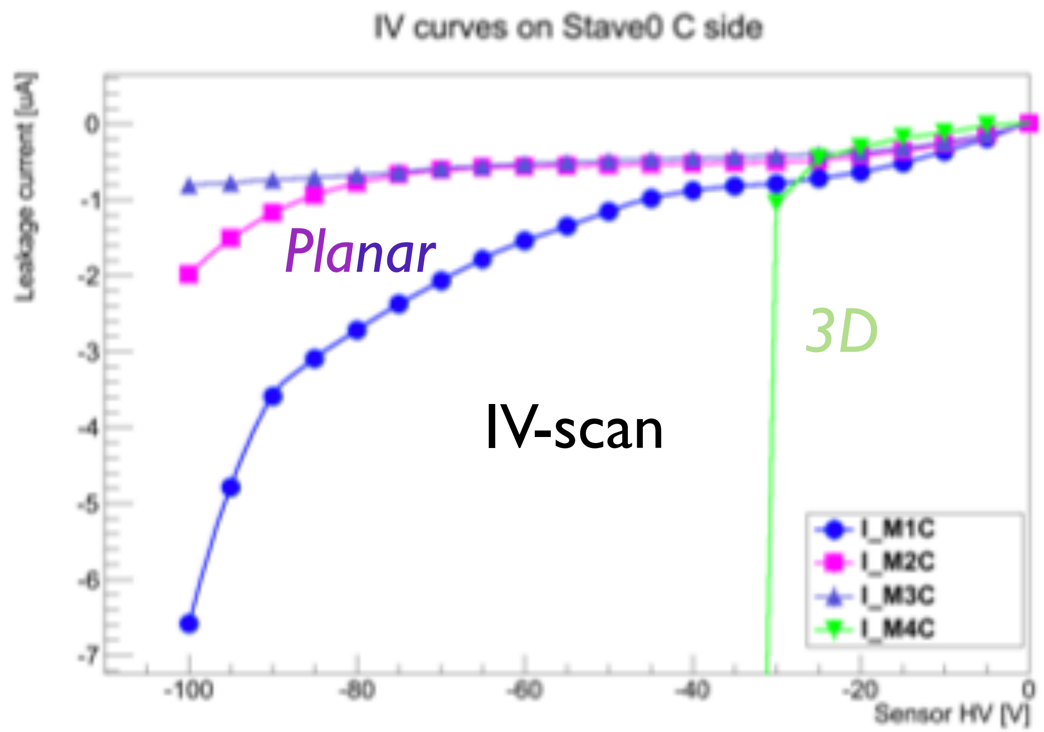
- Two systems (based on CO_2 cooling plant):
  - one at Loading site for Stave QC
  - one at CERN ALTAS Cleanroom (SR1) for long-term QA and source-tests
    - stave-setup equipped for running two stave-tests in parallel
    - includes 2x Am241 and 1x Sr90 sources on linear stages with automated scanning

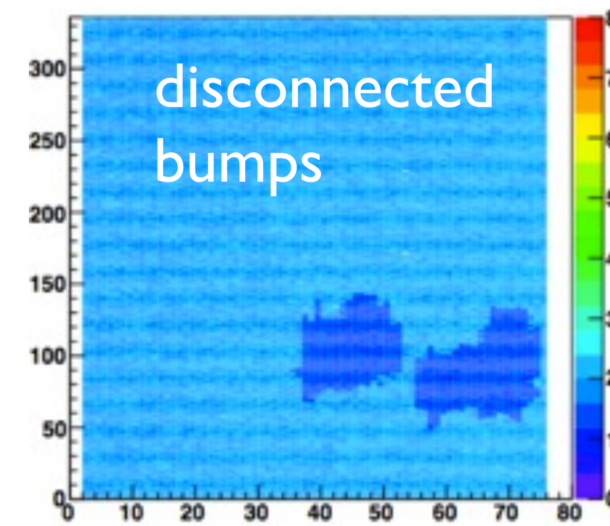




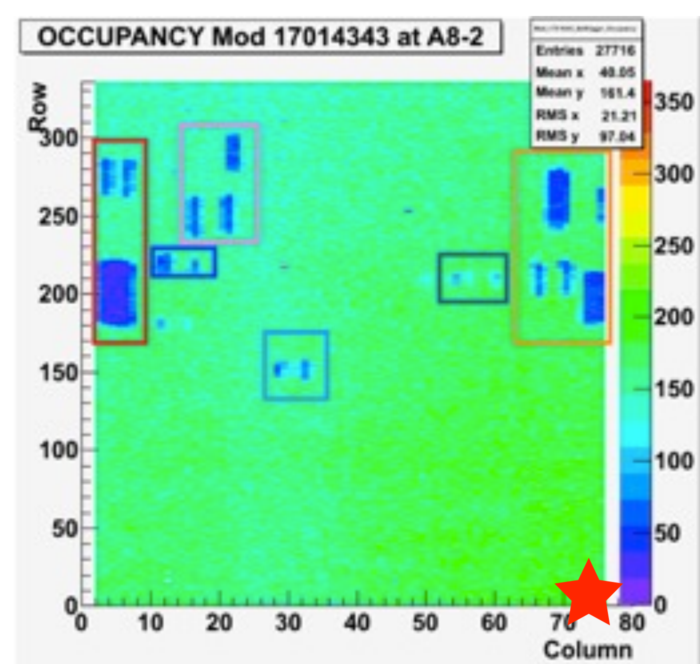
Stave prototype: test-results

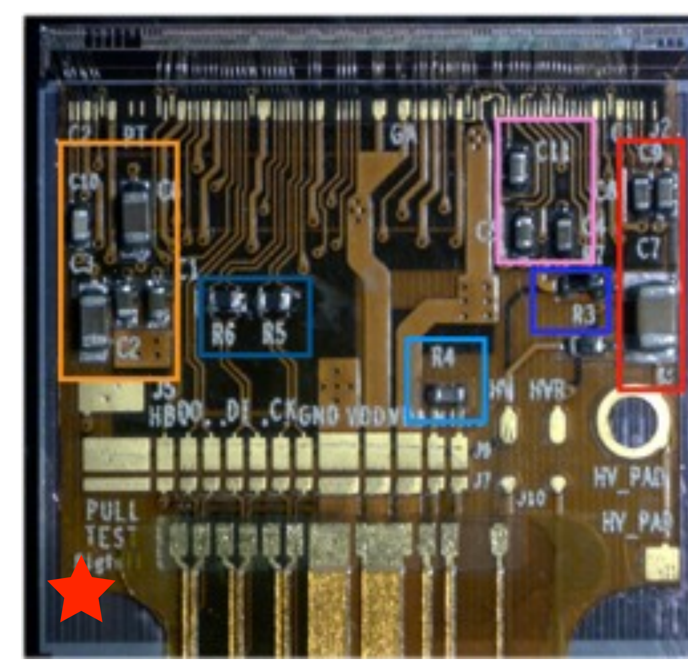
- Several systematic (system-related) tests:
  - tuning at different threshold, gain, supply voltages
  - test of all modules IV
  - test of noise
  - LVDS signal transmission and power studies
  - source-tests of modules
  - cross-talk
  - test for merged and disconnected bumps





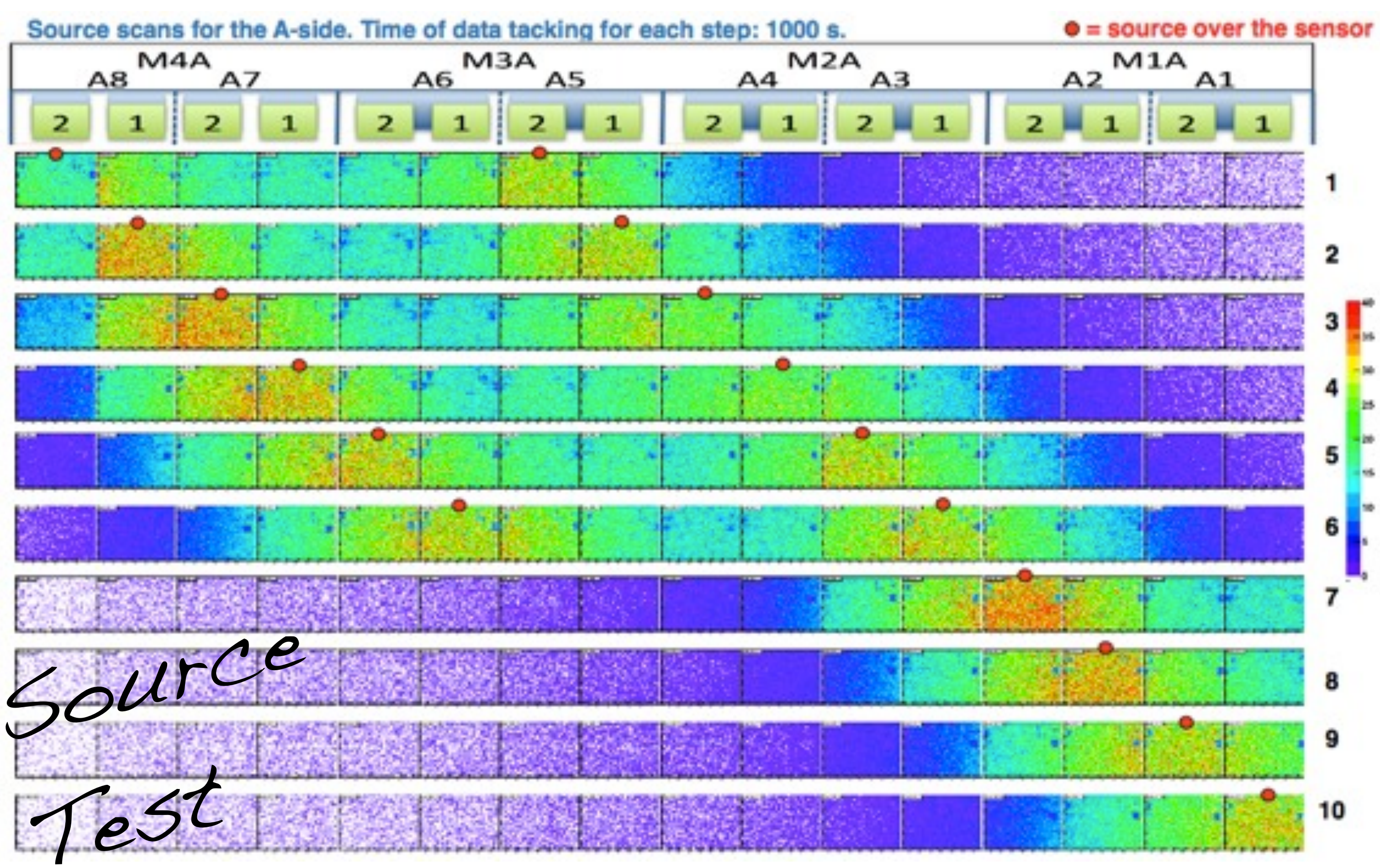
Am241 source-tests

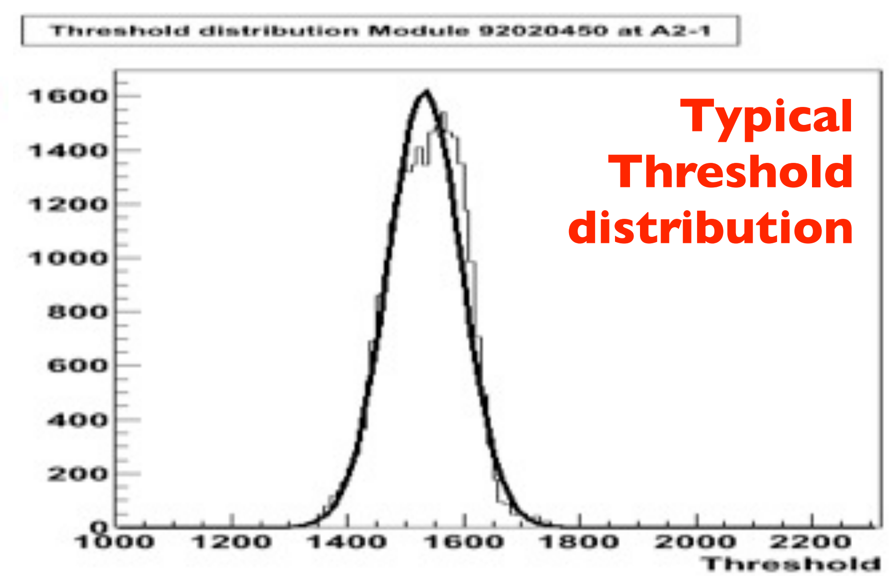


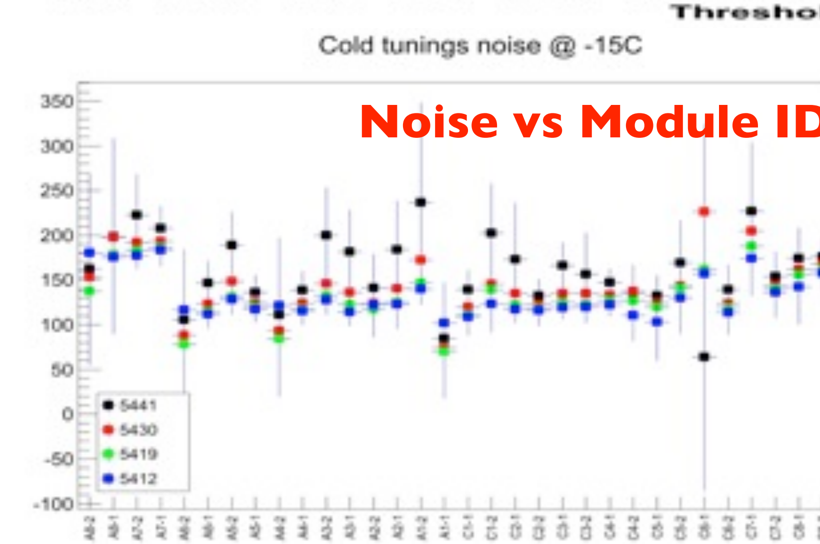


Stave prototype: test-results

- General stave works in calibration and source scans
- All modules functional
- Operational threshold of 3000e with typical noise of 140e-160e
  - ***found minimal threshold in cold stave tests of 1500e***



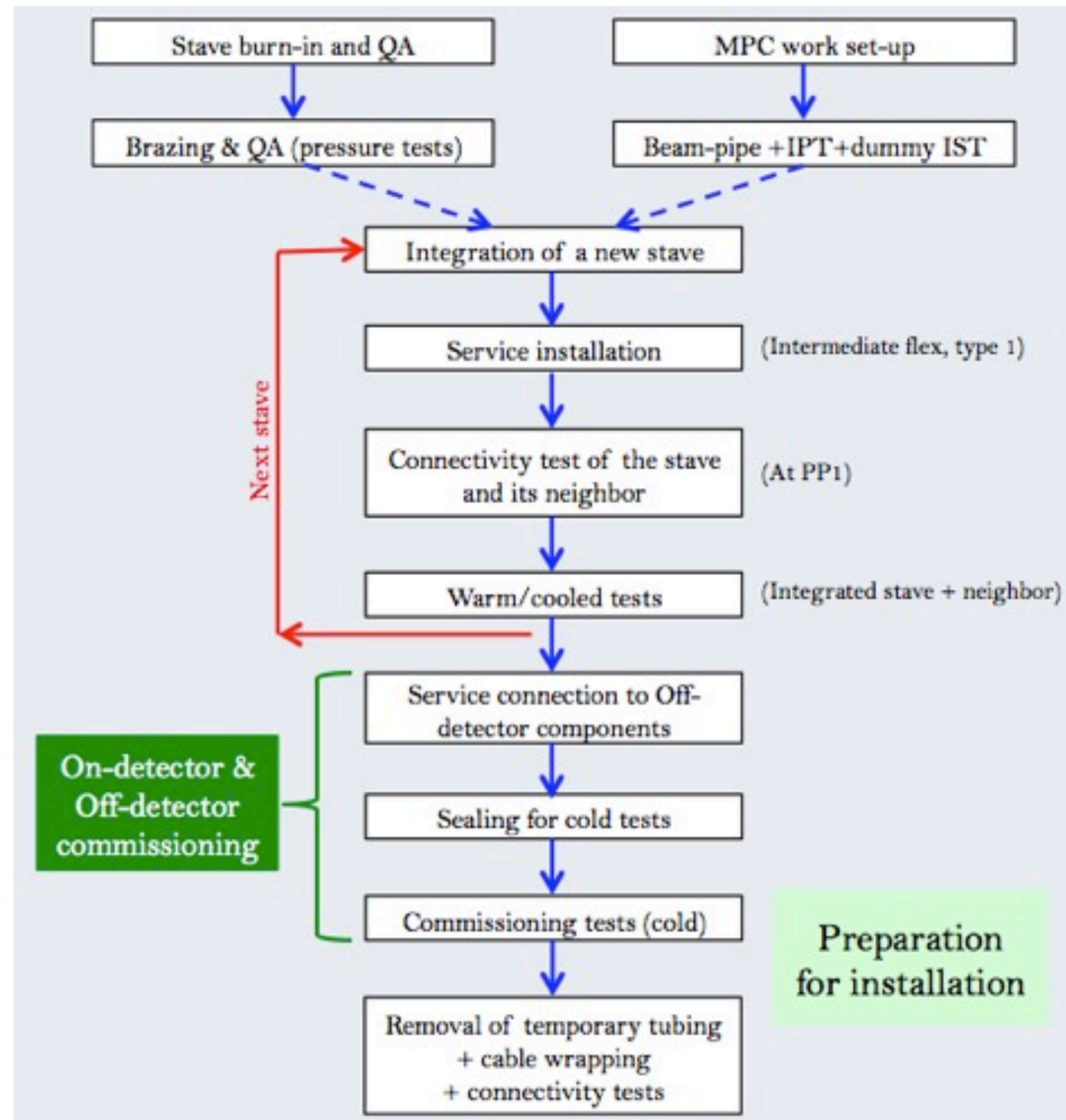




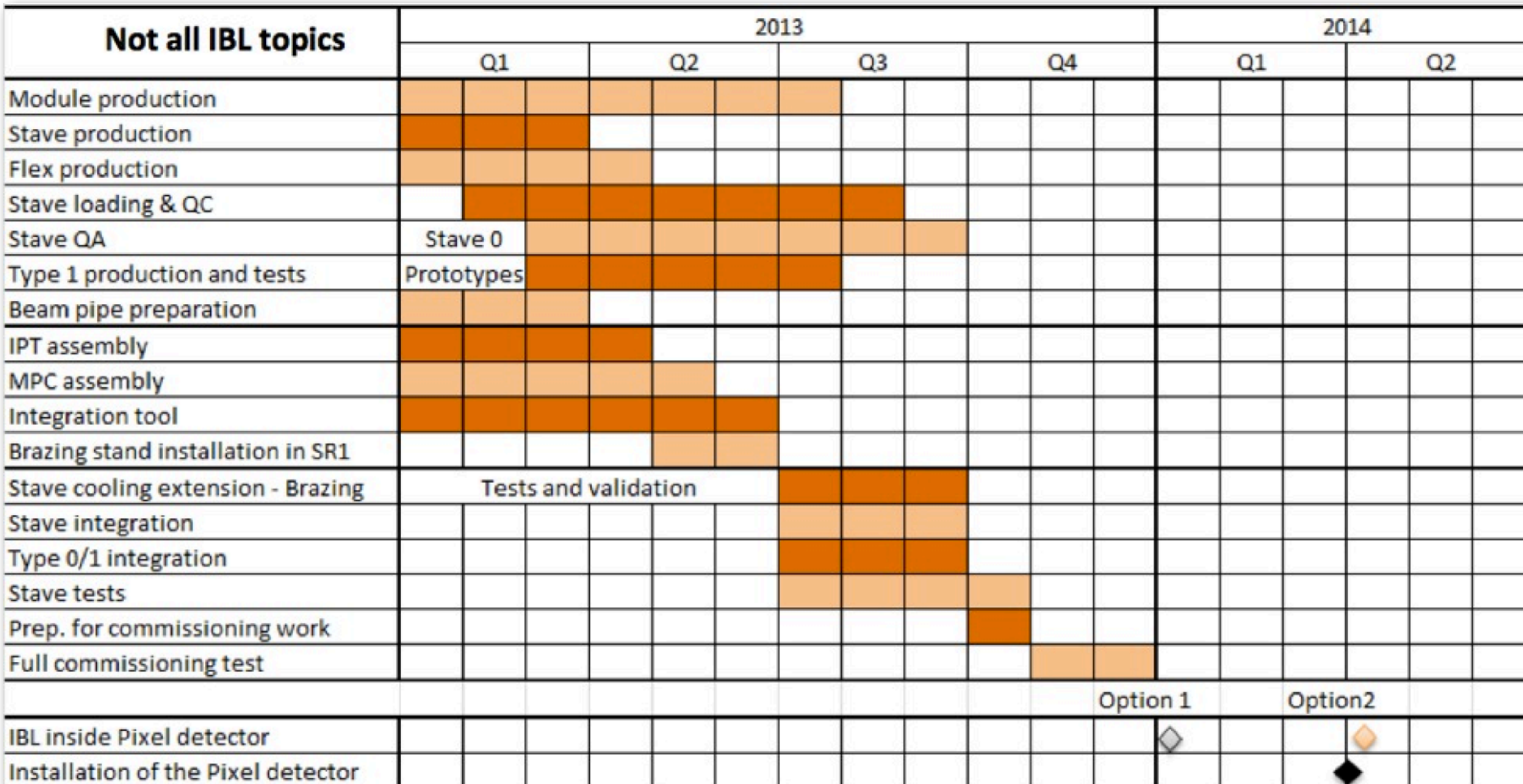
Stave Testing & Integration

- Integrate all 14 staves onto beam-pipe
  - including services
  - dedicated brazing stand
  - Multi-purpose container (MPC) for precision stave loading
- Commissioning each stave before integration (stave testing stand), and after with each integration
- Full 4th layer On and Off detector commissioning after all staves integrated

To repeat 14 times



IBL schedule overview



D. Ferrere, Pixel Week (12/2/2013)

Summary

- The FEI4 readout chip is qualified and delivered
- Planar n-in-n and 3D are qualified and manufactured
- Module hybridization is in production
- Mechanics and service are qualified and in production
- Evaluation of pre-production staves done
- Assembly stave production started

References

- *ATLAS Insertable B-Layer Technical Design Report.* CERN-LHCC-2010-013
- *ATLAS Insertable B-Layer Technical Design Report Addendum.* CERN-LHCC-2012-009
- *Prototype ATLAS IBL Modules using the FE-I4A Front-End Readout Chip.* JINST (2012) 7 P11010.