

Fabrication of new p-type pixel strip detectors with enhanced multiplication effect in the n-type electrodes

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Mask set Technological simulation Electrical simulation for FZ Conclusions

Motivation

- 1. Thin p-type epitaxial substrates
- 2. Low gain avalanche detectors



Old results: Simulation of the electric field

Standard strip



Strip with P-type diffusion



Strip with P-type diffusion: 2D and 1D doping profiles





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Simulation of the electric field: Curves at 500V

No irradiated



- Standard strip: Electric field strength at the junction increases after irradiation
- Strip with P-type diffusion: electric field strength at the junction is held after irradiation

Irradiated $\phi_{\it eq} = 1 \cdot 10^{16} {\it n/eqcm^2}$



Irradiation trap model: cceptor: E= E, + 0.46 eV; n=0.9; σ, = 5

acceptor,	L= L, + 0.40 CV, I]=0.5,	0, - 3 × 10 ,	0h = 3 x 10
Acceptor;	E= E _c + 0.42 eV; η=1.613;	$\sigma_e = 2 \times 10^{-15};$	$\sigma_{\rm h} = 2 \times 10^{-14}$
Acceptor;	$E = E_c + 0.10 eV;$	η=100;	$\sigma_{e} = 2 \times 10^{-15};$
σ _h = 2.5 x	10-15		
Donor;	E= E _v - 0.36 eV; η=0.9;	σ _e = 2.5 x 10 ⁻¹⁴	; $\sigma_{\rm h}$ = 2.5 x 10 ⁻¹⁵

 Impact Ionization Model: Universty of Bolonia

¹P. Fernandez et al, "Simulation of new p-type strip detectors with trench to enhance the charge multiplication effect in the n-type electrodes"

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Pads detectors with multiplication



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Mask layout: Strip detectors with multiplication





Round diode do not have p+ implant

Ongoing measurements of the detectors in Liverpool and Freiburg

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NEW PROJECT

Mask set Technological simulation Electrical simulation for FZ Conclusions Motivatio

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1. Thin p-type epitaxial substrates

Detector proposed by Hartmut Sadrozinski and Abe Seiden (UCSC), **Ultra-Fast Silicon Detectors (UFSD)**.

Provide in the same detector and readout chain:

- Ultra-fast timing resolution [10's of ps]
- Precision location information [10's of μ m]

We propose to achieve high electric field using thin p-type epitaxyal substrates^a grown on thick support wafers, p+ type doped, that acts as the backside ohmic contact. Different thicknesses will be used to study the multiplication effect induced by the high electric field at the collecting electrodes, depending on availability we propose to use: 10, 50, 75 μ m. Need very fast pixel readout.

^aH. Sadrozinski, "*Exploring charge multiplication for fast timing with silicon sensors*" 20th RD50 Workshop, Bari 2012

Motivation

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2. Low gain avalanche detectors (LGAD)

Creating a n++/p+/p- junction along the centre of the electrodes. Under reverse bias conditions, a high electric field region is created at this localised region, which can lead to a multiplication mechanism².



²P. Fernandez et al, "Simulation of new p-type strip detectors with trench to enhance the charge multiplication effect in the n-type electrodes", Nuclear Instruments and Methods in Physics Research A658 (2011) 98–102.

Wafers Substrates Strip detectors Mask

Mask set





Wafers Substrates Strip detectors Mask

Wafers



Total of 24 wafers with three different annealings (shallow, standard and deep)

	Epitaxial $9.8 \mu m$	Epitaxial 50.4 μm	FZ
With	2 Shallow	2 Shallow	2 Shallow
p-implant	1 Standard	1 Standard	1 Standard
	1 Deep	1 Deep	1 Deep
Without	2 Shallow	2 Shallow	2 Shallow
p-implant	1 Standard	1 Standard	1 Standard
	1 Deep	1 Deep	1 Deep
Total:	8	8	8

Wafers **Substrates** Strip detectors Mask

Substrates



Epitaxial

Substrate: 100mm, 525 μm Boron type with resistivity 0.006 $\Omega\cdot cm$ < 100 > Epilayer:

Thick	Resistivity
9.8µ <i>m</i>	$110.5\Omega \cdot cm$
50.4 μ m	96.7Ω · <i>cm</i>

FΖ

p-type 285 $\mu m < 100 >$ resistivity $(12 \pm 7) k\Omega \cdot cm$

Wafers Substrates Strip detectors Mask

Strip detectors



Pitch $p = 80 \mu m$

	Strip	Metal	P-implant	w/p				
	$[\mu m]$	$[\mu m]$	$[\mu m]$					
AC1	24	20	6	0.3				
AC2	24	24	6	0.3				
AC3	24	28	6	0.3				
AC4	48	44	30	0.6				
AC5	48	48	30	0.6				
AC6	48	52	30	0.6				
AC7	62	58	44	0.775				
AC8	62	62	44	0.775				
AC9	62	66	44	0.775				
AC and DC	32	40	14	0.4				

Wafers Substrates Strip detectors Mask

Strips AC





Wafers Substrates Strip detectors Mask

Strips DC





Wafers Substrates Strip detectors Mask



FE-I4

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Wafers Substrates Strip detectors Mask

FE-I4 with one guard ring





Wafers Substrates Strip detectors Mask



FE-I3



Wafers Substrates Strip detectors Mask

FE-I3 with one guard ring





Wafers Substrates Strip detectors Mask





Pixels with polysilicon bias resistor



Wafers Substrates Strip detectors Mask

Diodes



Diodes without and with p-implant $1000 \mu m$ diameter



2D simulations Doping profiles



Technological simulation for epitaxial wafers



2D simulations Doping profiles

Centre Nacional de Microelectrònica

Technological simulation for the FZ wafer





2D simulations Doping profiles

Doping profiles for epitaxial wafers





2D simulations Doping profiles

Doping profiles for FZ wafer







AC1

Electric field for FZ wafers for AC1 detector at 200V

With multiplication Without multiplication









Electric field for FZ wafers for AC2 detector at 200V

With multiplication Without multiplication







AC3

Electric field for FZ wafers for AC3 detector at 200V

With multiplication Without multiplication







- We have measured pads with multiplication from the previous fabrication
- Measurements of strip detectors are ongoing
- More electrical simulations need to be performed
- The fabrication of the new devices will begin soon in the clean room facility at CNM Barcelona (end of February)
- More information in Hartmut Sadrozinki's talk "Ultra Fast Silicon Detectors"



Thanks for your attention