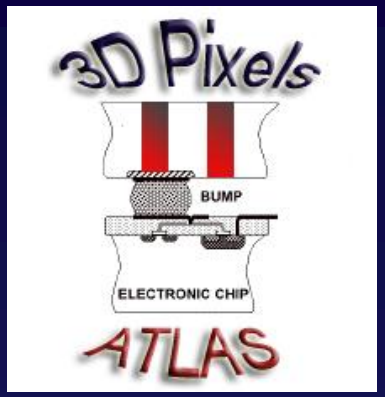
# 3D-S: A fast, high resolution, low-mass, detector with embedded cooling and internal charge multiplication capability



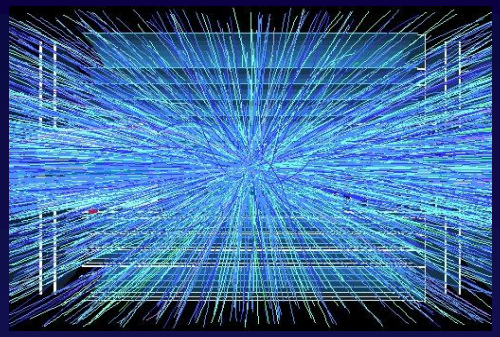

Cinzia Da Via, The University of Manchester, UK

GianFranco Dalla Betta, Marco Povoli, Ian Houghton, Maurizio Boscardin, Jasmine Hasi, Angela Kok, Giulio Pellegrini, Chris Kenney, Sherwood Parker, Giovanni Darbo, Sebastian Grinstein, Philippe Grenier, Steve Watts, Vladislav Tyzhnevy, Giulia Romagnoli, Jerome Noel, Paolo Petagna, Alessandro Mapelli

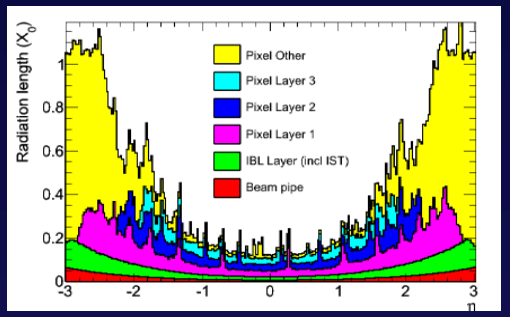
- Introduction
- 3D-S the low mass modular system:
  - The sensor
  - The interconnection
  - The micro-channel cooling
- Summary and plans

# 3D-S

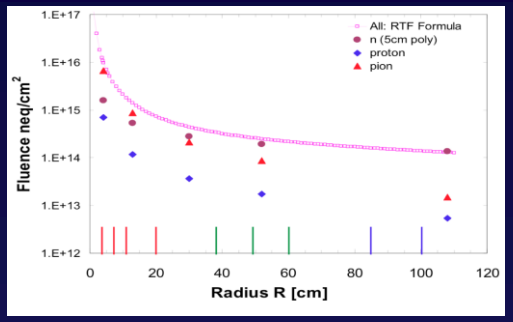
We are exploring ways to build a low mass modular system exploiting "micro-fabrication". The ATLAS Vertex detectors at the HL-LHC is our primary goal.



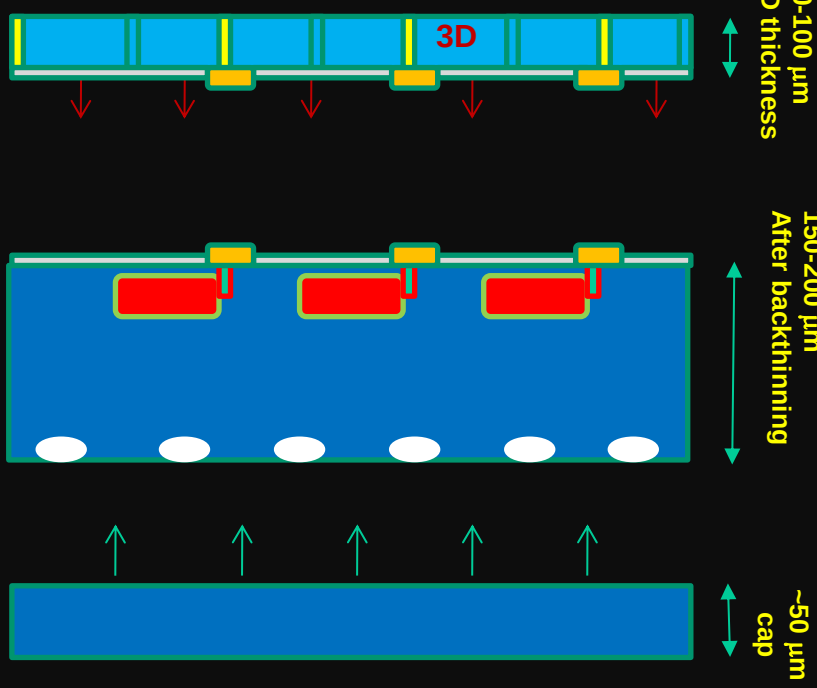
Precision reconstruction




Material budget

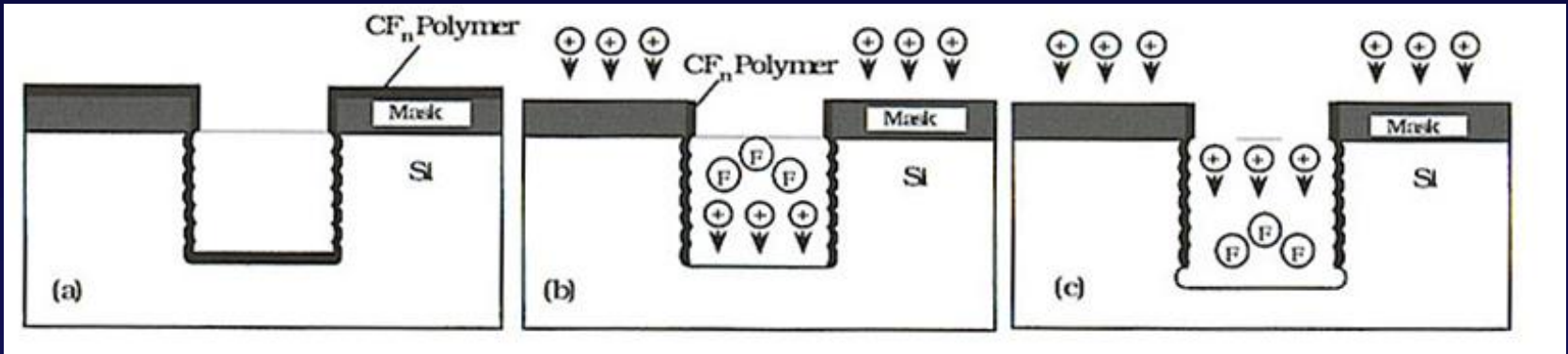


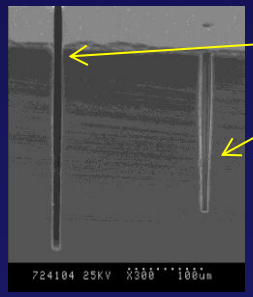

Radiation tolerance




- Thin 3D silicon sensor modules with active edges
  - Charge multiplication by design
- Interconnected with micro-bump bonds and through chip bias supply
- Embedded micro-cooling
- Support

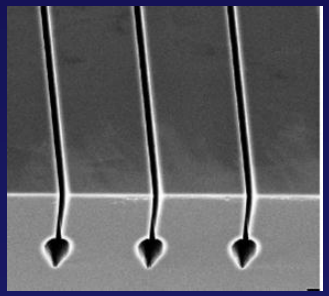
# Microfabrication



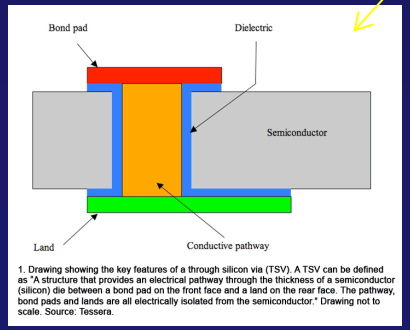



For 3D sensors electrode definition and active edges

For cooling micro-channels



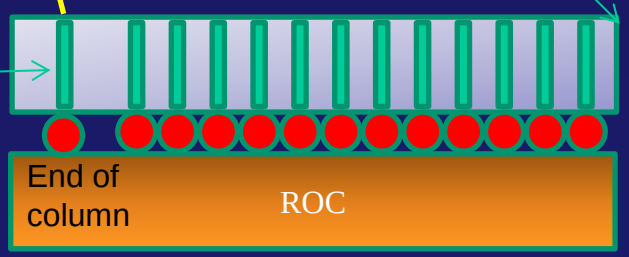
Interconnectivity Using TsV



1. Drawing showing the key features of a through silicon via (TSV). A TSV can be defined as "A structure that provides an electrical pathway through the thickness of a semiconductor (silicon) die between a bond pad on the front face and a land on the rear face. The pathway, bond pads and lands are all electrically isolated from the semiconductor." Drawing not to scale. Source: Tessera.

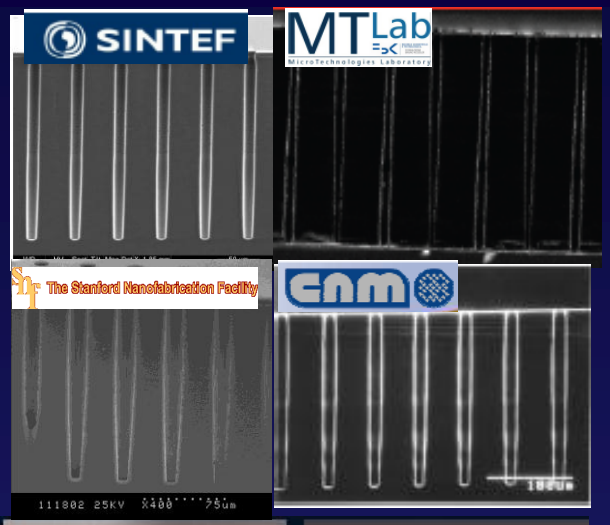
Extra holes
On 3D sensor side
To carry signal out

1- conformal metal
2-doped poly (tests encouraging



# Aspect ratio

M. Puech. ALCATEL



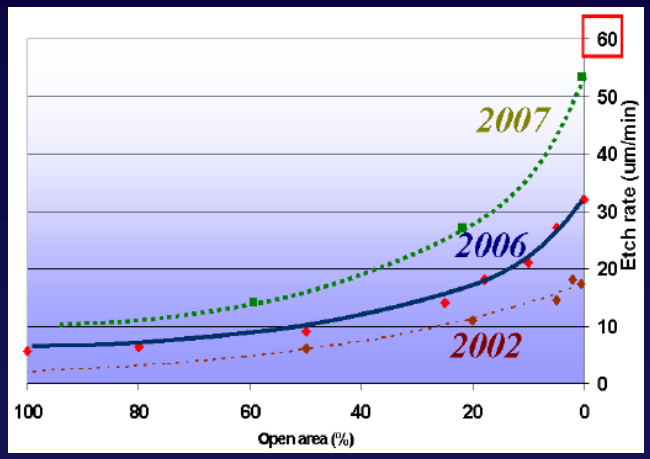

11:1 1997

24:1 2009

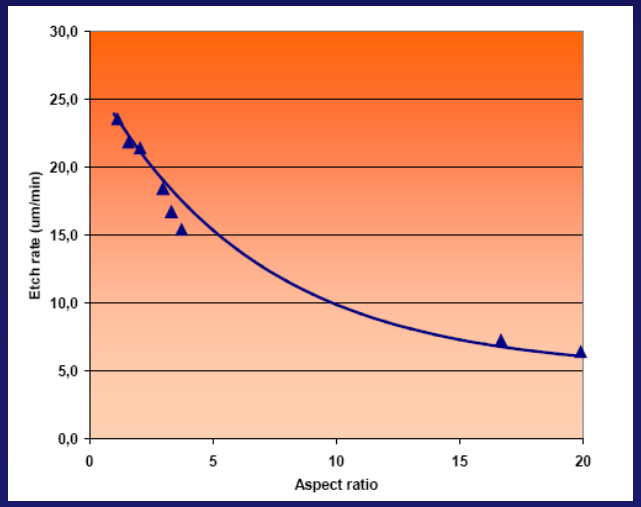
Today

40-60:1

110:1!!!

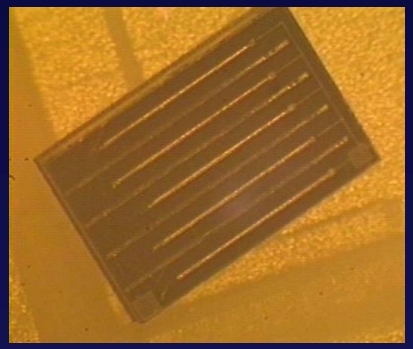



Etching rate depends on exposed area

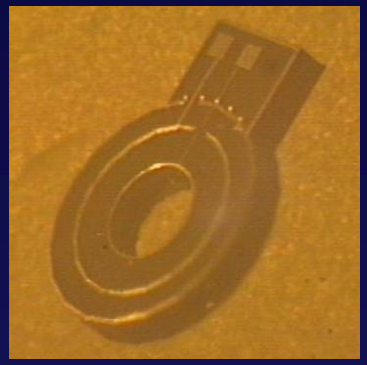



etching rate depends on aspect ratio

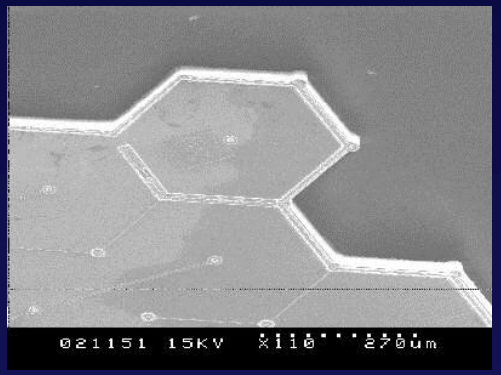
# Other structures already fabricated at STANFORD (C. Kenney, J. Hasi) to improve speed, detection properties



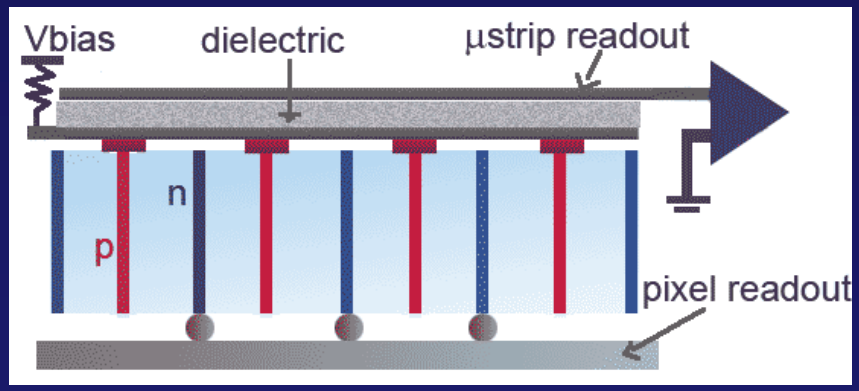
3D Parallel trenches



3D coaxial layout




3D hexagonal

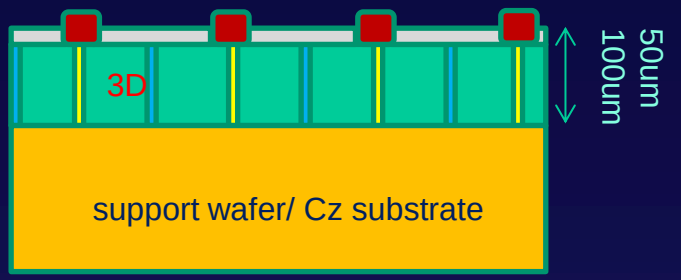


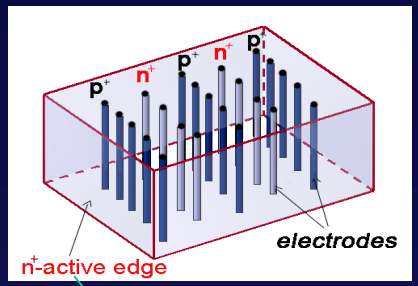

Dual readout:

Improved spatial resolution
With the same material budget

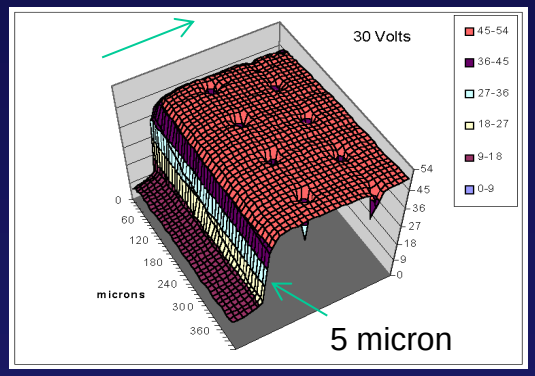
*C. Da Via et al., "Dual readout – strip/pixel systems", NIM A594, pp. 7-12 (2008).*

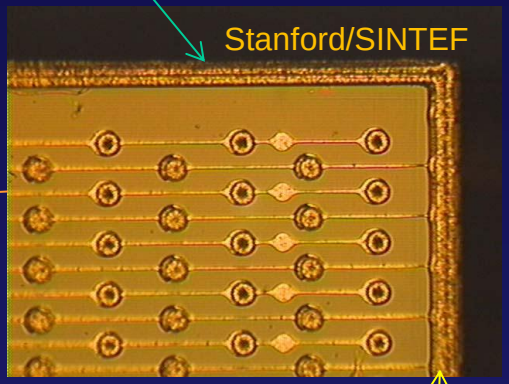
# A thin 3D sensor with active edges

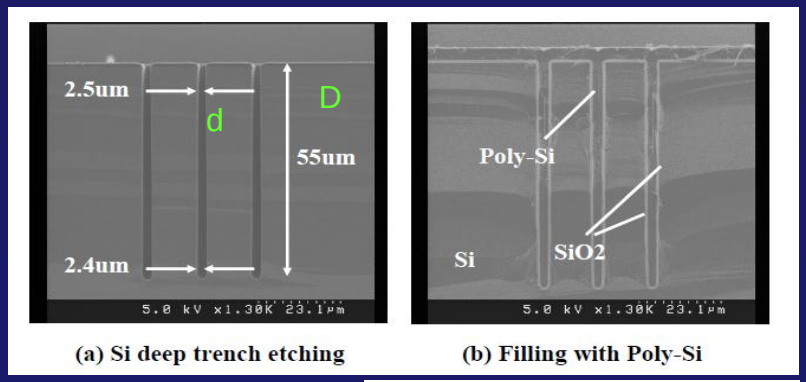



X-ray micro beam scan J. Hasi




Aspect ratio

D/d =24
55/24=2.3

- 3D silicon with active edges
- Processing vias on thin silicon requires a support wafer
- In 3D Capacitance decrease with thickness
- Epitaxial silicon can be used in case of very thin substrates
- The support wafer can be removed after bump bonding (or after UBM using reversible wafer bonding)

# Activity at CNM , D. Quirion

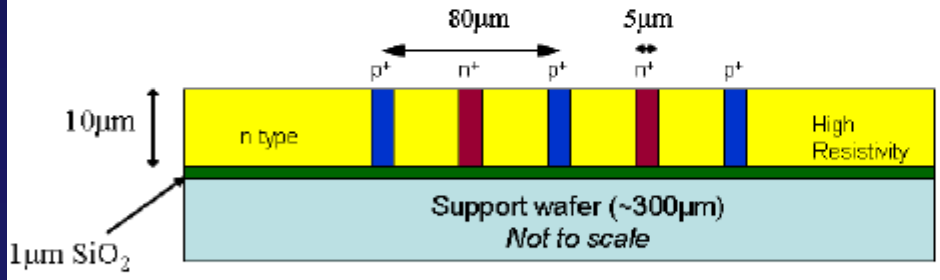
Similar work at FBK and SINTEF

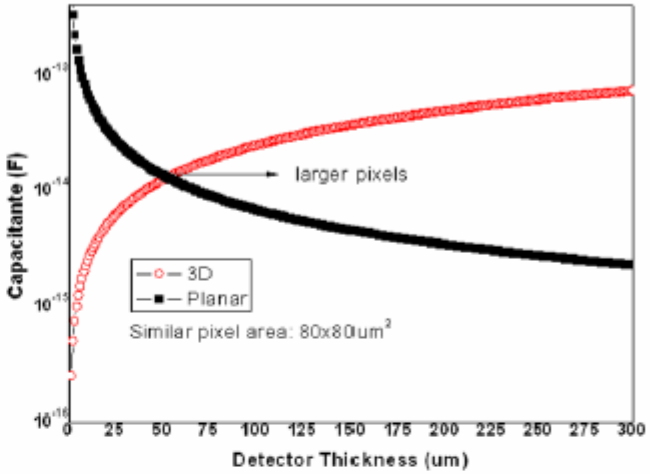


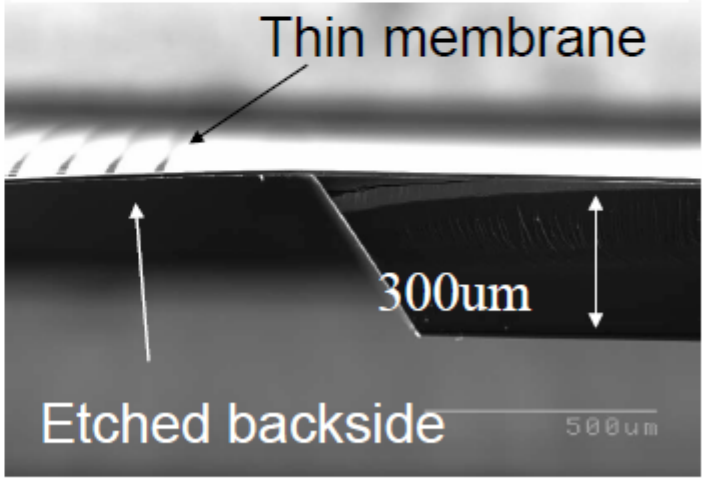
## U3DTHIN sensors

When sensor thickness is reduced below 50um, capacitance is high and electronic noise is large

Idea: combine very thin sensors with 3D geometry



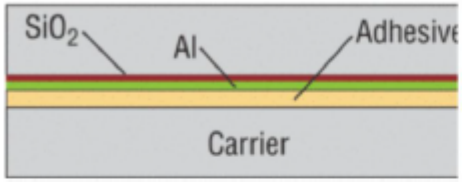

*F. García et al., Nucl. Instrum. Meth. Phys. Res. A 607 (2009) 57*

# Activity at SINTEF

A. Kok, Workshop on 3D sensors and Microfabrication Systems



## Temporary bonding - brewer science® waferbond®



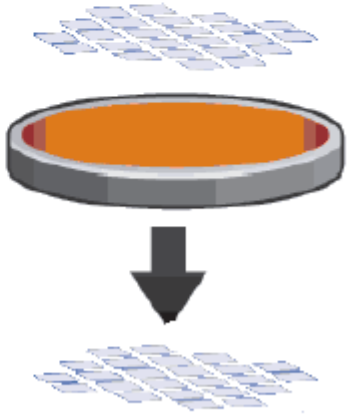

Bonding device wafer to a carrier to allow processing

Through substrate patterning (eg. VIA)

Patterning of through substrate structure

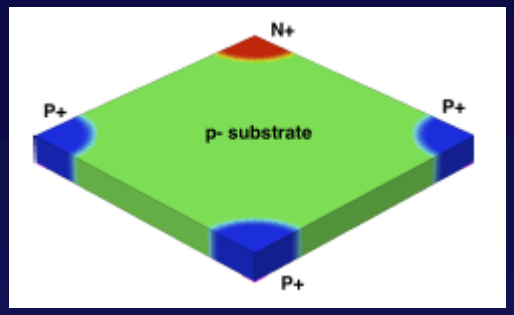
Release of carrier wafer

Similarly, sensors with active edges can have the support wafer removed when bonded to a carrier wafer, while sensors are release once the waferbond® is removed

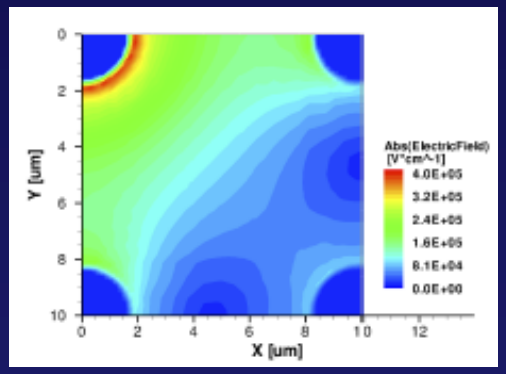


# 3D Fast + Charge multiplication by design simulation results

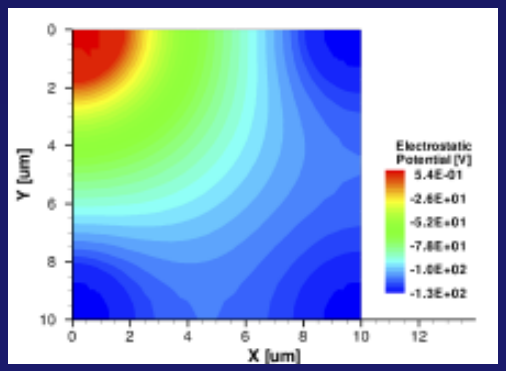
Sentaurus simulation package
M. Povoli and G-F Dalla Betta (University of Trento, Italy)



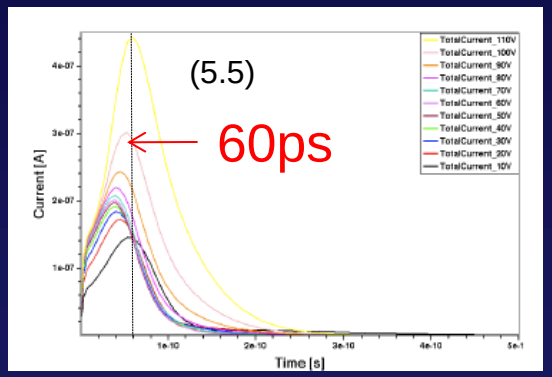

Size = 10 x 10 x 1μm$^3$
Column radius = 2μm
Electrode doping = 5x10$^{19}$cm$^{-3}$
Bulk doping = 1x10$^{13}$cm$^{-3}$

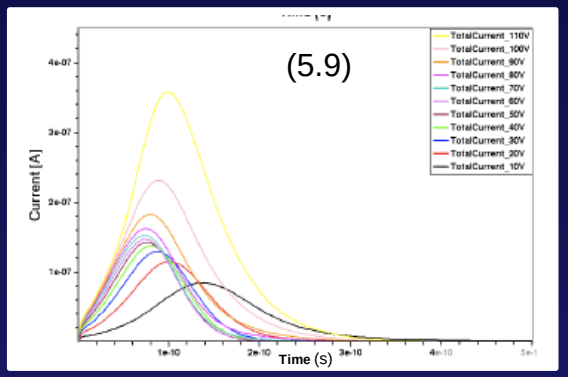


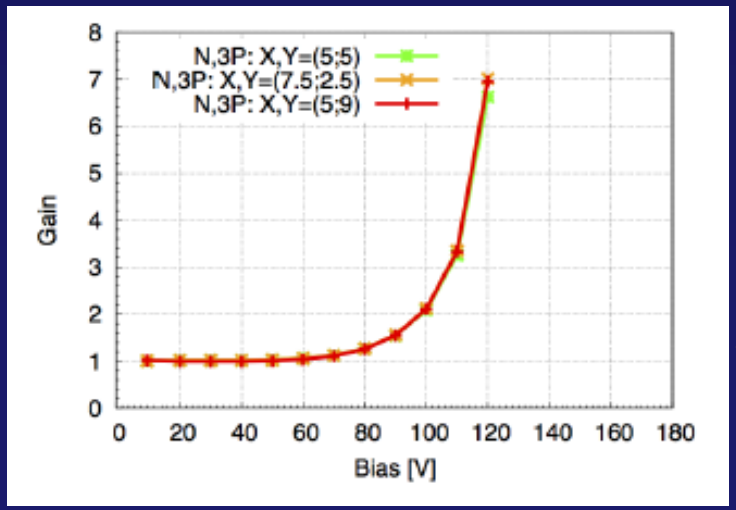

V=130V

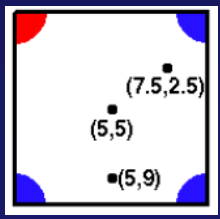



Transients with minimum-ionizing particles




GAIN does Not depend on position

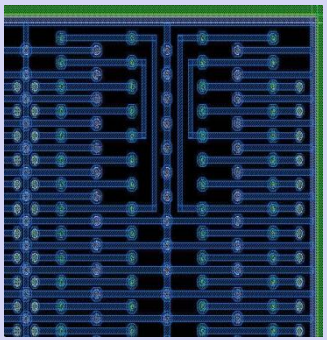
# Radiation Tolerance of 3D sensors

$\lambda = \tau \times v$

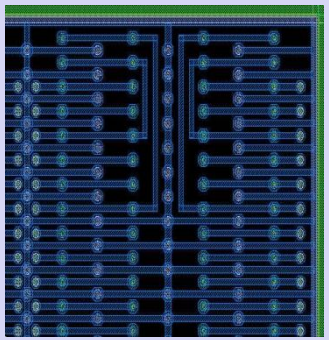
Drift length — Trapping time — Drift Velocity (saturated)

$$S = \frac{\lambda}{L}\left[1 - \exp\left(-\frac{L}{\lambda}\right)\right]$$

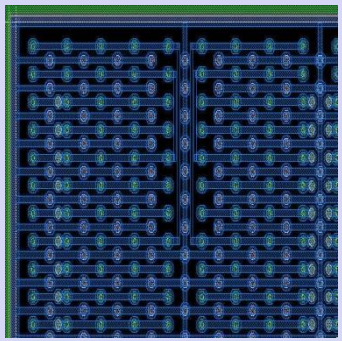
L= Inter-Electrode Spacing



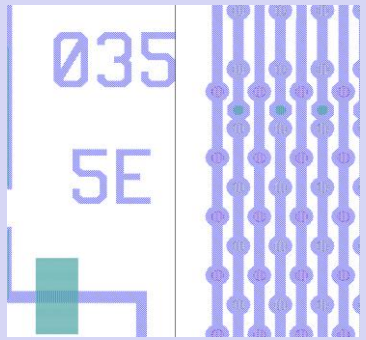
2E = 103um



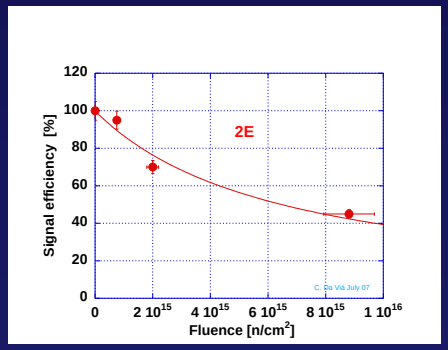
3E= 71um (IBL DESIGN)

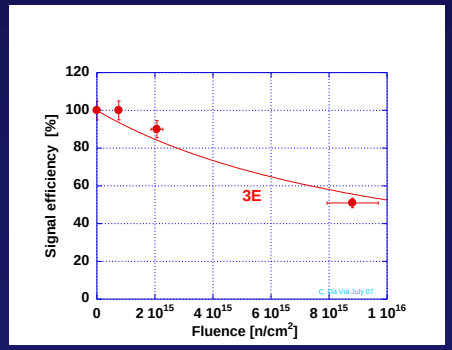


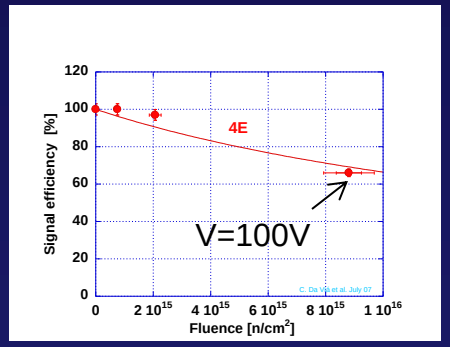
4E= 56um

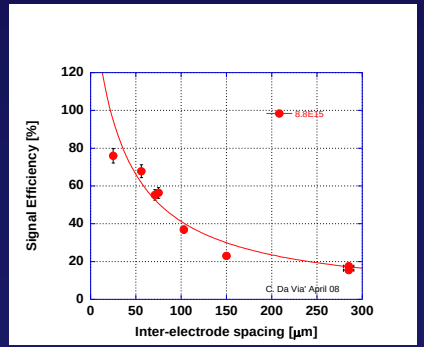



5E= 47um




**At 9x10$^{15}$ ncm $^{-2}$ And biases below 200V**

| L=IES [um] | 105 | 71 | 56 | 47 |
|---|---|---|---|---|
| Signal Efficiency [%] | 45 | 51 | 66 | 68 |
| Charge 50um [e−] | 1800 | 2040 | 2640 | 2720 |
| Charge 100um [e−] | 3200 | 4080 | 5280 | 5440 |

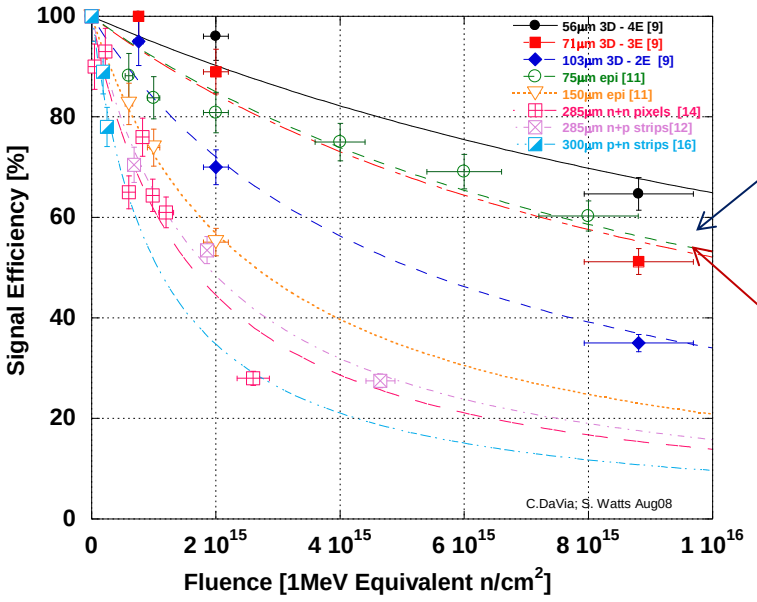
Nucl. Instrum. Meth. A 603 (2009) 319-324

# Signal efficiency and signal charge in Si Sensors


[9] C. Da Via et al.", (NIMA-D-08-00587)
[10] G. Kramberger at al., Nucl. Instr. Meths. A 554 (2005) 212-219
[11] G. Kramberger, Workshop on Defect Analysis in Silicon Det, Hamburg, August 2006. http://wwwiexp.desy.de/seminare/defect.analysis.workshop.august.2006.html
[12] G. Casse et al., Nucl. Instr. Meths. A (2004) 362-365
[14] T. Rohe et al. Nucl. Instr. Meths. A 552 (2005) 232-238
[16] F. Lemeilleur et al., Nucl. Instr. Meths. A 360 (1995) 438-444



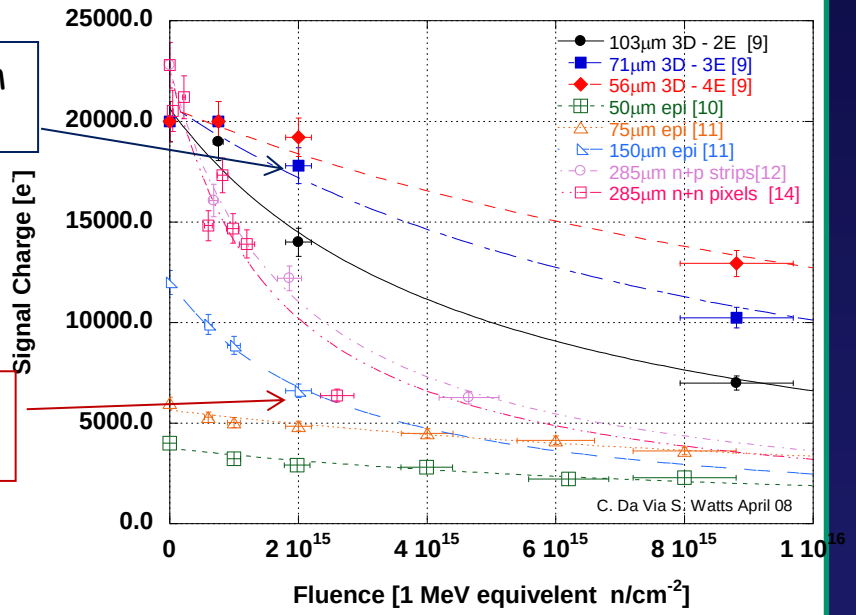

## Signal Efficiency (prop 1/IES)




71μm 3D

75μm epi

## Signal charge (depends on Δ)




## Simple example at $10^{16}$ ncm$^2$

Δ=substrate thickness
λ= <trapping distance>~30um

$S_{MIP}$ planar ~ 80 (λ/IES) x Δ ~ 80λ ~ 80x30 ~ 2400e$^-$

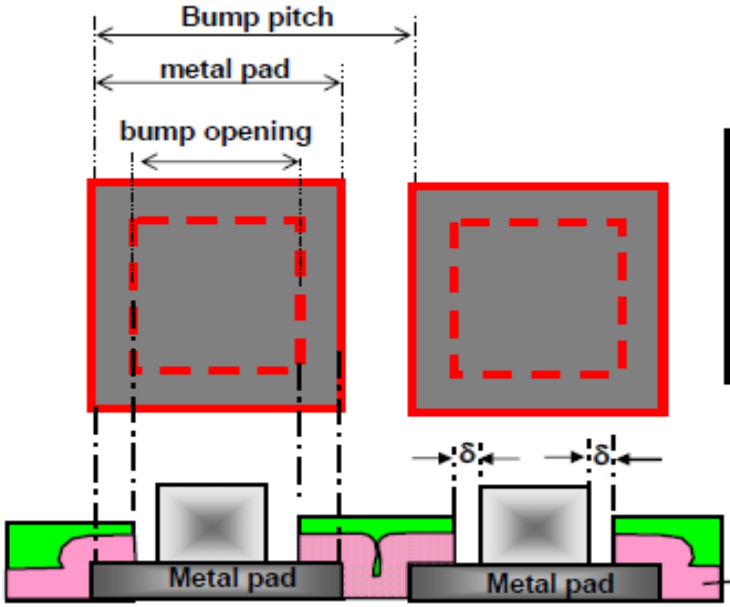
$S_{MIP}$ 3D ~ 80λ x (Δ/IES) ~ 2400 x 210/(71-22$_{electrode\ implant}$) ~ 10290e$^-$

3D has more signal charge because collection distance and substrate thickness are Decoupled

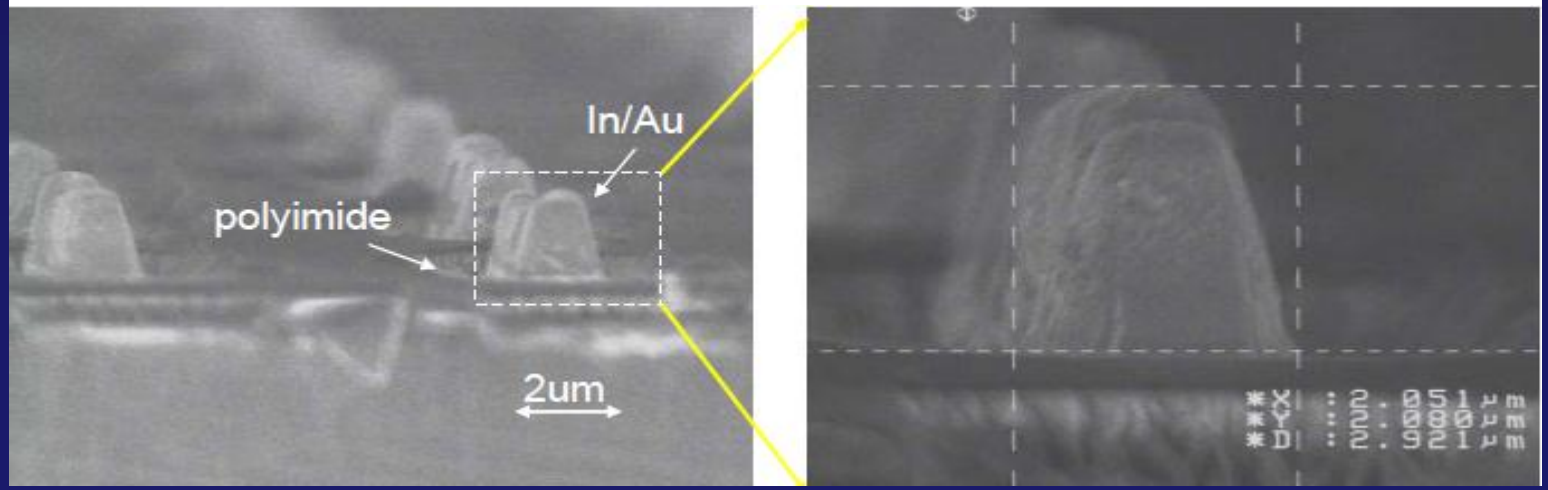
# Interconnectivity: New developments in small pitch bump-bonding



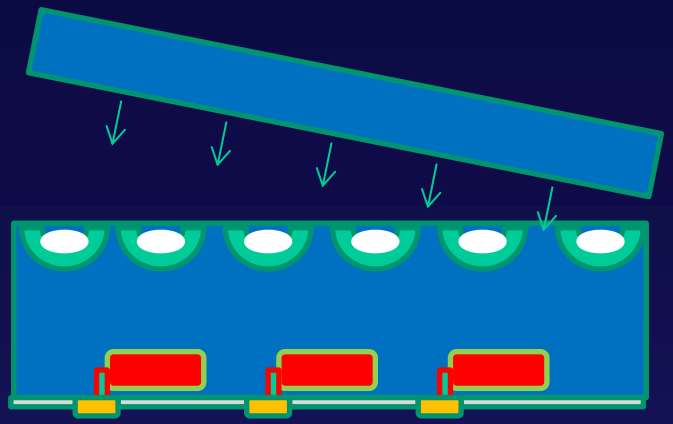





| | |
|---|---|
| bump pitch | 5.0 μm |
| Metal pad | 4.0 x 4.0 μm |
| Bump opening | 3.0 x 3.0 μm |
| Bump size | 2x2 μm (bottom) |



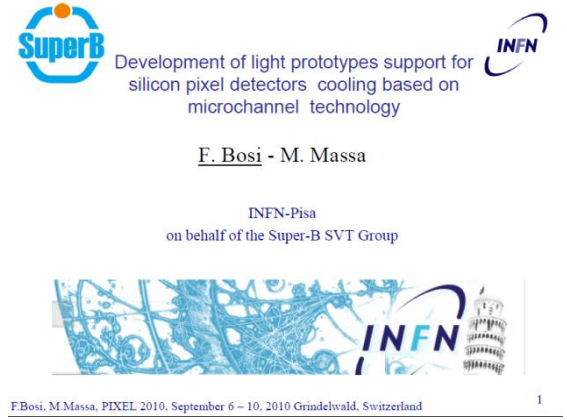
# Embedded Micro-cooling

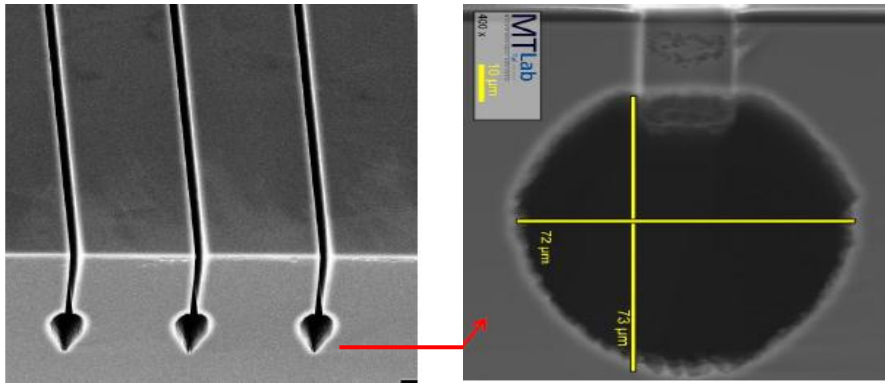



Two methods presently explored:

1- surface micro-groves

2- over-etched channels in trenches




Micro-channels fabricated at FBK in collaboration with the Pisa group

# Prototype using Method 1

Driving CERN +EPFL group

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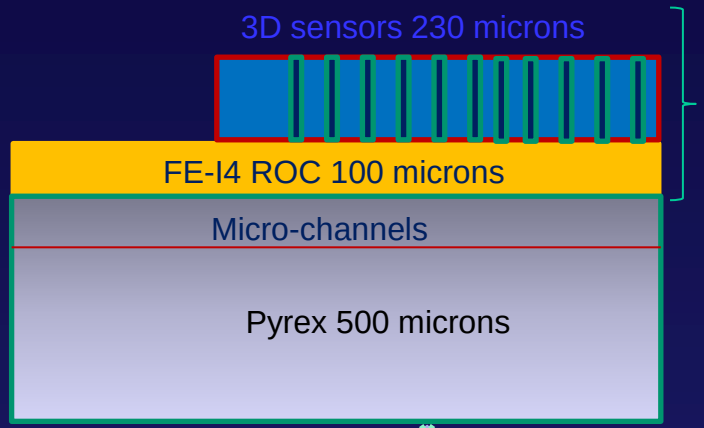
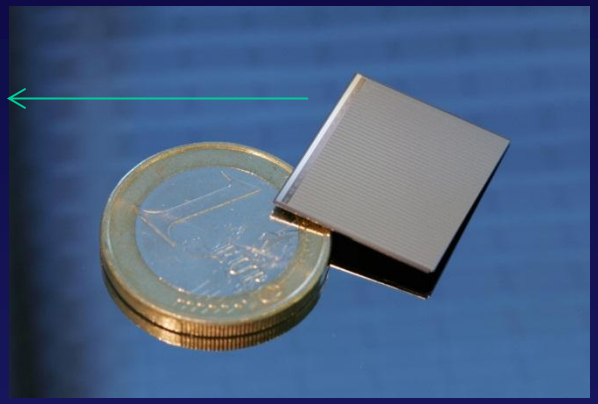
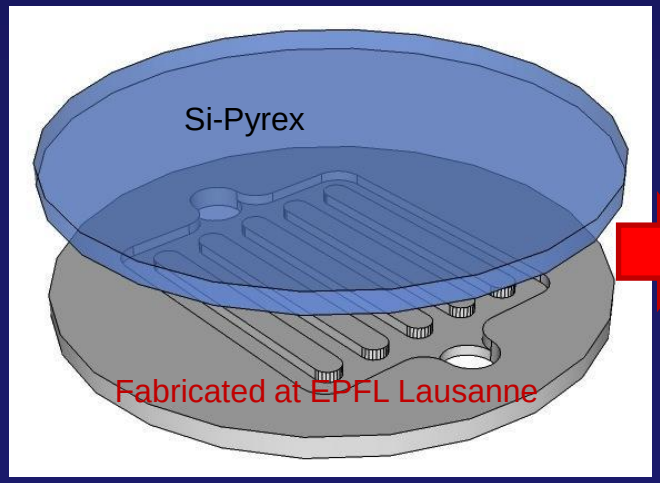
Paolo Petagna
Alessandro Mapelli
(Jan McGill)
(Alan Honma)

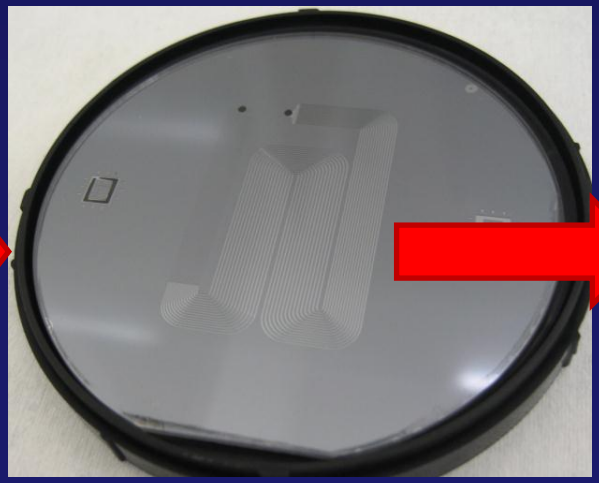


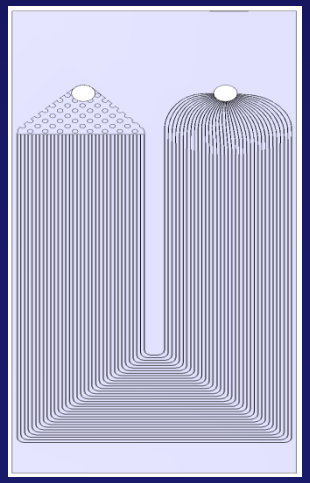



Bump-bonding and Thinning IZM Berlin

LHCb design





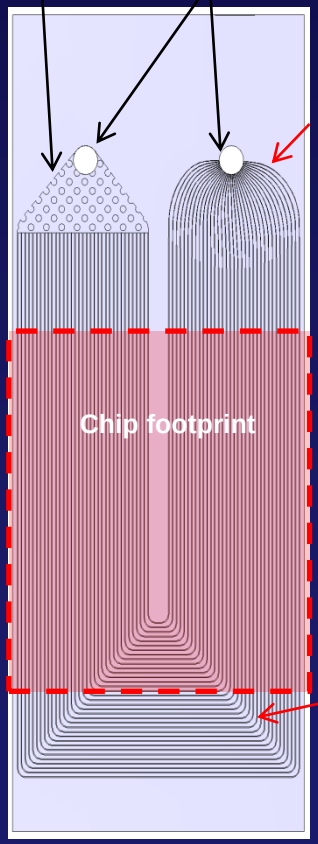
# ATLAS Micro-channel Cooling – First Prototype

- 35 Channels 50 x 50 μm + 200 μm walls
- Channels with restrictions (10 μm wide x 50 μm deep, 7 mm long )
- Two holes for inlet and for outlet (1.6 mm diameter)
- Pillars in the outlet to maximize the bonded surface

Silicon device 380 μm thick, with etched micro-channels
Bonding with 2mm pyrex to close the channels

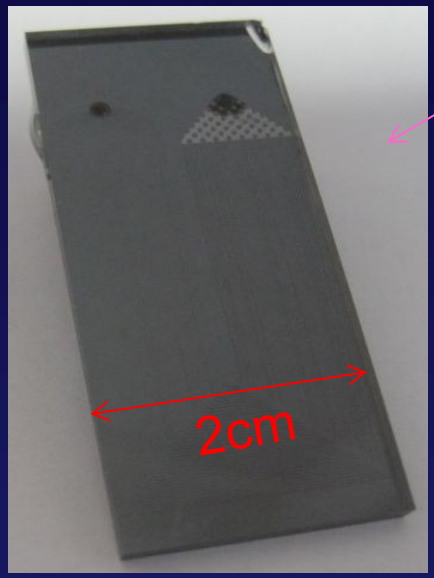
**Pillars in the outlet** to maximize the bonded surface

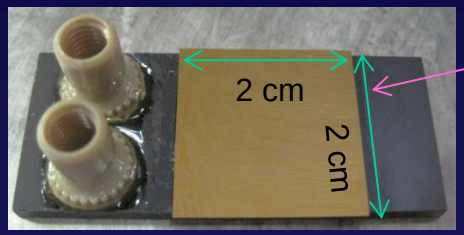
**2 holes for fluidic inlet and outlet** (1.6 mm diameter)




**Restrictions** (10 μm wide x 50 μm deep, 7 mm long) to bring $CO_2$ in critical conditions at the channels entrance

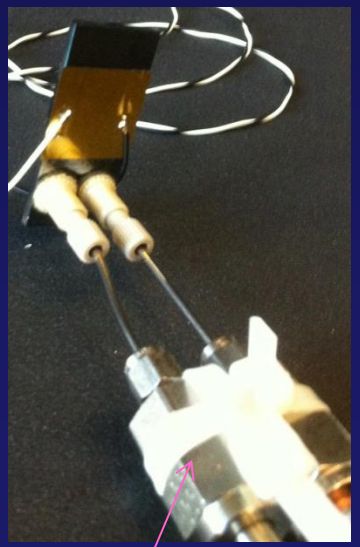
**35 micro-channels** 50 x 50 μm separated by 200 μm wide walls



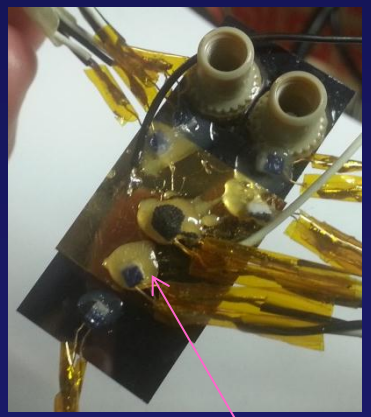




silicon heater with (20 nm Ti + 200 nm Au) metal layer

With glued nano-port connectors



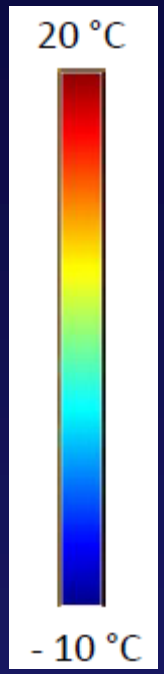
Connect the device to a $CO_2$ plant

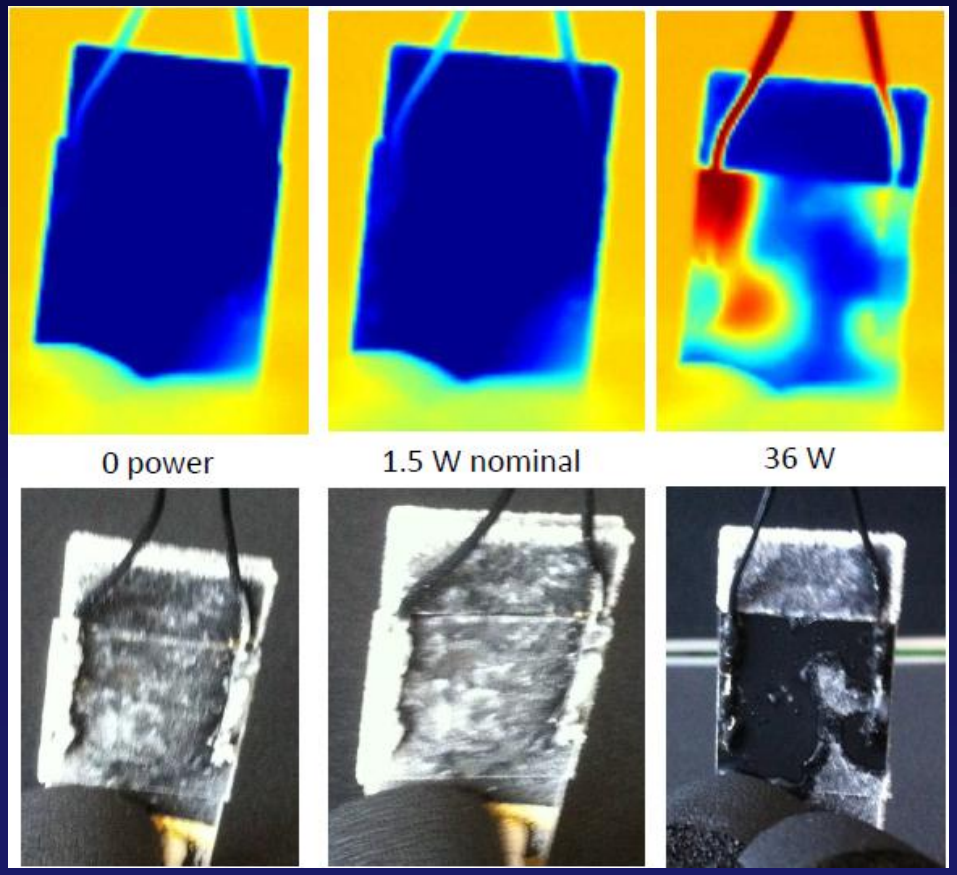


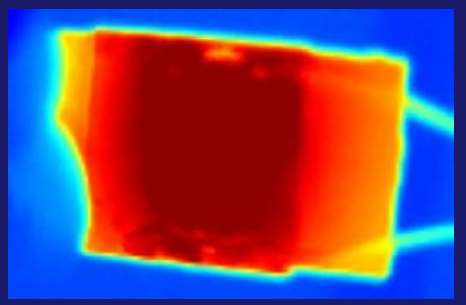
Pt100 on the surface

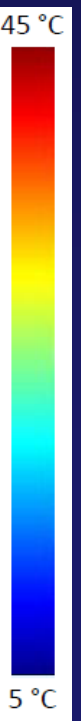
# Second prototype cooling tests with CO2








Manufactured at EPFL
Measurements Giulia Romagnoli

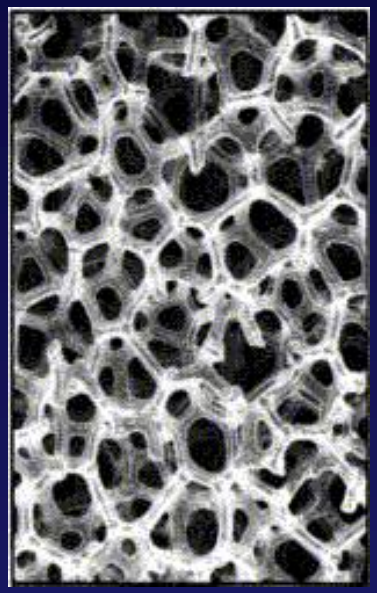
No cooling!!! →

# Supports

Plume Collaboration
For the ILC



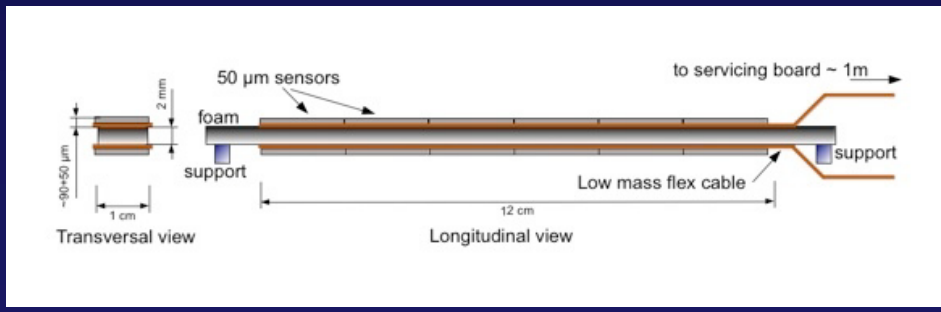


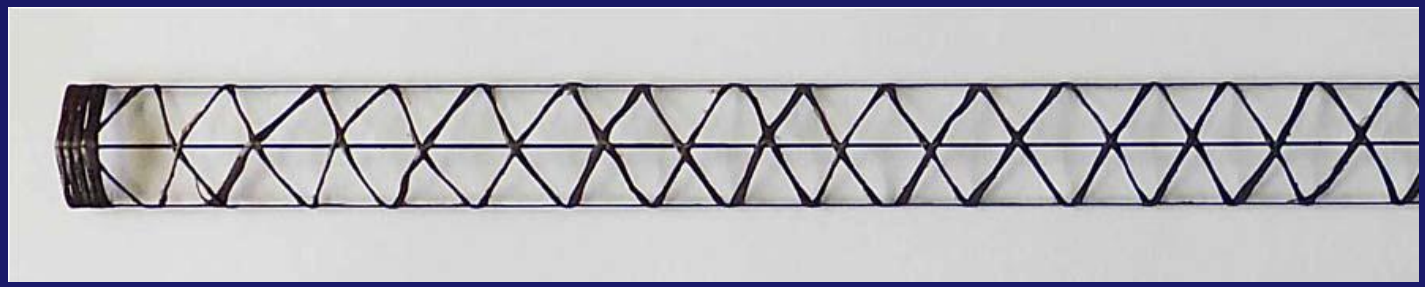


- Open-cell foam
- Macroscopically uniform
- No tensioning needed

- Lightweight elements in silicon carbide (SiC) foam
  - 4 to 8 % fill factor
  - Can be machined

Ultra-thin ladders



ALICE

# Summary and plans



## 3D-S :

a compact detector module with:

- Active edges
- Fast
- Charge multiplication by design
- Embedded cooling

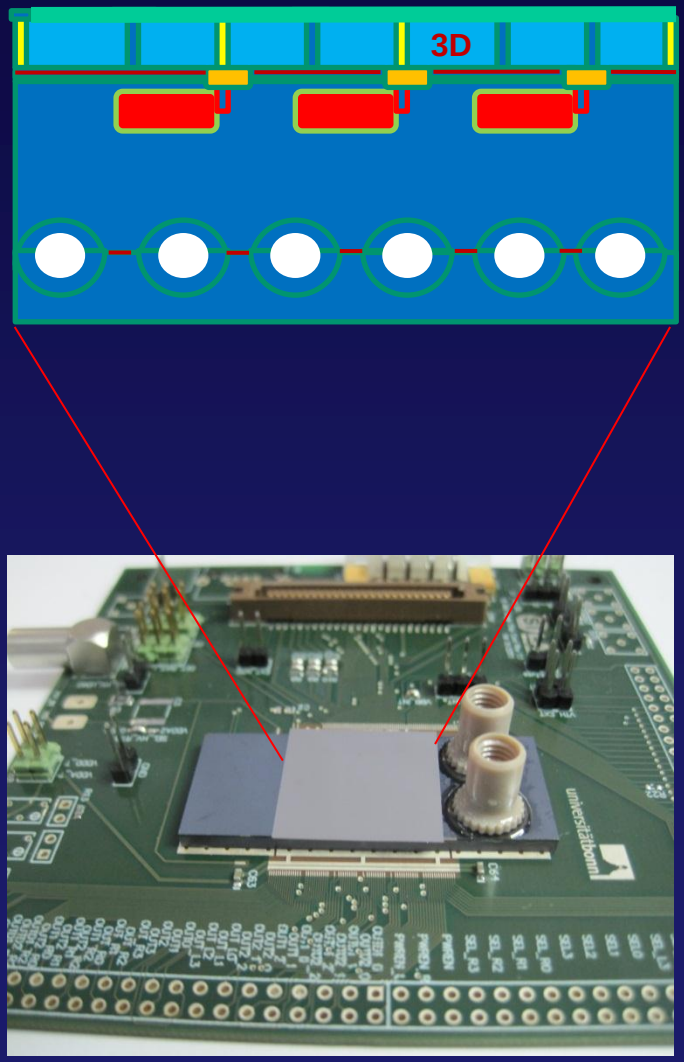
should address some of the future vertex detector challenges:

- Granularity (this will be electronics dependent)
- Low mass
- Radiation tolerance

prototypes of sensors (FBK, CNM, SINTEF, SLAC) and micro-cooling channels (see talk of Giulia Romagnoli) are being designed and fabricated

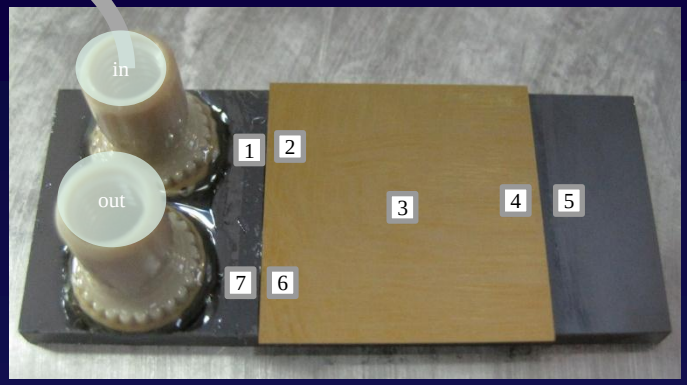
Simulated structures show that charge multiplication by design can have gain as good as 7 before and after irradiation

A test module based on a 230 microns 3D sensor from the IBL-pre-production (with slim edges) bump-bonded to a 100 micron thin front-end electronics FE-I4 A chip (IZM Berlin) is being equipped with micro-channels and will be tested in beams before and after irradiation



# SPARES

# Preliminary Tests

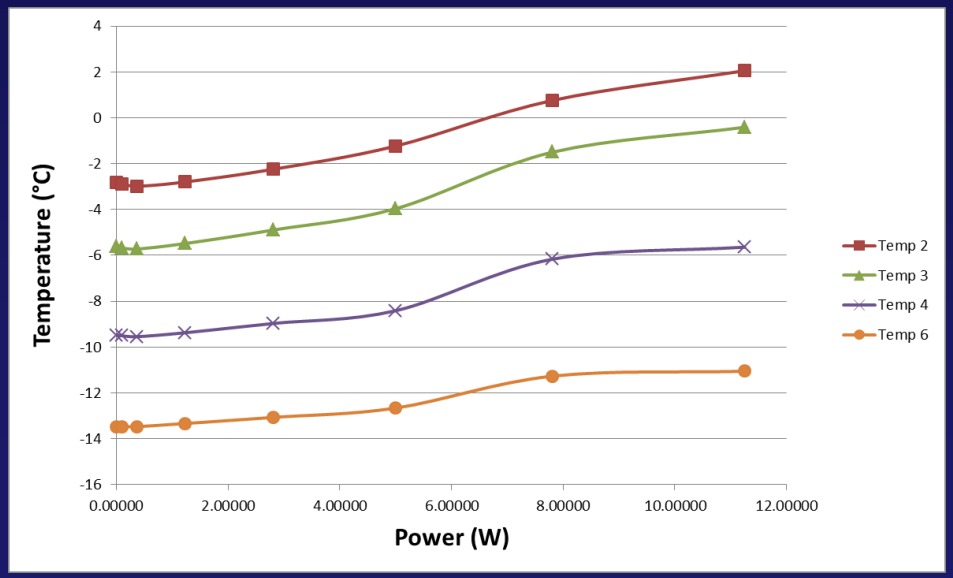



Pressure test good up to 65 bars

Mass flow rate: **0.25 g/s** (**1000 * nominal**)

Temperature measurement accuracy ± 0.5 °C

Numerical simulations of $CO_2$ flow courtesy of João Noite




Design optimized for ideal flow conditions:

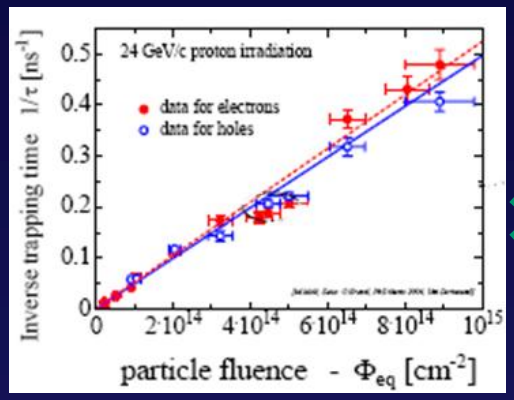
- Flow rate = **0.2 mg/s**
- $T_{inlet}$ = - 18 °C
- $T_{after\ restrictions}$ = - 20°C
- $\Delta T_{under\ chip\ area}$ < 1 °C
- $P_{inlet}$ = ~ 20 bar
- ΔP = ~ 0 bar

Test conditions (limited by setup):

- Flow rate = **0.2 g/s**
- $T_{inlet}$ = - 2 °C
- $T_{after\ restrictions}$ = - 4 °C
- $\Delta T_{under\ chip\ area}$ ~ 10 °C extimated
- $P_{inlet}$ = ~35 bar
- ΔP = ~10 bar

# TRAPPING in Si → COLLECT ELECTRONS, INCREASE E-field and USE SHORT 'IES' (THIN SUBSTRATES FOR PLANAR) NIMA 603 (2009) 319–324



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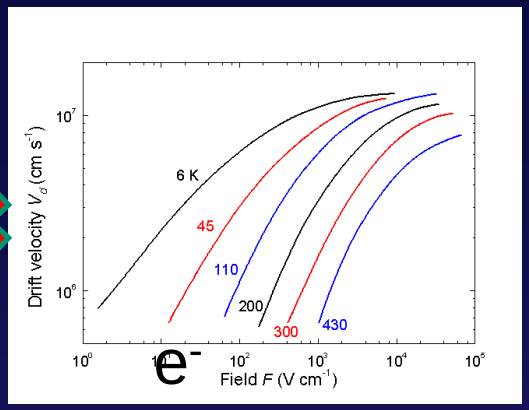


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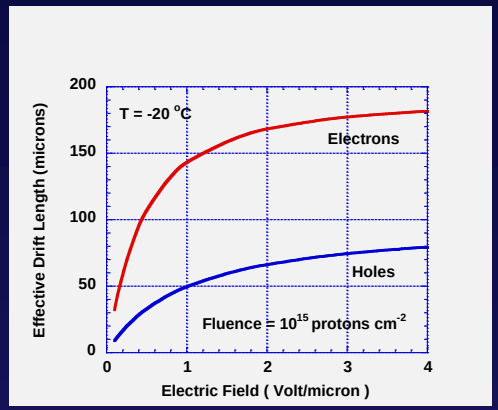


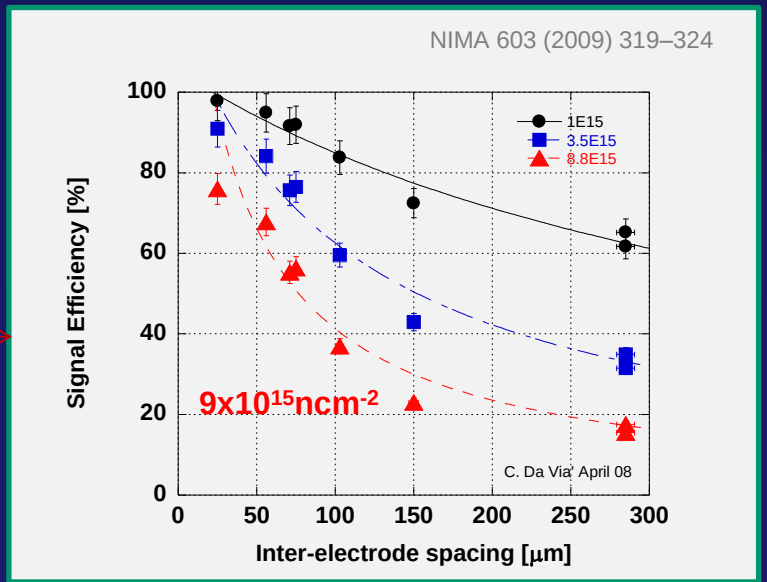

$\tau_{tr}$ $V_{drift}$ $\lambda$ (trapping distance)

$$\frac{dS}{dt} = q\frac{dV_W}{dx}\frac{dx}{dt}\exp(-\frac{x}{\lambda})$$

$$S = \frac{\lambda}{L}\left[1-\exp(-\frac{x}{\lambda})\right]$$

Trapping times from Kramberger et al. NIMA 481 (2002) 100

Expected signal
After irradiation
Without multiplication
Depends on λ/L
This is also true for diamond



# 3D for the ATLAS IBL
# by the 3DATLAS R&D Collaboration
# 25% of the total IBL modules

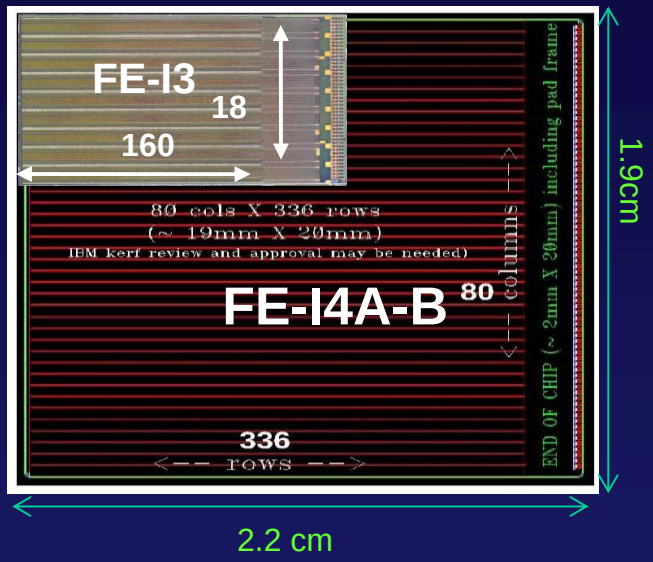
NIMA 694 (2012) 321–330

See N14-154 poster

Cinzia Da Viá , Uni. Manchester, Trento Workshop 20th February 2013

total pixel number: 26880

Total number of columns per chip : >100.000




4+1 runs were completed in February and October 2012 by CNM (Barcelona, Spain) and FBK (Trento, Italy) with double side process with >350 good chips, more than 100 wafers and an yield exceeding 60% fulfilling the following:

**Sensor specifications for IBL:**

- Qualify to $5 \times 10^{15}$ $n_{eq}$
- max. power dissipation: 200 mW/cm$^2$ at -15 C
- tracking efficiency > 98%.

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| Item | Sensor Specification |
|---|---|
| Tile type | single |
| Number of $n^+$ columns per 250 $\mu$m pixel | 2 (so-called 2E layout) |
| Sensor thickness | 230 $\pm$ 20 $\mu$m |
| $n^+$-$p^+$ columns overlap | > 200 $\mu$m |
| Sensor active area | 18860 $\mu$m $\times$ 20560 $\mu$m (including scribe line) |
| Dead region in Z | < 200 $\mu$m guard fence $\pm$ 25 $\mu$m cut residual |
| Wafer bow after processing | < 60 $\mu$m |
| Front-back alignment | < 5 $\mu$m |