# HARDWARE CHANGES IN THE LHC BLM SYSTEM DURING LS1

C. Zamantzas*, B. Dehning, E. Effinger, V. Grishin, S. Jackson,
CERN, Geneva, Switzerland

*Abstract*

The strategy for machine protection and quench prevention of the LHC is heavily relying on the Beam Loss Monitoring (BLM) system. In this paper, a review of the operational experience with the system of the last running period, i.e. 2012, will be given together with the areas where required improvements were identified. Further, the foreseen changes during the first Long Shutdown (LS1) concerning the equipment, the code of the reprogrammable devices, the supporting applications, as well as the commissioning steps, will also be summarised.

## INTRODUCTION

The strategy for machine protection and quench prevention of the LHC is heavily relying on the Beam Loss Monitoring (BLM) system. Each turn, several thousands of data values are recorded and processed in order to decide if the particle beams are permitted to continue circulating or whether their safe extraction should to be triggered. The decision involves a proper analysis of the loss pattern in time and a comparison with predefined threshold levels that need to be chosen dynamically depending on the energy of the circulating beam. The processing of the acquired data has to be performed in real-time and thus requires dedicated hardware to meet the demanding time and processing capacity requirements.

The BLM system is sub-divided geographically into the tunnel and the surface building installations. The tunnel installation consists of close to 4000 detectors, placed at various locations around the ring, and radiation tolerant electronics for acquiring, digitising, and transmitting the data. The electronics installed in the surface buildings receive the data via 2 km long redundant optical data links. This system conditions, analyses and stores the data, and when needed issues warnings and abort triggers. For this purpose, the system has connections to the Beam Interlock, the Logging, the Beam Energy Tracking, the Collimation, the External Post-Operation Checks (XPOC), the Injection Quality Check (IQC) and the Post-Mortem systems.

## 2012 PERFORMANCE SUMMARY

From the initial deployment of the system onwards, continuous maintenance, either preventive or to repair failures, has been performed. In addition, new features have been introduced regularly to match new requests or in responds to new observations. An overview of the major performance improvements made during the 2012 operational period and a summary of the fault statistics is presented in the following chapters.

### *Automatic and Fast Collimator BBA*

Maximum beam cleaning efficiency and machine protection are provided when the collimator jaws are properly adjusted at well-defined distances from the circulating beams. Therefore, each of the LHC collimator needs to be verified and aligned regularly. A jaw is aligned with respect to a pilot beam when,while moving in steps towards the beam, a sharp increase followed by a slow exponential decrease appears in the signal read out from a BLM detector located downstream of the collimator.

As of January 2012, a new BLM data buffer was implemented for an automatic collimator Beam Based Alignment (BBA) system. Beam loss values, integrated over 82 ms, are transmitted in User Datagram Protocol (UDP) packets to a new collimation client at a rate of 12.5 Hz (was 1 Hz). Fig. 1 shows examples of the standard and the new dedicated data delivered to the Collimation system.

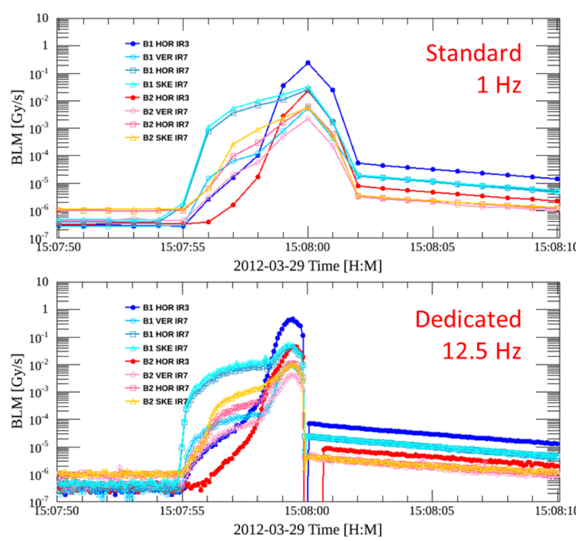


Figure 1: Comparison of the standard and dedicated data delivered to the Collimation system [courtesy of B. Salvachua and G. Valentino].

This development has resulted in a significant reduction of the beam time required to setup the collimation hierarchy [1]. In addition, it was found to be an excellent diagnostic tool that has been used successfully to study the time evolution of the losses in IR7 and IR3 during loss maps measurements as well as to study the halo diffusion and population.

* christos.zamantzas@cern.ch

## UFO Buster

The *Unidentified Falling Objects* (UFOs) are potentially a major luminosity limitation for nominal LHC operation [2]. In order to provide better and more detailed observation capabilities and to assist in the understanding of their mechanism and damage capabilities, a new dedicated buffer has been introduced in the processing Field Programmable Gate Array (FPGA).

This new dedicated *Capture* buffer allows a selection of the recording length and the data type, of either 40 $\mu$s integral with 512 samples per channel or 80 $\mu$s integral with 4396 samples per channel. This implementation was complement by a new client process referred to as *UFO buster*. This process detects abnormal losses in real time, triggers a timing event to freeze the FPGA buffer and initiates the collection of the high frequency data from the capture buffer.

## LIC Detector Development

During 2012 a vigorous program was followed to develop and characterise the Low-pressure Ionisation Chamber (LIC) detector. The aim was to provide a new type of detector to cover the sensitivity region between the standard Ionisation Chamber (IC) and the Secondary Emission Monitor (SEM) detectors. The first candidate installation of this new type will be part of the strategy for the mitigation of the injection losses.

As soon as the first batch of prototypes were produced, a set of these detectors were installed to observe losses from both LHC beams in parallel to the well-known IC detectors. In this way, it was possible to study their behaviour and reliability, to verify the calculated conversion factor to Gy/s and to validate the calculated thresholds.

Many issues were revealed with the first batch. This triggered several changes in the production and design parameters and additional detectors were installed during the following *Technical Stops*. For more information see also [3].

## Fault Analysis for Preventive Maintenance

The LHC BLM system is quite large, distributed and holds significant complexity. The necessity to provide a "fail-safe" system, which at the same time is able to achieve the required availability, required an elaborate design with a large number of additional processes that evaluate, collect and monitor the state of the system in real-time.

A typical example is the data reception process. This process is hosted at the entry stage of the processing FPGA and has been implemented in a way that, besides ensuring a correct reception, also provides a highly capable detection of erroneous transmissions.

Fig. 2 shows a report example of the automated analysis of the communication links, which provides statistics on the Cyclic Redundancy Check (CRC) and the loss of packets for each of the optical links, as well as the loss of synchronisation between the redundant links.

It becomes obvious that the recording and relaying of such information can be used to identify weaknesses or failing components and will provide a history to understand

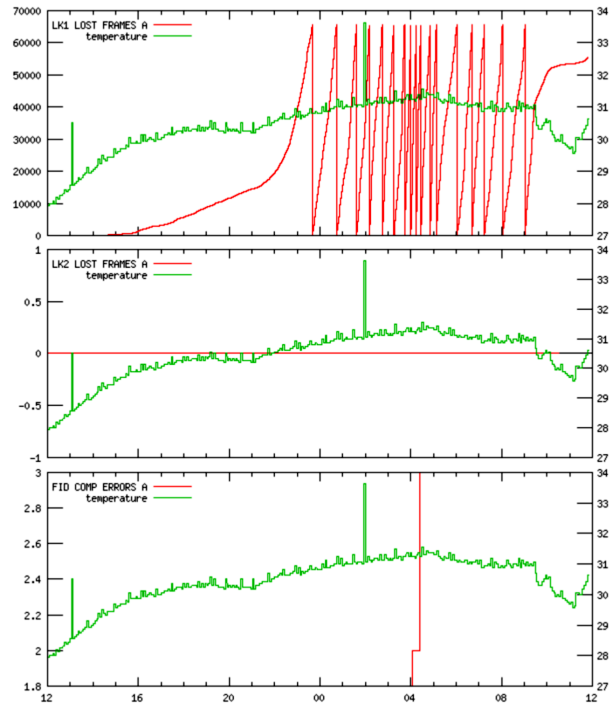


Figure 2: Example of the data transfer error reporting function for different types of checks presented over a period of 24 h (where red: check error count, green: temperature).

the events that forced an unintentional beam extraction request. Thus, a further effort has been made to use the gathered information in order to extract and provide the most relevant diagnostics. Several daily automatic analysis tasks are executed to asses the system's performance and state. In addition to the diagnostics of the communication links mentioned above there is an assessment of the detector response, the noise on the channels, the power supplies stability and many more.

Through the year these diagnostics provided input to the work planning of the technical stops and as a result several cards, detectors and cabling have been exchanged in the shadow of the interventions before their failure would affect the LHC availability. It should be further noted that the analysis tasks have shown that the errors in the optical link communications have increased significantly. This is also reflected in the unavailability of the system due to these errors. Their impact, as well as the additional mitigation measures under development, will be discussed in more detail below.

## Issue and Task Tracking

For the recording of the observed incidents and the actions performed, as well as the planning and management of the tasks over the technical stops, the JIRA project tracker [4], hosted at BE/CO servers, has been extensively used during 2012.

In summary, for the LHC BLM system more than 100 operational incidents were recorded and an equal amount of

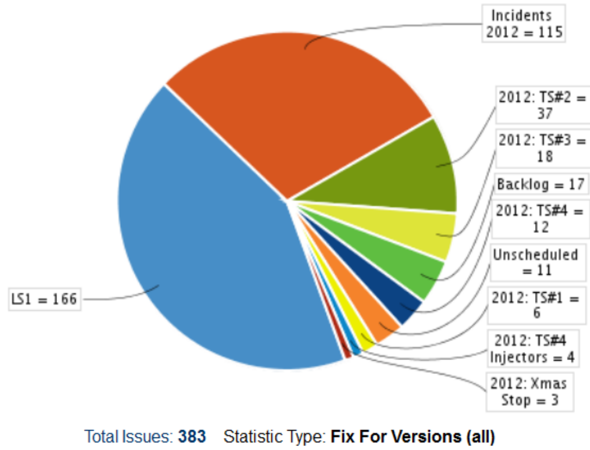


Figure 3: All issues and tasks recorded between March 2012 and March 2013 for the system classified by type.

tasks for the planning of the five *Technical Stops*. The tool is now also used for the planning of the first *Long Shutdown* (LS1). Fig. 3 shows a summary of all recorded issues and tasks classified by type.

### *Recorded System Faults*

The system performed as expected and issued abort requests in all cases that the measurements exceeded the predefined thresholds.

Nevertheless, internal system faults have caused an additional 31 unplanned beam abort requests in the operational period between March 2012 and March 2013. The majority, i.e. 20 requests, can be accounted to the communication links between the tunnel and the surface installations. The system utilises around 1600 optical links and the processing electronics have been designed to demand a beam abort in case no data was received during a 40 $\mu$s cycle for any of the channels declared as part of the MPS.

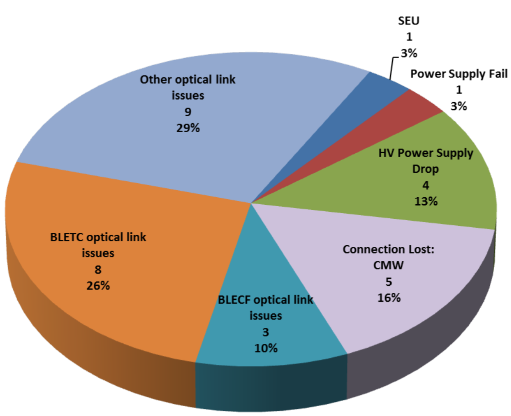


Figure 4: LHC BLM System fault events causing a beam interlock between March 2012 and March 2013.

Table 1: LHC BLM System fault events causing a beam interlock between March 2012 and March 2013.

| Failure Type | Occurrences | Percentage |
|---|---|---|
| SEU (surface) | 1 | 3% |
| VME Power Supply | 1 | 3% |
| HV Power Supply Drop | 4 | 13% |
| Connection Lost: CMW | 5 | 16% |
| BLECF optical link | 3 | 10% |
| BLETC optical link | 8 | 26% |
| Other optical link | 9 | 29% |
| Total | 31 | |

Table 1 and Fig. 4 summarise the faults that caused a beam abort request.

Furthermore, looking at the complete list of faults that occurred over the same period, including those that happened during the preparation of the machine, there are several types of error (see Table 2 and Fig. 5) that had an impact on the machine availability and required an intervention.

From this view of system faults it is clear that, apart from the communication link errors, two other groups of errors show a significant contribution. Those were generated by the *Sanity Checks* and the *Controls MiddleWare (CMW)*.

The Sanity Checks [5] are systematically executed at the preparation of the machine before beam injection. Their purpose is to ensure the integrity of each beam loss detector and its cabling. To achieve this, predefined limits have been set and if any channel is found to be outside these limits, the test will fail and the beam permit will not be released. To resolve such a situation an expert intervention is necessary. During the 2012 operation, 23% of the fault events were generated by SEM and LIC detectors failing to pass the Sanity Check. These detectors, even though they are not part of the MPS, delayed unnecessarily the start of the physics program.

Table 2: All LHC BLM System fault events recorded between March 2012 and March 2013.

| Failure Type | Occurrences | Percentage |
|---|---|---|
| SEU (surface) | 3 | 4% |
| VME Power Supply | 1 | 1% |
| HV Power Supply Drop | 4 | 6% |
| Connection Lost: CMW | 6 | 9% |
| Sanity Error: CMW | 9 | 13% |
| Sanity Error: IC | 3 | 4% |
| Sanity Error: LIC | 6 | 9% |
| Sanity Error: SEM | 10 | 14% |
| BLECF optical link | 7 | 10% |
| BLETC optical link | 11 | 16% |
| Other optical link | 10 | 14% |
| Total | 70 | |

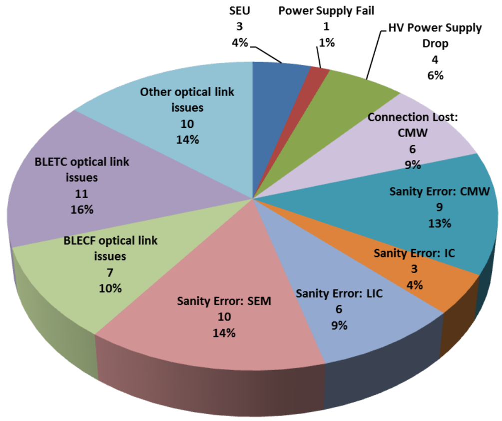


Figure 5: All LHC BLM System fault events recorded between March 2012 and March 2013.

The second group is related to CMW, whose purpose is to provide a common software communication infrastructure for the CERN accelerator controls. Partial or complete loss of CMW connection of the Front End Computers (FEC) with the control systems was responsible for 22% of the fault events recorded for the LHC BLM system.

Actions have been planned for LS1 to mitigate each of these types of system fault. These actions will be presented with the rest of the LS1 tasks in the following chapters.

## HARDWARE CHANGES DURING LS1

Several modifications are planned for the system components, which are distributed in all tunnel sectors, as well as in several surface buildings. The actions in the LHC tunnel come with additional complexity due to the restricted access.

### *Dismantling and Relocation of Detectors*

One of the main tasks during LS1 is the repair of the 1695 LHC magnet interconnects. The BLM system has detectors in the vicinity of the interconnects and in order to allow the intervention, all detectors and cable trays located in the arcs and dispersion suppressor regions have to be dismantled, i.e. approximately 2500 detectors in the arcs and of the order of 1000 detectors ($\approx$70%) in LSS regions.

Furthermore, detailed studies of the UFO characteristics showed that, in order to detect UFO events originating in the main dipoles, very low thresholds are required. Due to the positioning of all BLMs close to the quadrupoles, these thresholds would be very close to, or even below the system noise level. For this reason, it was decided to relocate 816 detectors in more appropriate positions that cover these blind spots, such to improve the overall protection (see also [6] for more information). To realise this task, a design and production of a new type of detector support, of signal and power cable extensions, as well as the cable trays to host them will be needed.

### *Modifications in the Tunnel Installation*

In the context of improving all noisy cable installations to provide better measurements, 40 multi-wire cables will be exchanged with cables of NES18 type. It is expected that this modification will reduce the externally induced noise of 240 detector channels and hense should allow to set more accurately the beam abort threshold levels.

To improve the stability of the acquisition crates, and to improve features that at the moment only work partially, 360 backplanes will be exchanged with a newly developed printed circuit board. Furthermore, 309 signal distribution boxes will be modified to allow a remote reset of each sector independently. Finally, the connection to the WorldFIP bus will be adapted to provide remote access to each individual card. These features will be extremely useful to reduce the number of tunnel accesses required for some type of interventions. To establish the WorldFIP connections in the Straight Sections additional electronics will be needed.

The High Voltage distribution network, used for biasing the detectors, have shown some weakness in areas with very high losses and caused some unintentional beam interlock events. For this reason, approximately 20 High Voltage distribution boxes in the identified areas will be modified. A prototype of a modified box, containing additional suppressor diodes and resistors, have been installed and tested in LHC towards the end of the operational period. It was found that the change was sufficient to mitigate the effect. Fig. 6 shows a picture of the position of the box in the tunnel. See also [7].

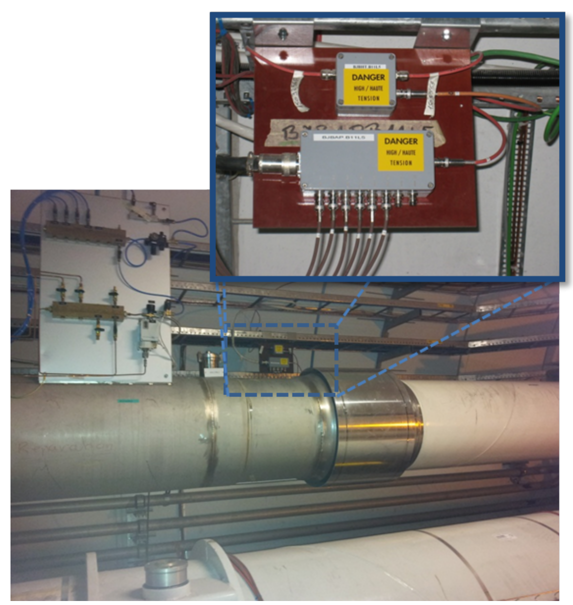


Figure 6: Picture of the High Voltage divider boxes.

### *Modifications in the Acquisition Electronics*

To mitigate issues observed with the acquisition modules (BLECF) a modification has been planned of all of the approximately 750 printed circuit boards. The modification will change the limit for the HV level drop detection flag. The detection level will be changed from 1370 V to 950 V to allow longer high steady-state losses (see also [7]).

The original level was chosen to simply confirm that the HV power supply is connected and active. Later this HV status information was included into the Software Interlock System. However, for this application, the level was too restrictive and has given several false alarms, some of them also leading to beam interlocks.

### *Modifications in the Surface Installation*

The surface installations are currently hosted in racks that are cooled by a forced vertical air flow traversing the different modules. This cooling provided poor temperature stability and the variation in the day cycle ranged from 5 to 10 °C. During the summer months, the modules often operated above 40 °C. This has been of particular concern, not only for the life expectancy of the electronics but also because of the impact of sudden temperature and humidity changes on the optical links.

For these reasons it was decided to replace all the racks with temperature regulated racks. Obviously the replacement will imply the removal and disconnection of the complete installation, i.e. crates, cables, and power supplies, but also the very tedious and delicate reconnection of all the fibre patchcords afterwards, i.e. approximately 1600 optical links connecting the distribution racks with the crates.

On the rear side of the rack, there are several daisy chain cables to control of the HV power supplies, to distribute the beam energy value received by the CISV module and to propagate the beam interlock signals to the CIBU modules. In the current configuration, these cables have to be disconnected each time before replacing a VME power supply. A new configuration is foreseen that will allow faster and more reliable interventions.

Finally, two new processing crates will be added to the 25 crates already employed, to optionally implement a *Dump-Inhibit during Injection* in the future. The additional racks, which are needed to host those crates, will be placed in the support buildings for Point 2 and 8. These two crates will be dedicated to host the detectors that are problematic during beam injection. This new configuration will allow, if needed, to deploy modified firmware on the installed modules that will filter beam interlock requests generated by this subset of detectors during beam injection (see also [8] and [9] for more information).

### *Modifications in the Processing Electronics*

The BLM system employs approximately 400 processing modules hosted in VME crates. All of them will need to be maintained in order to provide the required availability during the next operational period.

The maintenance will include repair or replacement of approximately 20% of the mezzanines modules and cleaning all 1600 optical adaptor and connector pairs. There has been a significant accumulation of dust on the connectors after five year following their installation. Fig. 7 shows an example of the dust accumulation on the optical connectors.

Further analysis of the recorded optical link statistics over the last operational period showed that 80% of the optical link errors and failures occurred in the upper redundant connection pair, i.e. links 1 and 2. This is a clear indication of a weakness in the design. To avoid a possible a common mode failure, link 2 and 3 will be swapped on all modules, i.e. the physical connection in hardware and in the logical mapping in firmware. In this way, we aim to improve the availability by removing the commonality and by sharing the weak links between the two pairs arriving in the Processing and Threshold Comparator (BLETC) module.

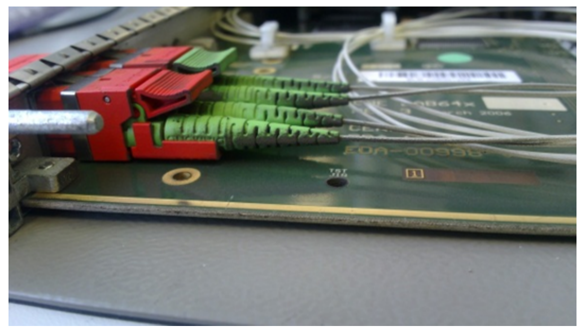

Figure 7: Example of dust accumulation on the optical link connectors.

## FIRMWARE CHANGES DURING LS1

The system employs three FPGA devices. Two of them are reprogrammable and their code will be modified during LS1.

### *Modification of the BLETC firmware*

The FPGA firmware modifications of the BLETC module aim to improve and extend the data delivered to external systems. The core protection mechanisms will remain unchanged since no weaknesses have been identified from the initial release.

One of the most important and mandatory modifications is to add compatibility with the new Linux based CPUs. This change implies the implementation of a new VMEbus core that provides the Multiplexed Block Transfer (MBLT) access mode. Moreover, to profit from the additional increase of speed, a new memory map optimized for block transfers is also necessary.

The buffers for the *Post-Mortem* system and *UFO Buster* will be increased in size to provide 43,690 samples per channel, profiting from the additional new CPU's performance.

An effort will be made to resolve an issue with the *XPOC* buffers by decoupling the buffers (i.e. the measurement trigger and recording) of the two circulating beams. Although it is not clear whether this separation is possible, mainly due to the limited resources in the FPGA, it would eliminate a major cause for the extraction analysis failures when the LHC operates with the two beam dump loops unlinked.

Finally, one last feature to be investigated is a further increase of the Collimation BBA measurement data rate, which is now at 12.5 Hz. A continuous stream of high frequency measurement data will be very useful, not only for the Collimation system but in many more cases of machine studies.

### *Modification of the BLECS firmware*

The Combiner and Survey (BLECS) module receives all the beam interlock requests from the BLETC modules in the crate. The module is also responsible for distributing the beam energy within the crates. Finally, when there is no beam in the accelerator, the module initiates all the test procedures and checks the results. The firmware modifications will focus on improving the survey features that had a significant impact on the system availability, on making the beam energy value reception and internal distribution more resilient with respect to external errors, and on upgrading the communication link with the FEC.

To improve the regular automatic system checks, modifications are planned to limit the level of the internally injected input current offset. This additional current is a self protection mechanism against unintentional blockage of the current-to-frequency converter circuit by radiation, but has been seen to be activated erroneously after some checks. A timeout will be added to the test duration, to avoid deadlocks caused by e.g. CMW communication errors. Especially for the improvement of the Connectivity Check, these additional modifications will allow to increase the range of the input values and the allowed threshold limits. This will benefit mainly the SEM and LIC detectors by reducing the false positives of the Sanity Check.

The impact of proton losses on the magnets depends on the loss duration and on the beam energy. For this, the processing electronics applies abort thresholds that depend on the beam energy, which is distributed by the control system. During operation, the received energy value has shown a couple of times abnormalities such as very quick changes. Those erroneous values were propagated to the processing modules where the logic chose the wrong threshold values with respect to the real beam energy circulating in the machine. Due to the short duration of these glitches, and the way the used energy and threshold values are logged, it was not possible to reconstruct afterwards the sequence of events using the information in the database. Thus, the modification of the code will aim to improve the energy value reception and the logging of the fast changes such that all the energy values received and propagated to the BLETC modules are logged in the database.

Compatibility with the new Linux based CPUs will need to be added, which, as for the BLETC's tasks, implies a new VMEbus core with MBLT access mode and a memory map that is optimized for block transfers.

Finally, the firmware will be adapted in the light of a possible inclusion of the *Dump-Inhibit during Injection* feature.

## APPLICATION CHANGES DURING LS1

The applications that support the configuration and that provide an operational view of the system are maintained and used by several sections and groups. Here we only present an improvement wish list.

The *Internal Parameters* application provides an interface to commit all the system parameters in the LSA database. In order to reduce erroneous entries from user actions, changes like automatically filling the serial numbers when a card is exchanged, or to step increase the connectivity check limits, could be added.

The *System Status* application could give a global overview and, when faults occur, display the system error cause. This will be beneficial to both the machine operators and system experts.

The *Monitor Factor* application could be improved by additional features like a viewer to show the history of changes, allowing to compare two points in time, and to roll back selected changes. All these modifications will contribute to a good overview of the system state after modification of the settings, especially those done temporary for MD studies or MPS checks.

Finally, a *System Management* application should be developed that a) will allow the generation of new monitors and their parameters in the database, b) will have the ability to load the settings to the electronics, and c) can initiate or abort system checks. Each of these actions already exists individually though generic applications, e.g. generation, trim and drive applications. However, these applications provide too many options not needed for the specific system, increasing the complexity and the probability for user errors.

## COMMISSIONING AFTER LS1

Due to the large number of modifications and the reinstallation of the complete system, a commissioning effort equal to the effort made during the LHC start-up will be required. All optical connections will need to be checked, the serial numbers must be updated in the database, the behaviour of each individual module will be measured, and finally new Connectivity check limits have to be calculated.

Since the majority of the detectors will have been disconnected and reconnected, with some of them even relocated, verification of the complete chain will be necessary by inducing a signal in each of the detectors with a radiation source.

Finally, similar to every start-up, the complete MPS check-list will need to be revalidated.

## SUMMARY

The majority of the system components will be completely removed, transported to the laboratories for refurbishment and later re-installed. All system modules will be modified and undergo maintenance with the aim to reduce failures and errors. All optical link patchcords will be redone after the replacement of the racks. The power network for the supply of the detectors will get additional components to improve the stability. The Sanity checks will be modified to provide less false positives.

A second set of changes will aim to improve the remote control of the cards and crates, the data collection and distribution for external systems and will improve ability to maintain the installation in an as good as new state.

Finally, a complete recommission will be necessary including a verification with a radiation source and complemented with all actions of the complete MPS checklist.

## ACKNOWLEDGMENT

The BLM team would like to express their gratitude and acknowledge the help and support provided by the colleagues of the BI Field Support Units and the Institute for High Energy Physics (IHEP) in Protvino, Russia, as well as the colleagues in the Controls and Operations groups of the Beams department.

## REFERENCES

[1] G. Valentino, R. Assmann, R. Bruce, S. Jackson, S. Redaelli, B. Salvachua, D. Wollmann, C. Zamantzas, "Fast Automatic Beam-based Alignment of the LHC Collimation System", 14th International Conference on Accelerator & Large Experimental Physics Control Systems (ICALEPCS2013), San Francisco, California, Usa, 6 - 11 Oct 2013.

[2] T. Baer, M.J. Barnes, F. Cerutti, A. Ferrari, N. Garrel, B. Goddard, E.B. Holzer, S. Jackson, A. Lechner, V. Mertens, M. Misiowiec, E. Nebot del Busto, A. Nordt, J. Uythoven, V. Vlachoudis, J. Wenninger, C. Zamantzas, F. Zimmermann, N. Fuster Martinez, "UFOs in the LHC: Observations, studies and extrapolations", 3rd International Particle Accelerator Conference 2012 (IPAC2012), New Orleans, LA, USA, 20 - 25 May 2012, pp.3936.

[3] E. Nebot Del Busto, B. Dehning, E. Effinger, V. Grishin, J. H. Alvarez, "Study of the Response of Low Pressure Ionization Chambers", 3rd International Particle Accelerator Conference 2012 (IPAC2012), New Orleans, LA, USA, 20 - 25 May 2012, pp.888.

[4] JIRA© `https://www.atlassian.com/software/jira` LHCBLM Project Issue Tracker `https://issues.cern.ch/browse/BIBML`

[5] J. Emery, B. Dehning, E. Effinger, G. Ferioli, C. Zamantzas, H. Ikeda, E. Verhagen, "LHC BLM Single Channel Connectivity Test using the Standard Installation", 9th European Workshop on Beam Diagnostics and Instrumentation for Particle Accelerators (DIPAC2009), Basel, Switzerland, 25 - 27 May 2009.

[6] E. Nebot del Busto, B. Dehning, E. B. Holzer, S. Jackson, M. Nemcic, A. Priebe, C. Roderick, M. Sapinski, C. Zamantzas, "Beam losses and thresholds", these proceedings.

[7] E. Effinger et al., "Modification of HV interlock of BLM to allow for 200kW losses", Machine Protection Panel, 12 December 2012, `http://lhc-mpwg.web.cern.ch/lhc-mpwg/MPP-Meetings/No73-14-12-2012/EEffinger_Proposal_for_modification_of_HV_interlock_20121214.pptx`

[8] C. Zamantzas et al., "LHC BLM system: Possible modification schemes to keep or to force TRUE the Beam Permit signal at Injection", Machine Protection Panel, 30 September 2011, `http://lhc-mpwg.web.cern.ch/lhc-mpwg/MPP-Meetings/No51-30-09-2011/MPP_LHCBLMSunglasses_20110930.pptx`

[9] W. Bartmann, M.J. Barnes, C. Bracco, E. Carlier, B. Dehning, L. Drosdal, R. Folch, B. Goddard, V. Kain, A. Lechner, F. Loprête, R. Losito, V. Mertens, E. Nebot del Busto, J. Uythoven, G. Vanbavinckhove, J. Wenninger, C. Zamantzas, M. Zerlauth, "Injection", these proceedings.