Interlocking strategy versus availability

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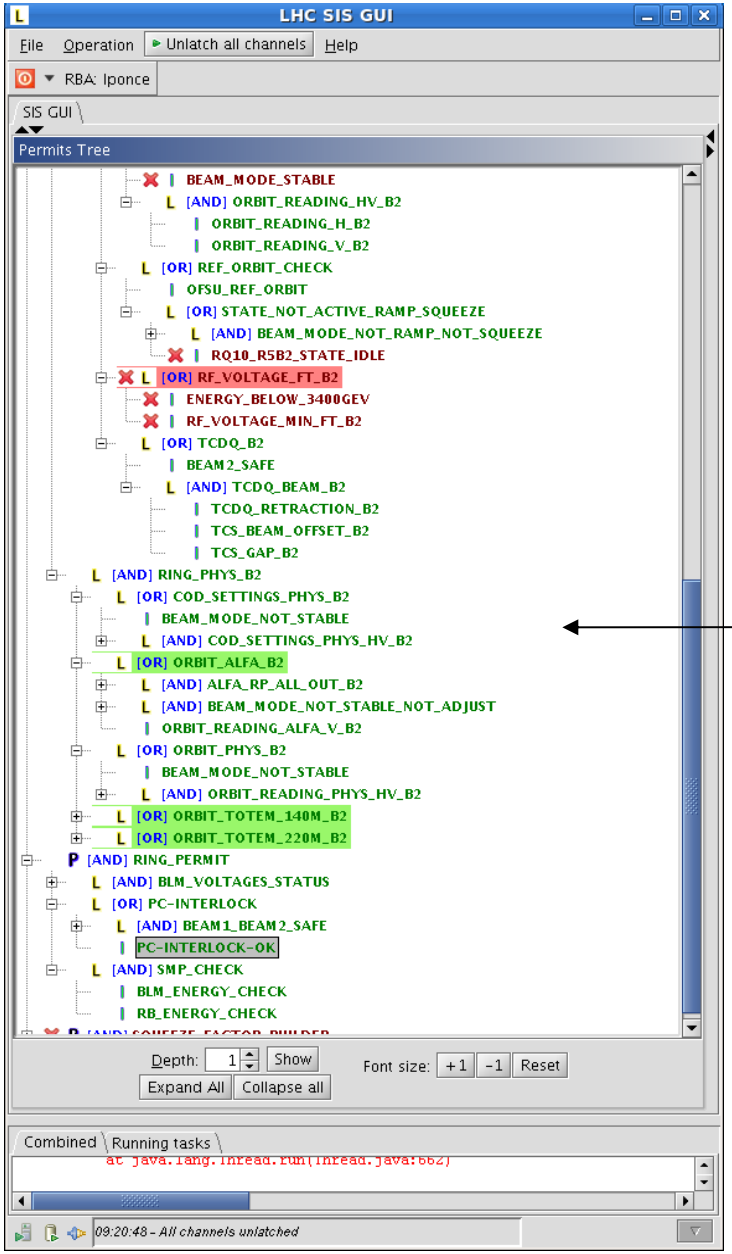
Introduction

- Interlocking strategy rely on the Beam Interlock System to prevent injecting or dumping the beam whenever a failure can provoke damage:
  - Entirely Hardware implementation
  - Highly reliable
- The Software Interlock System is providing further protection by implementing more complex logic,
  - All software, fast implementation
  - Highly configurable

Software interlocks versus Hardware interlocks



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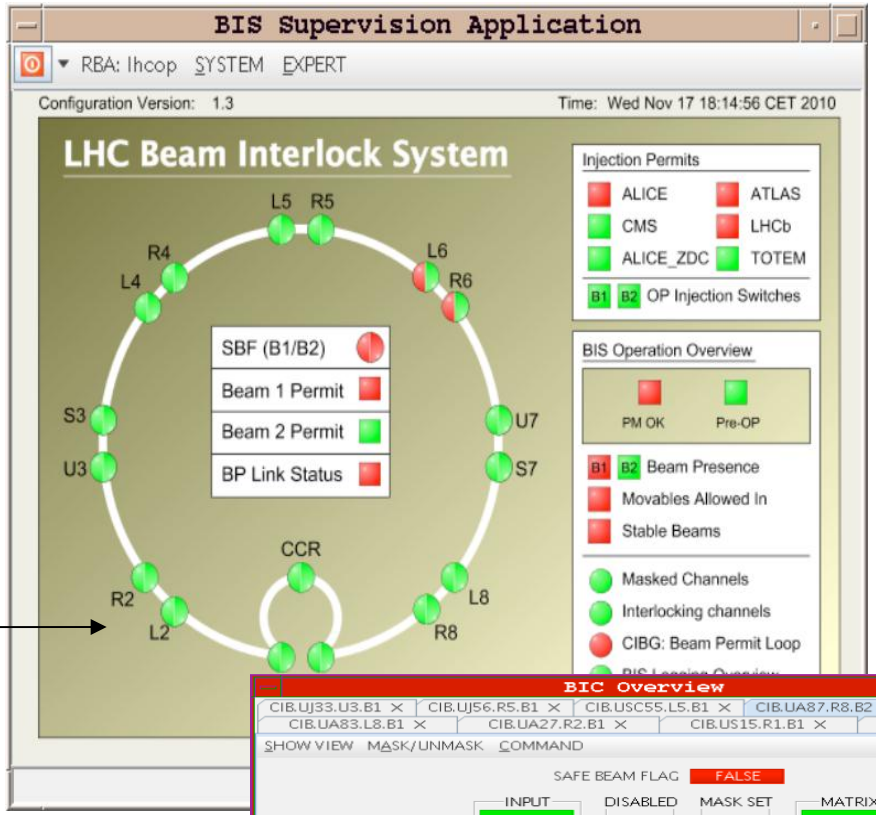
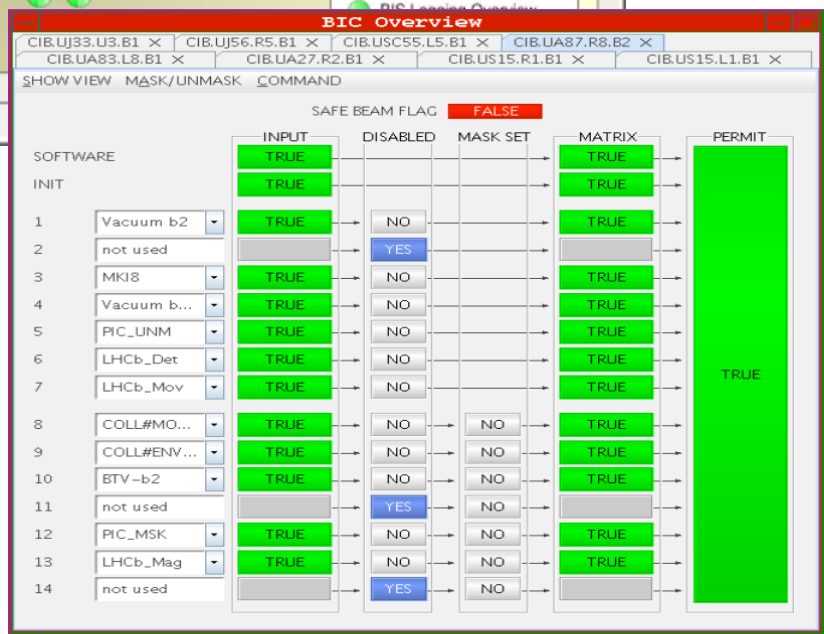




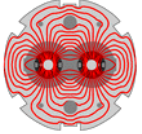
- SIS functionality and performance
  - Key features
  - SIS availability
  - List of interlocks
- SIS improvements:
  - Dumps due to loss of communication problems
  - SIS GUI and PM data
  - Beta* info
- Orbit interlocking:
  - General strategy for interlocking (SIS + OP experience)
  - Moving to PC interlocks

Software Interlock System

- SIS core functionality is to protect the machine through surveillance and analysis of several key parameters/ devices states published over the Common Middleware (CMW) protocol

- Interlocks tests are grouped in a hierarchical manner (Tree structure) with AND/OR logic

- The interlock results (permits) are exported to the Beam Interlock Controller devices
  - INJECTION (Beam 1, Beam 2 and both beams) permits exported to inhibit extraction(s) from SPS.
  - RING (Beam 1, beam 2 and both beams) permits exported to BIS to dump the beam(s)
  - *(POWERING permits (1 per octant) exported to the PIC to abort powering)*



SIS GUI

Permits Tree

- P [AND] INJ_B1_PERMIT
  - ADT_BUNCH_INTENSITY_B1
  - L [OR] BEAM_TYPE_B1
  - L [AND] BI_INJ_B1
  - L [OR] COD_SETTINGS_INJ_B1
  - L [AND] HANDSHAKE_TI2_OFF
  - L [OR] INJECTED_INTENSITY_OK_B1
  - INJECTION_BUCKET_B1
  - L [OR] INJECTION_MODE_B1
  - L [AND] IQC_B1
  - L [AND] MKI2_STATUS
  - L [OR] ORBIT_INJECTION_B1
  - L [OR] ORBIT_INJREGION_B1
  - L [AND] PC-CURRENTS-B1
  - L [AND] PC-STATES_B1
  - REQUEST_R1
  - L [AND] RF_INJ_B1
  - L [AND] TDI_GAP_B1
    - TDI_GAP_DOWNSTREAM_B1
    - TDI_GAP_UPSTREAM_B1
  - L [AND] XPOC_B1
- P [AND] INJ_B2_PERMIT
- P [AND] INJ_PERMIT
  - L [AND] BIC_PREOP_CHECKS
  - L [AND] DP_TRIM_RT
  - INJECTION_BUCKET
  - INJECTION_ENERGY
  - L [AND] PC-CURRENTS
  - L [AND] PC-STATES
  - L [AND] POST_MORTEM

SIS Structure

- Java based Software, Configuration files in XML for easy configuration

- LHC SIS has subscriptions to 2665 control system devices/parameters subscriptions (

- Interlock types:
  - *Initially*: used simple test logic comparison of acquired value to reference value (number or boolean) – hardcoded into configuration.
  - *Now*: more and more complicated interlocks (JAVA) that pull together multiple signals and DB references. Very flexible, but sometimes tricky to test (like orbit interlocks)!

- All interlock trees are evaluated every **2 seconds** (can be faster). The evaluation is triggered from the 1 second clock signal provided by the LHC timing system.

SIS Availability

- LHC SIS Core runs on dedicated HP server in the CCR.
  - The server is equipped with a timing card (CTRI).
- SIS processes of LHC have never failed during operation since 2008
  - SPS Server crashes were however observed in the 2009-10 shutdown. This was traced to a timing library (concurrency) and fixed.
- 77 dumps caused by SIS in the PM database in 2012 (B. Todd):
  - Not SIS failure as SIS followed the programmed logic

SIS dump cause	Creates PM	Ratio
CMW failure	yes	20%
Orbit feedback issues	yes	20%
Power converter faults	yes	15%
Beam Position measurements	yes	10%
Beam Loss Monitor HV	yes	10%
Others (wrong settings, masks...)	yes	25%

All events due to real interlocking conditions:
=>SIS did what it is asked to do

SIS Circulating Beam Interlocks

- Initial configuration in 2010

Test	Coverage	Comments
SMP energy	All RBs, SMP energy	0.2% to 2% (ramp or not)
SMP energy distribution	All BLM crates	Verify energy across all BLM crates
BETS	Q4 and MSD in IR6	
TCDQ – beam	Beam center in TCSG TCSG gap TCDQ-TCSG retraction	Achievable tolerances depend on orbit stability
COD integral	All arc Hor. CODs	dp/p < 0.2%
Orbit	All ring BPMs	Achievable tolerances depend on orbit stability
COD settings	All CODs in STABLE BEAMS	Achievable tolerances depend on reproducibility and variation in ramp & squeeze
COD trips	60 A CODs (not in PIC)	Dump if COD(s) trips and missing kick > threshold.

SIS Circulating Beam Interlocks

- Several interlocks added during operation to fill the holes

Test	Coverage	Comments
RF voltage	Energy > 3.4 TeV	More strict for min limit that the internal interlock
BLM HV	All BLM crates	Dump if HV link lost, complement for sanity checks
FB masks	RAMP & SQUEEZE	Dump if >25% of BPM disabled
Ref orbit	RAMP & SQUEEZE	Dump if zeroed/wrong ref orbit
PC interlock	All 60A CODs	Dump if 2 CODs out of tolerance

SIS Injection Interlocks

- Initial configuration in 2010

Test	Coverage	Comments
PC states	All PCs	
PC currents	RB, RQ, RD, MCBX	Extended to IPQ
QPS_OK	All circuits with QPS	
RF	Synchronization Cryo maintain	
BTV position	Ring and dump line BTVs	
Injection bucket	Abort gap and over-injection protection	
Injection mode		Avoid injecting with wrong mode
Energy		
(Pre)-op checks	XPOC, PM, IQC, BIC, SMP	
Triplet alignment	WPS in all IRs	

SIS Injection Interlocks

- Quite long list of added interlocks:

Test	Coverage	Comments
ADT bunch intensity		Check SPS intensity compatible with ADT settings
Beam type	Telegram and TT10	Check ions/proton configuration
TL handshakes	IP2 and IP8	Allow extraction till TED
Injected intensity	SPS intensity vs circ.	Added for intermediate intensity concept
Injection orbit	All BPMs	Tighter than orbit too avoid large oscillation
Orbit in injection region	BPM around TDIs	
TDI Gap		
RF RT trims	Radial modulation OFF	
MKI vacuum	Magnets and interconnect	
MKI temperature	MKI magnets	Max values (MCS) per magnets
Ventilation doors	Non LASS interlocked doors	

SIS Masking

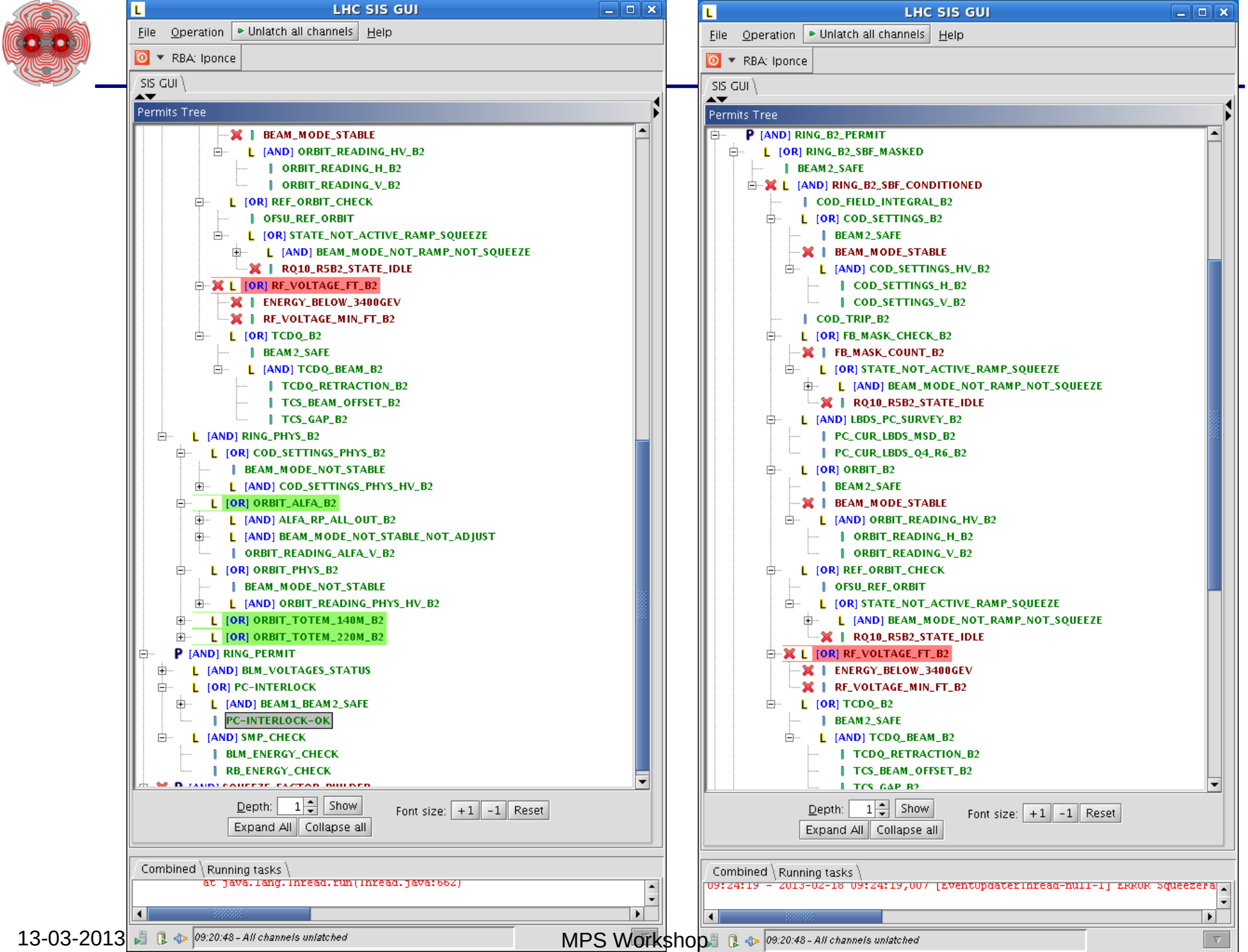
- Each interlock test is declared maskable or unmaskable (hardcoded):
- Masking done via the SIS GUI application:
  - Independent of Set-up Beam Flag.
  - Allowed for all holders of RBAC roles : LHC-EIC, MCS-SIS
- Some interlocks are "masked" through an OR logic with the safe beam flag conditions directly in the permit tree.
- Quite a long lists now of UNMASKABLE interlocks:
  - Orbits in physics,XPOC, PM_mach_protec permit, IQC injection oscillations
  - A lot more to come for 7TeV,
- Note: sequencer tasks available to unlatch/unmask tests automatically at beginning of cycle or during state changes
  - Not used yet for unmasking

SIS improvements : CMW communication

- ~ 7 dumps (injection and STABLE BEAMS), flagged as SIS failure but due to stop of the data streams:
  - Several cases due to PC FGCs stopping publishing data for
  - SIS dumps to avoid being blind for too long
- Traced back to CMW communication problems:
  - Due to “slow clients”, missing data for several seconds
  - SIS time-out increased from 20 seconds (2010) to around 120 s end of 2012
  - Clear degradation of the situation along the 2012 run
- Planned up-grade of CMW during LS1:
  - To protect against “slow” clients
  - + test bend?

SIS improvements : GUI

- Tree displays could be more user friendly:
  - Quite complex structure now with the safe-beam flag OR logic
- Need the possibility to monitor a parameters to ease diagnostics
- Masking.
  - So far masking rights apply to all (maskable) signals. Could consider making masking role-dependent.
  - Already deployed is the masking by pre-declared groups
- Protection of the subscription UI.
  - Avoid accidental stopping of data subscription – mostly availability, but also safety when there are timeouts.


LHC SIS GUI
File
Operation
Unlatch all channels
Help
RBA: Iponce
SIS GUI
Permits Tree
BEAM_MODE_STABLE
[AND] ORBIT_READING_HV_B2
ORBIT_READING_H_B2
ORBIT_READING_V_B2
[OR] REF_ORBIT_CHECK
OFSU_REF_ORBIT
[OR] STATE_NOT_ACTIVE_RAMP_SQUEEZE
[AND] BEAM_MODE_NOT_RAMP_NOT_SQUEEZE
RQ10_R5B2_STATE_IDLE
[OR] RF_VOLTAGE_FT_B2
ENERGY_BELOW_3400GEV
RF_VOLTAGE_MIN_FT_B2
[OR] TCDQ_B2
BEAM2_SAFE
[AND] TCDQ_BEAM_B2
TCDQ_RETRACTION_B2
TCS_BEAM_OFFSET_B2
TCS_GAP_B2
[AND] RING_PHYS_B2
[OR] COD_SETTINGS_PHYS_B2
BEAM_MODE_NOT_STABLE
[AND] COD_SETTINGS_PHYS_HV_B2
[OR] ORBIT_ALFA_B2
[AND] ALFA_RP_ALL_OUT_B2
[AND] BEAM_MODE_NOT_STABLE_NOT_ADJUST
ORBIT_READING_ALFA_V_B2
[OR] ORBIT_PHYS_B2
BEAM_MODE_NOT_STABLE
[AND] ORBIT_READING_PHYS_HV_B2
[OR] ORBIT_TOTEM_140M_B2
[OR] ORBIT_TOTEM_220M_B2
[AND] RING_PERMIT
[AND] BLM_VOLTAGES_STATUS
[OR] PC-INTERLOCK
[AND] BEAM1_BEAM2_SAFE
PC-INTERLOCK-OK
[AND] SMP_CHECK
BLM_ENERGY_CHECK
RB_ENERGY_CHECK
Depth: 1
Show
Expand All
Collapse all
Font size: +1 -1 Reset
Combined
Running tasks
09:20:48 - All channels unlatched
LHC SIS GUI
File
Operation
Unlatch all channels
Help
RBA: Iponce
SIS GUI
Permits Tree
[AND] RING_B2_PERMIT
[OR] RING_B2_SBF_MASKED
BEAM2_SAFE
[AND] RING_B2_SBF_CONDITIONED
COD_FIELD_INTEGRAL_B2
[OR] COD_SETTINGS_B2
BEAM2_SAFE
BEAM_MODE_STABLE
[AND] COD_SETTINGS_HV_B2
COD_SETTINGS_H_B2
COD_SETTINGS_V_B2
COD_TRIP_B2
[OR] FB_MASK_CHECK_B2
FB_MASK_COUNT_B2
[OR] STATE_NOT_ACTIVE_RAMP_SQUEEZE
[AND] BEAM_MODE_NOT_RAMP_NOT_SQUEEZE
RQ10_R5B2_STATE_IDLE
[AND] LBDS_PC_SURVEY_B2
PC_CUR_LBDS_MSD_B2
PC_CUR_LBDS_Q4_R6_B2
[OR] ORBIT_B2
BEAM2_SAFE
BEAM_MODE_STABLE
[AND] ORBIT_READING_HV_B2
ORBIT_READING_H_B2
ORBIT_READING_V_B2
[OR] REF_ORBIT_CHECK
OFSU_REF_ORBIT
[OR] STATE_NOT_ACTIVE_RAMP_SQUEEZE
[AND] BEAM_MODE_NOT_RAMP_NOT_SQUEEZE
RQ10_R5B2_STATE_IDLE
[OR] RF_VOLTAGE_FT_B2
ENERGY_BELOW_3400GEV
RF_VOLTAGE_MIN_FT_B2
[OR] TCDQ_B2
BEAM2_SAFE
[AND] TCDQ_BEAM_B2
TCDQ_RETRACTION_B2
TCS_BEAM_OFFSET_B2
Depth: 1
Show
Expand All
Collapse all
Font size: +1 -1 Reset
Combined
Running tasks
09:20:48 - All channels unlatched

SIS improvements : PM

- Post Mortem files triggered on beam dumped event and log files:
  - But data mining quite painful
  - no details in case of complex JAVA coding interlocks, ex. orbit interlocking
- Improvement:
  - Need a kind of PM module, giving details on the triggered tests

SIS improvements: Beta*

- SIS using Quadrupoles current in IPs to derive the actual Beta* at each IP.
  - Published to the Safe Machine Parameters (used by collimators)
  - Read back from timing to cross-check with reference table
- Calibration curves hard-coded in SIS configuration files (one per IP):
  - Worked very well for normal optics (monotone current change during the squeeze): nominal, HighBeta
  - Does not work for ATS optics
- Proposal:
  - Migrate the calibration curves to LSA settings
  - Also migrate the IPQ used to allow flexibilty for different squeeze

Orbit interlocking

- Complex interlocking logic to limit global orbit excursion and catch un-detected bumps (COD settings):
  - Distributed systems: reference+ tolerance+ enable flag per BPM/COD
  - Beam mode dependent: different tolerances along the cycle
    - stable beams : ± 2.5 mm IR1,2,5,8, ± 0.6 mm elsewhere
    - other modes : ± 6 IR1,2,5,8, ± 1.2 mm elsewhere
- Trigger beam dumps when 10 BPM/2 kicks per beam/plane out of tolerance
- Worked very well for standard operation, but several problems during special fills (VdM scans, injection optics collisions...):
  - Need to open the tolerances (LSA trims)
  - Very flexible, too much?
- Proposal to remove the CODs settings checks as now redundant with the PC interlock

PC interlock

See Kajetan's presentation

- Check during all beam process that CODs current within tolerance:
  - Trigger beam dumps when 2 kicks per beam/plane out of tolerance
- Settings stored in a reference beam process in LSA (clones from PC BP)
- Change of reference triggered by timing events:
  - Allow complex COD settings change that occurs during ramp and squeeze
- Had few failure cases:
  - Example functions launched for other test (RF test during ramp down)
  - Bug during hypercycle change, fixed

- For the time being, only CODs are monitored, could be extended to all magnets

SIS to HW interlocks?

- TCDQ interlocking:
  - Planned modifications of TCDQ during LS1 will allow to remove the SIS interlocks
  - + Collimators with integrated BPMs
- TDI gap interlock?
- CODs interlocking transferred to PC interlocks after LS1
- What else?

- Following the workshop presentations, seems to be some more Software interlocks to come.

Conclusion: SIS and MPS

- SIS is a reliable solution for different classes of interlocks:
  - Injection interlocks: reliability less critical.
  - Complex interlocks involving multiple systems.
  - Interlocks for distributed systems like orbit.
  - Quick solutions for un-expected situations.
- Even if it is all software:
  - Safety will never be SIL3… but availability of the system during the last years is impressive
- Will profit of LS1 to improve interface with PM and operators
- Few interlocks will be moved to HW after LS1, but probably more will come to SIS