



Nikolaos TRIKOUPIΣ TE-CRG-CI

Design and prototyping of the heater supply board

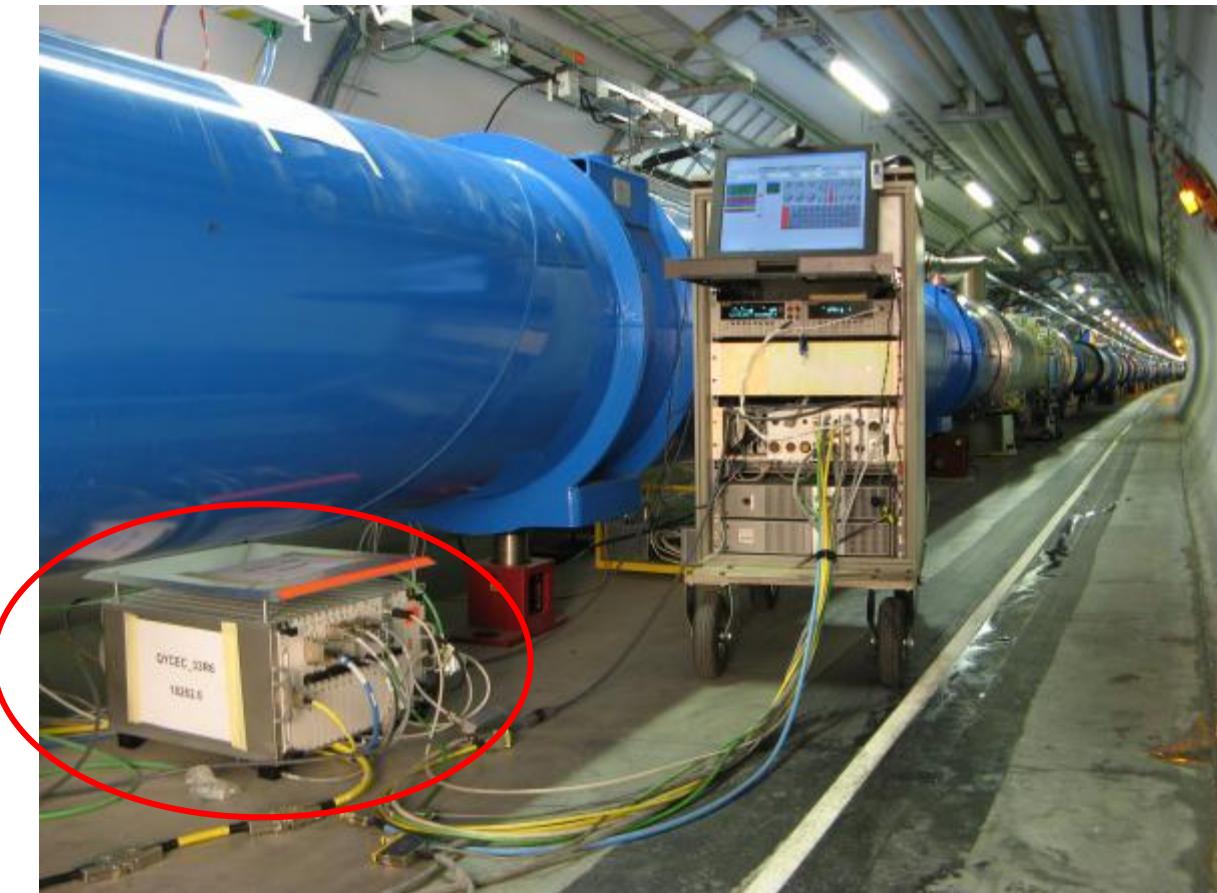


Contents

- The cryogenics crate
- Data flow
- Heater board - Theory of operation
- Comparisons: Existing design & Consolidations
- Prototyping



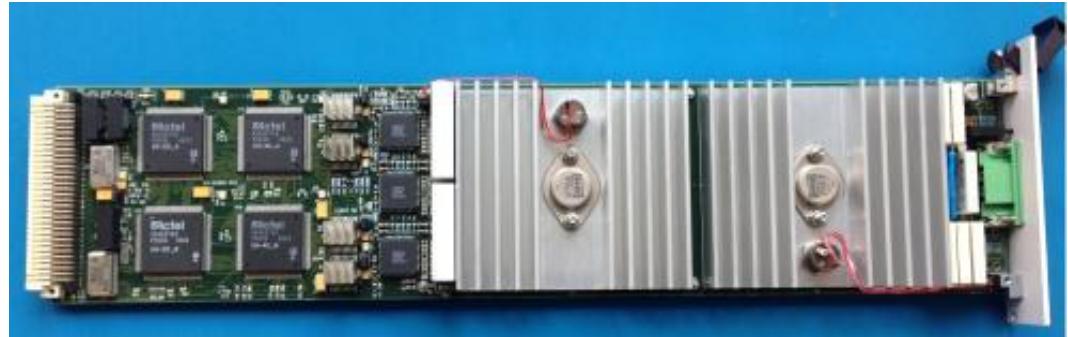
The cryogenics crate



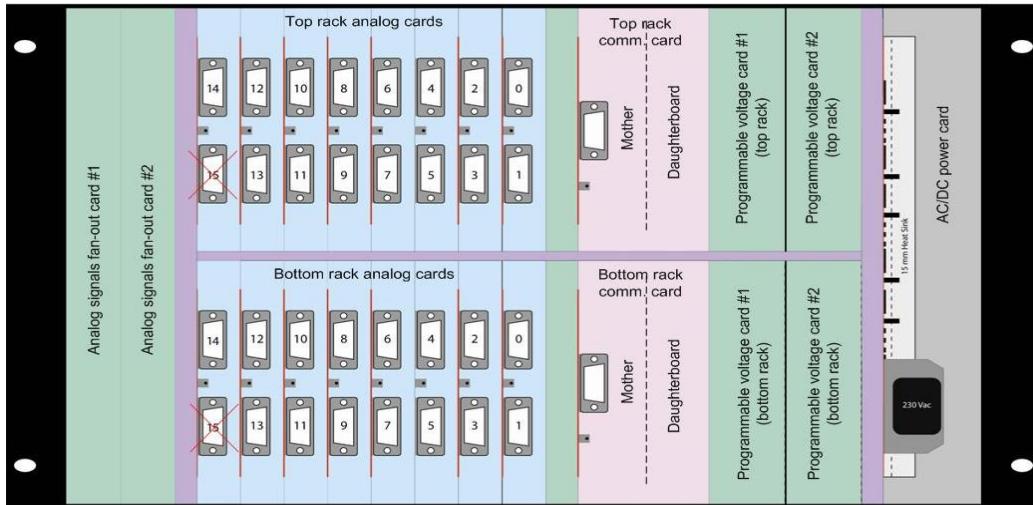
The cryogenics crate



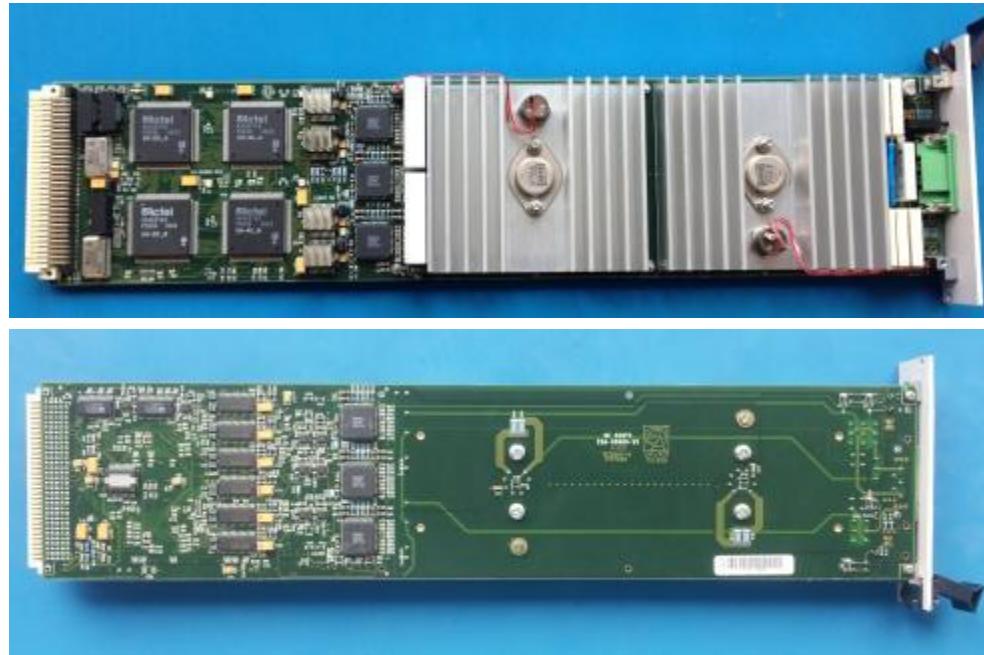
The cryogenics crate



The Electrical Heater (EH) card



The electrical heater card

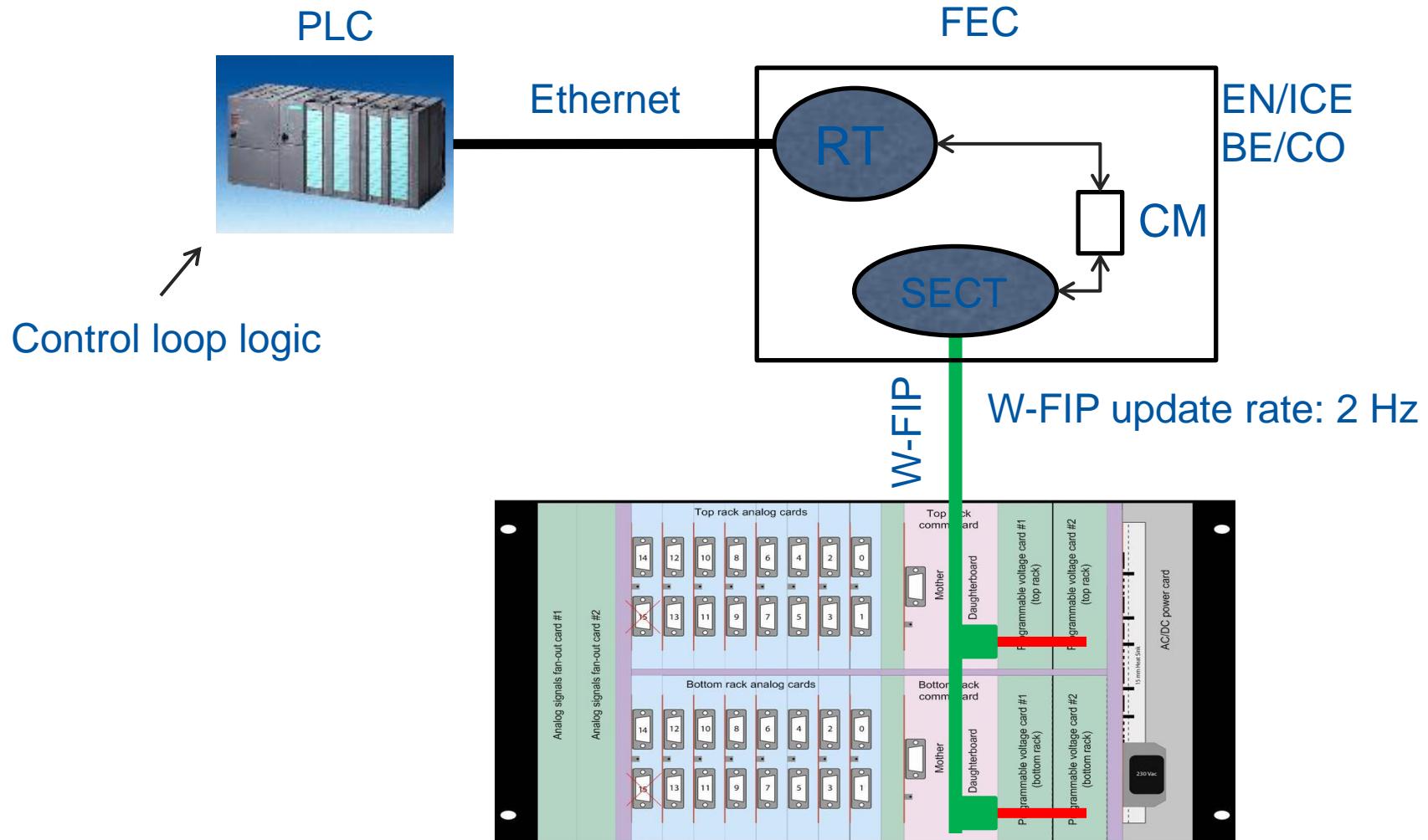


The Electrical Heater (EH) card

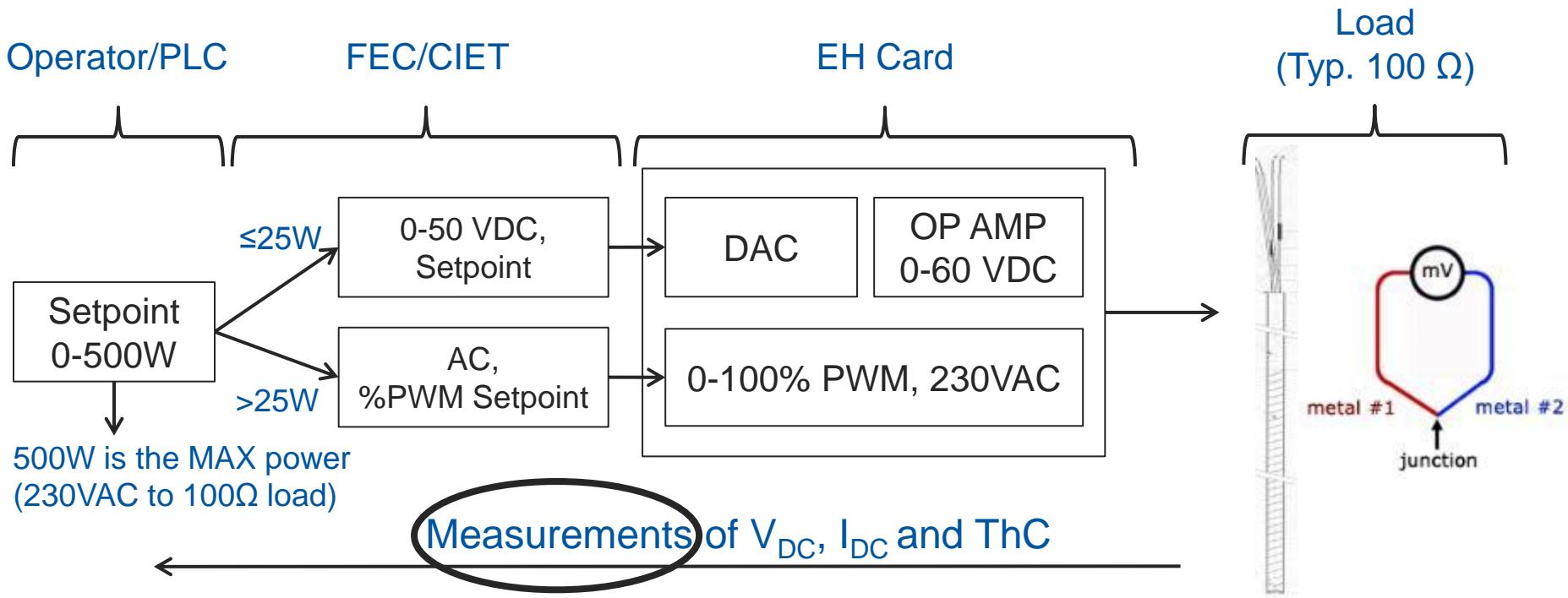
Purpose

- Deliver power to resistive loads by 0-60 VDC or 230 VAC PWM (Pulse Width Modulation).
- Provide measurements of V_{DC} , I_{DC} and thermocouple protection.

PLC - EH card communication



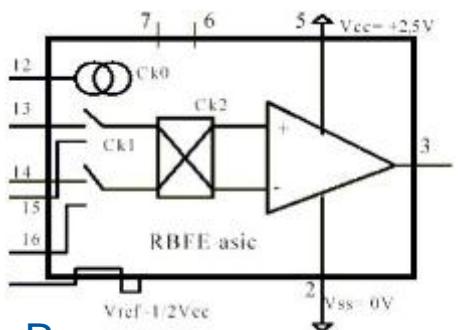
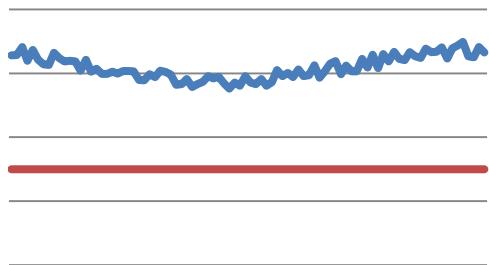
Theory of operation - Existing



- Provide DC/AC power
- Calculate ThC, V_{DC} and I_{DC}
- 2 Identical channels (Top/Bottom)

Theory of operation - Measurements

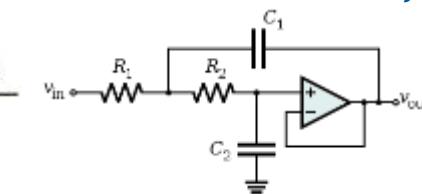
Input voltage
Reference voltage



Removes

1. Offset, common mode errors
2. Gains & gain errors
3. % of radiation effects

Sallen-Key
Low pass filter
Fc:159Hz, Q=0.5, $\zeta=1$



ADC

1024 samples
per position (40msec)

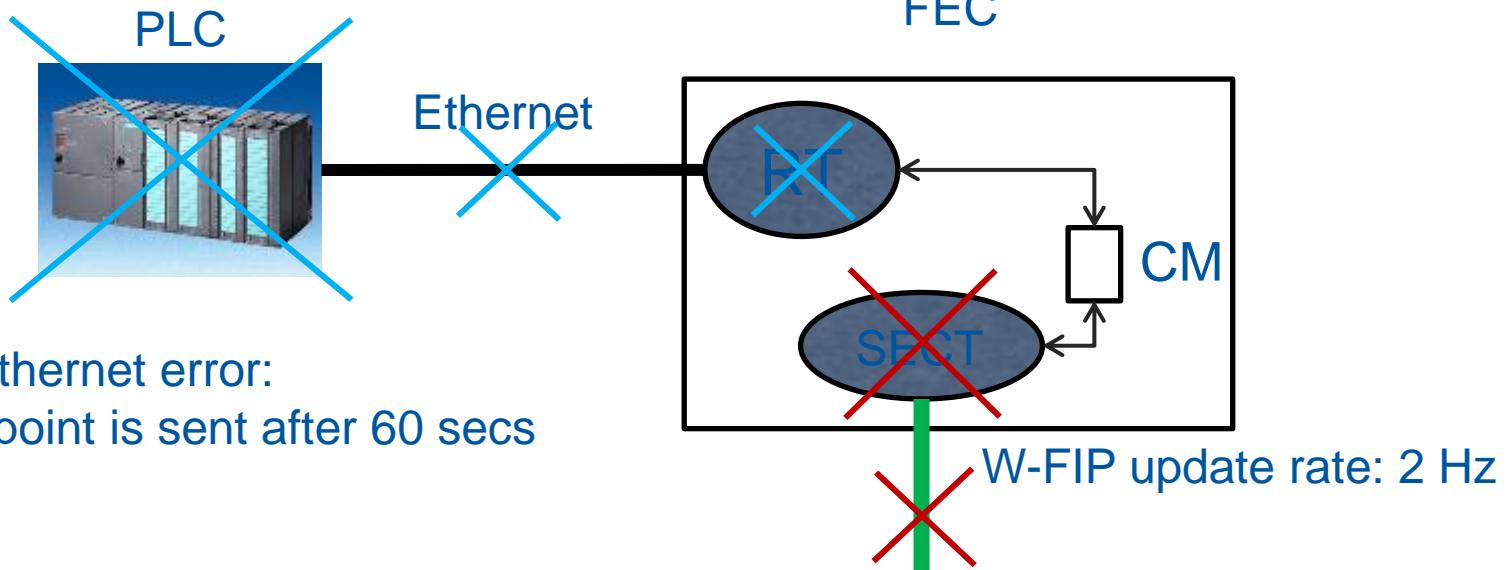
Simultaneous measurements of ThC, V_{DC} and I_{DC}



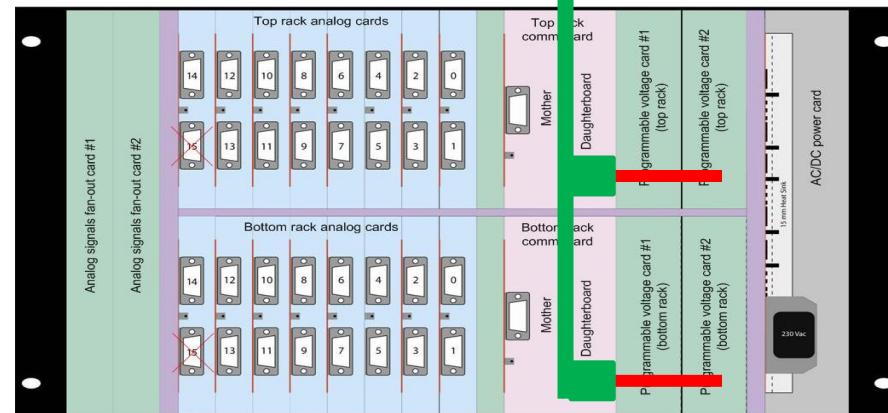
Existing design issues & Consolidations



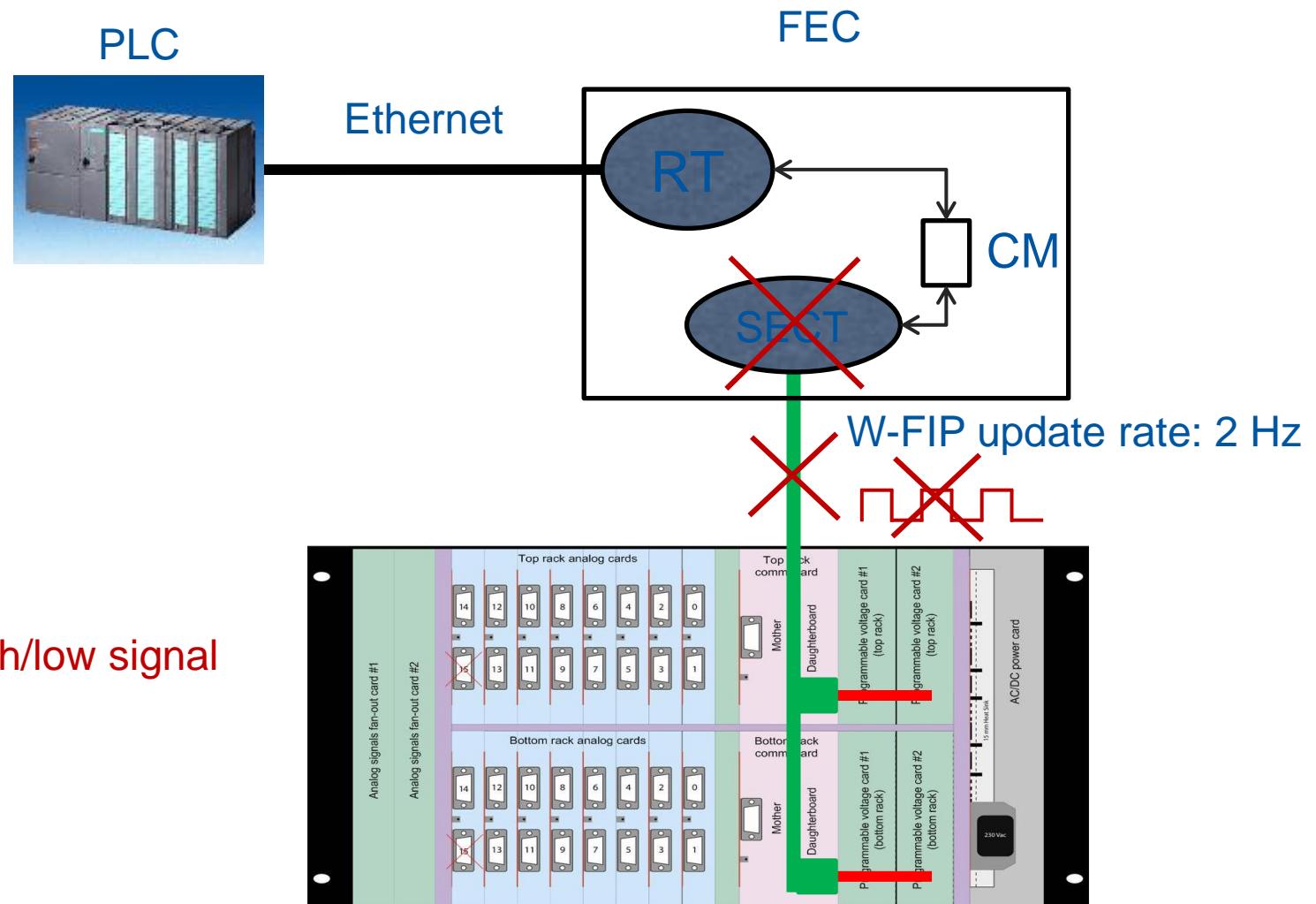
Communication lost - Existing



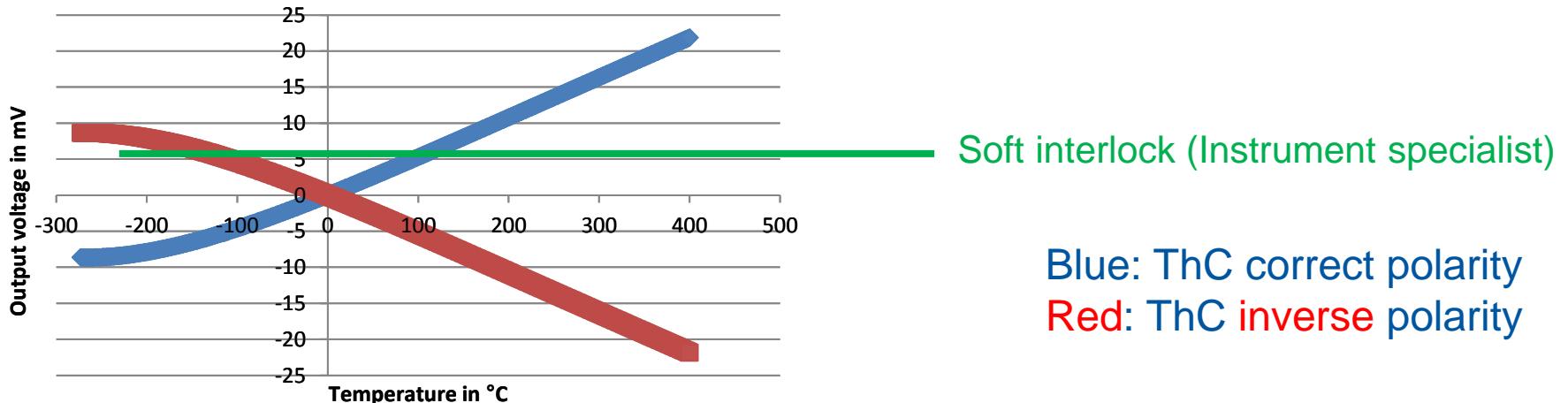
In case of failure,
The EH cards operates
with the latest setpoint



Communication lost - Consolidation

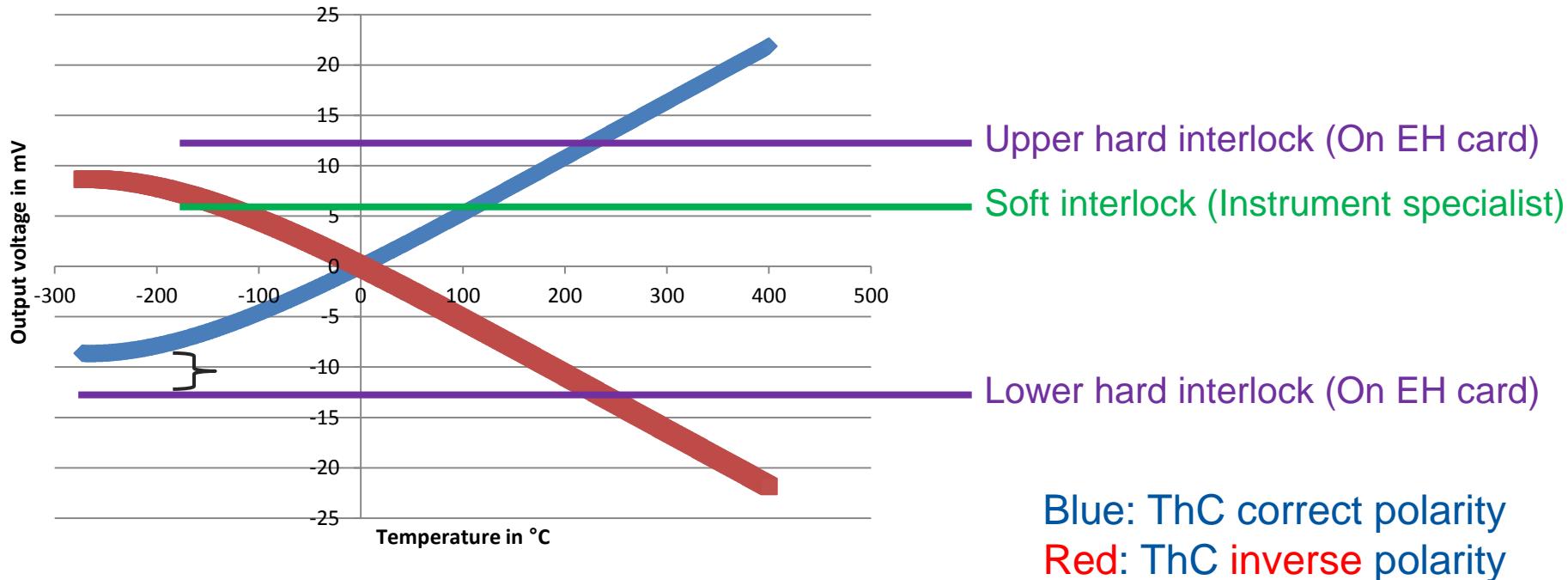


Thermocouple - Existing



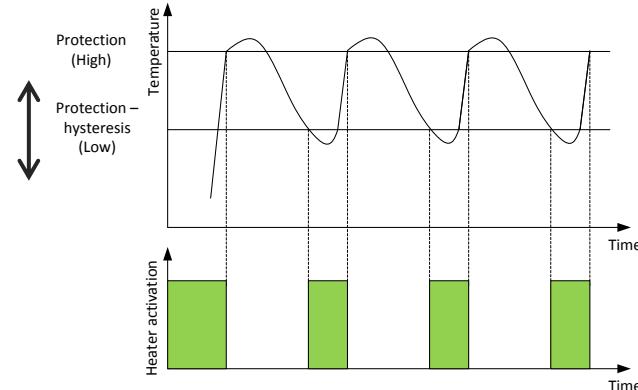
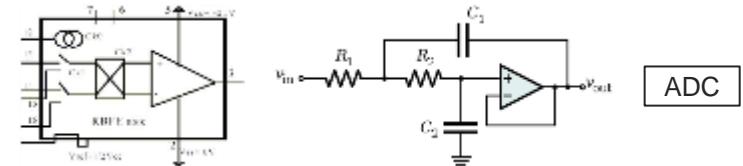
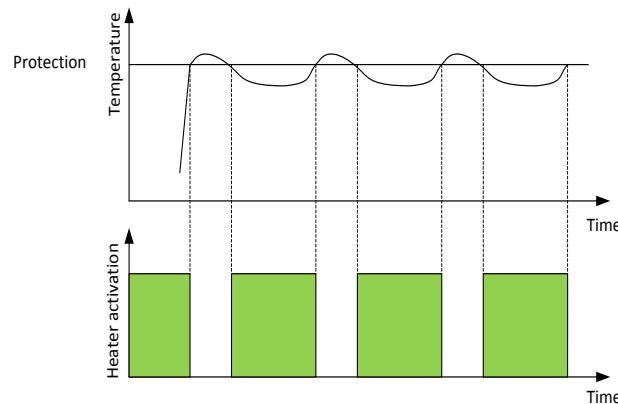
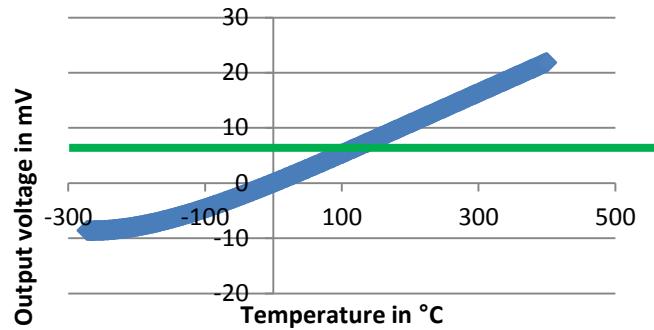
- Uncontrolled heating during LHC installation (April 2007)
- Due to a combination of tests on the CIET-FEC and not properly wired thermocouple protection (inverse)
- Not attributed to a problem of the communication

Thermocouple - Consolidation



- The **soft interlock** is set by the **instrument specialist** through the communication card
- The **hard interlocks** are set **on the EH card**

Auto Enable Mode - Existing



With hysteresis
(Feature not used)

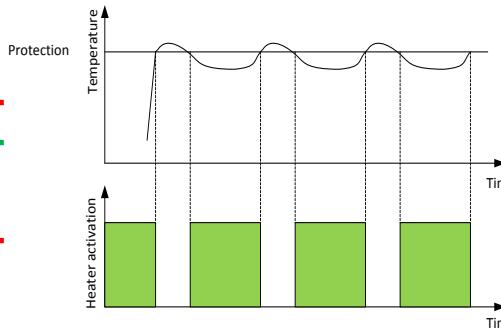
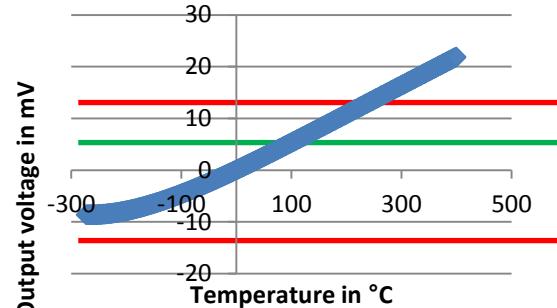
Consolidation request:

- Provide INTERLOCK functionality
- Provide ENABLE/DISABLE functions

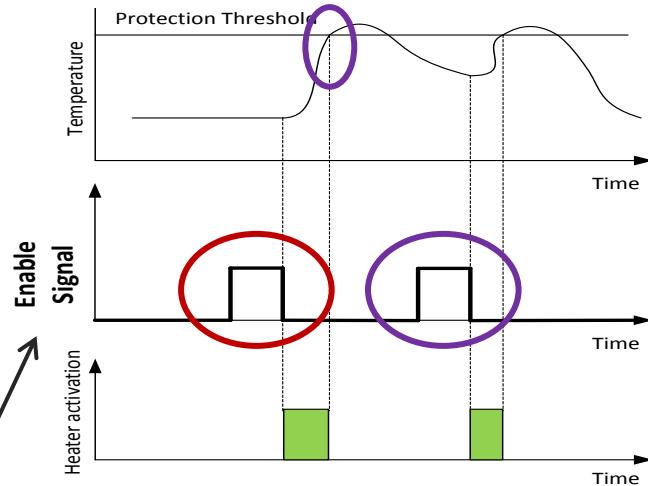
Interlock – New

EH card to support 2 modes of operation:

Auto
Enable

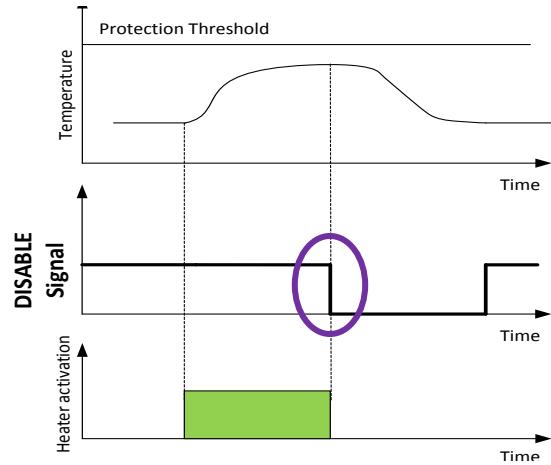


Manual
Enable



Operator ENABLE command after
a **reset/startup** and **interlock protection**

Manual
Disable

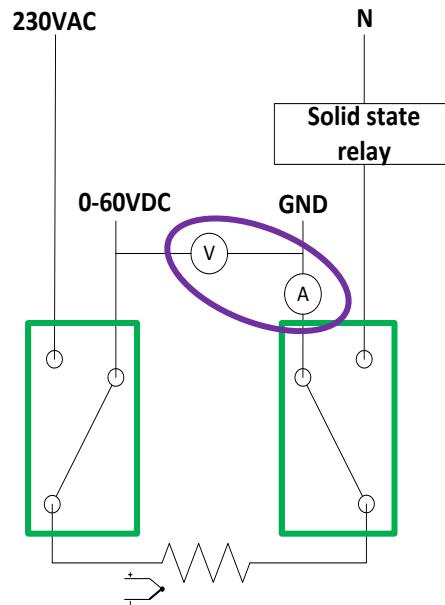


Operator DISABLE command to
deactivate and **disconnect** the load

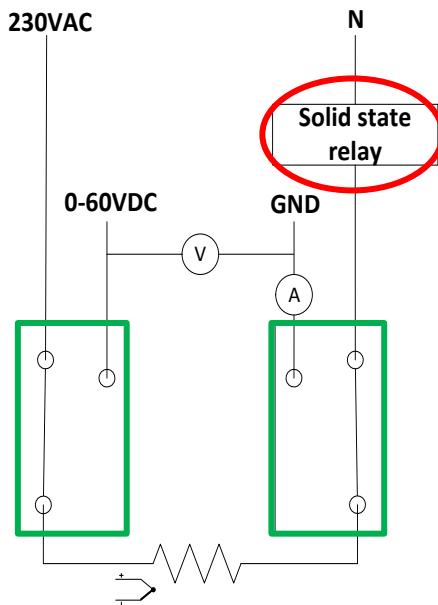
AC/DC mode - Existing

*Per channel

DC mode



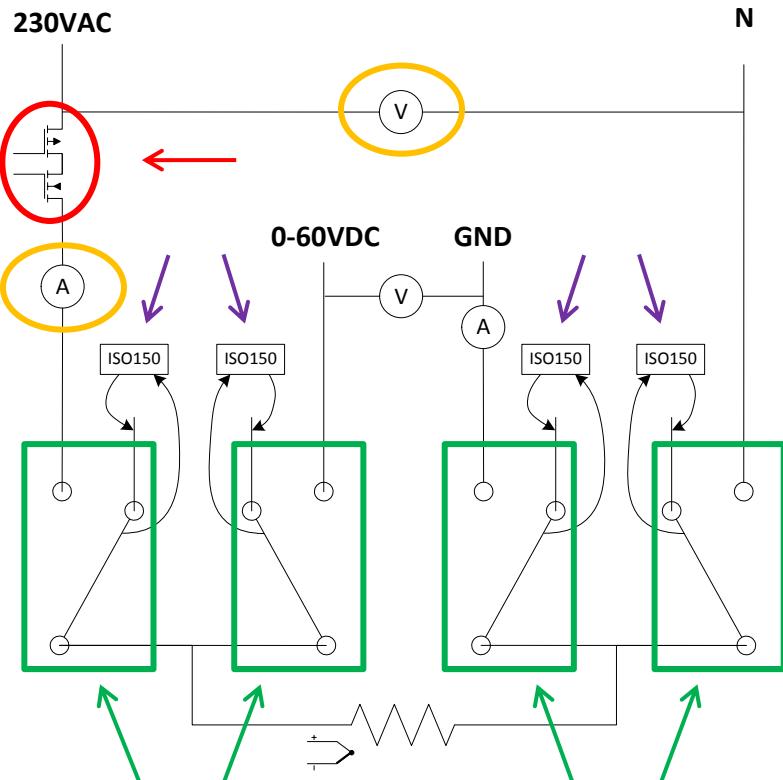
AC mode



- No **relay failure identification** exists. On failure, card destruction may occur.
- Load is connected to either **DC** or **AC**.
- Power calculations only in DC.
- **Solid state relays are not rad-tol and will stop operating (be always OFF) after dose accumulation.**
- Works without problem in protected areas.

AC/DC mode - Consolidation

*Per channel



Contact positional monitoring

- Use of isolation digital couplers

PCB Relay with forcibly guided contacts according to EN 50205 type B

- Double connection is not possible

AC mode is rad-tol

- Use of rad-tol NMOS power MOSFETs

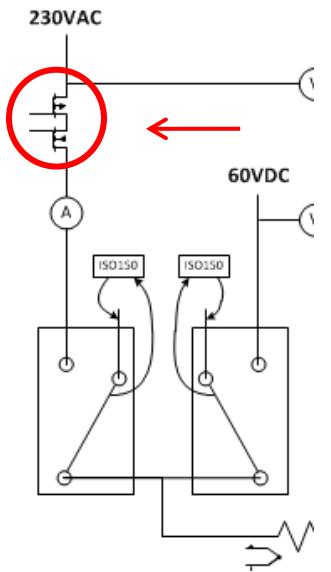
V_{AC} & I_{AC} measurements

Requirement for Beam Screen Heaters:

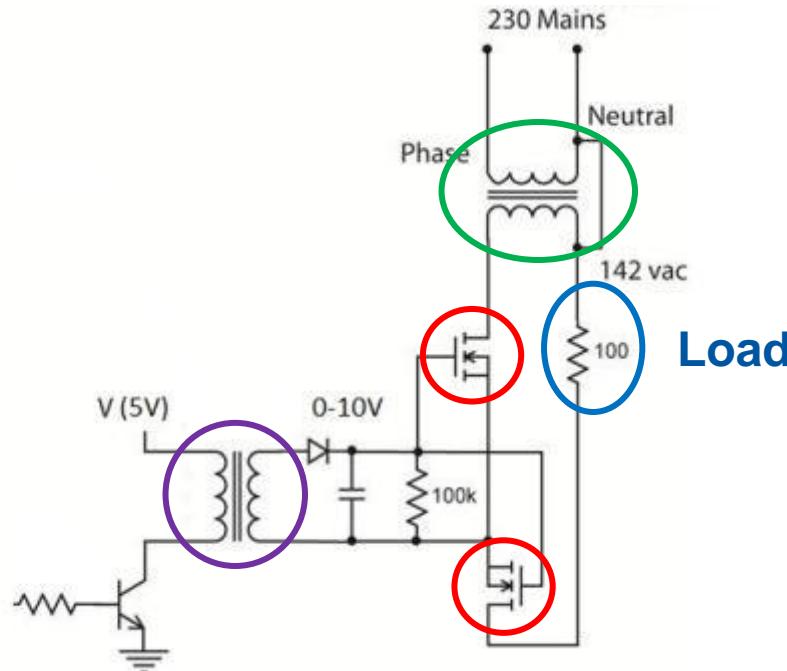
provide AC power up to 200W with beam OFF

(Provide DC power up to 25W with beam ON)

Rad-tol AC mode



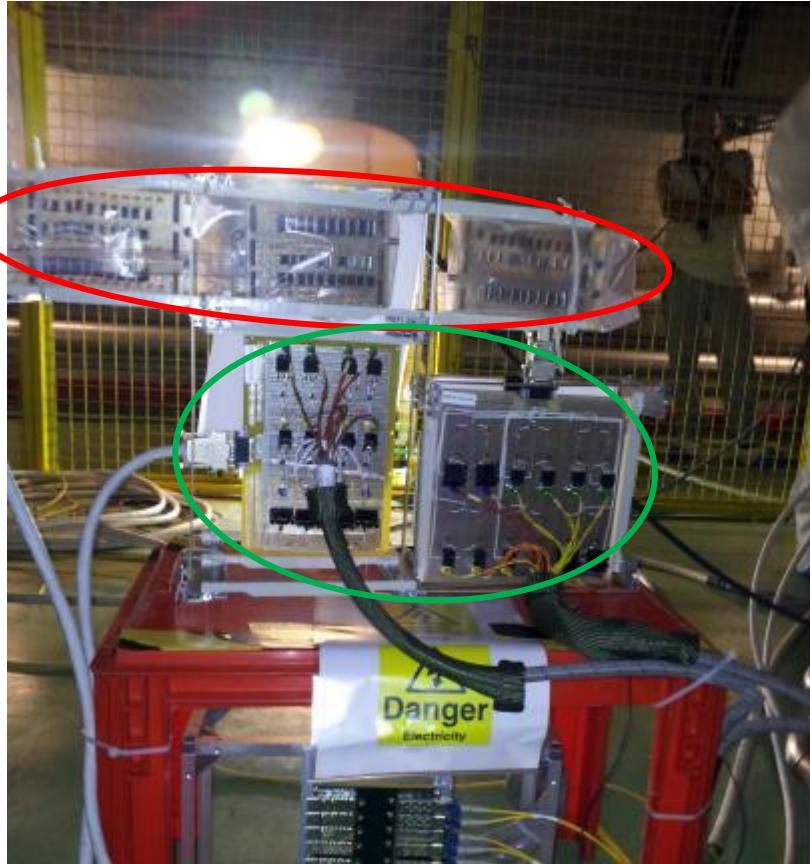
75 kHz square pulse
from FPGA



*AC/DC relays not shown

- 2 power MOSFETS for AC mode
- Isolation from the EH card digital circuitry using a PCB transformer (5V to 10V)
- A step-down transformer will be used to reduce the AC voltage (142VAC -> 200W max)

Rad-tol AC mode – Qualification (1)



MOSFET Types Tested

T1: FCA36N60NF	600V,	36A,	0.095 Ω
T2: STFI10NK60Z	600V,	10A,	0.65 Ω
T3: FDP7N60NZ	600V,	6.5A,	1.25 Ω

From each type:

- 30 in **passive** mode
- 8 in **active** mode (connected to 230VAC & 130Ω)

T1, T2, T3: No failures in passive mode

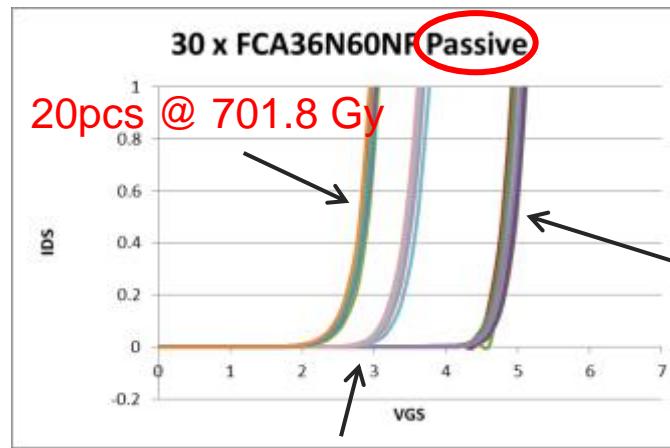
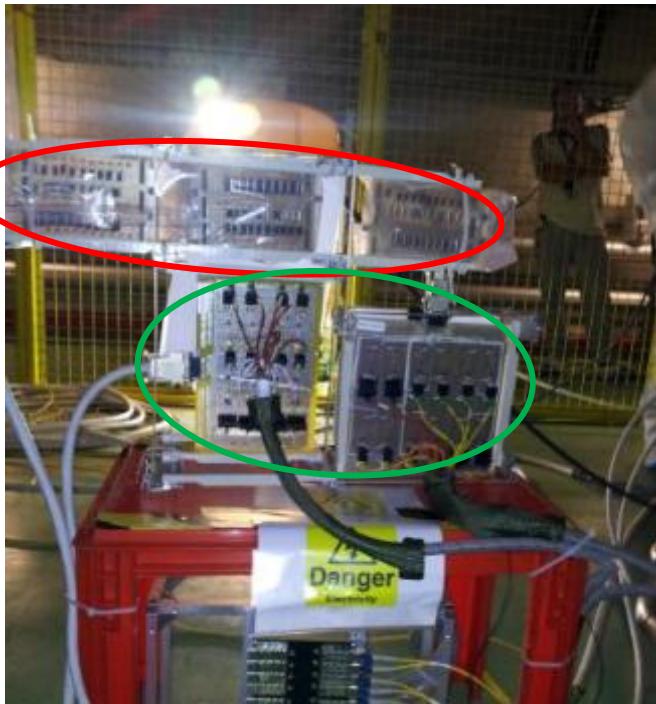
T1 only: No failures in active mode

LHC conditions:

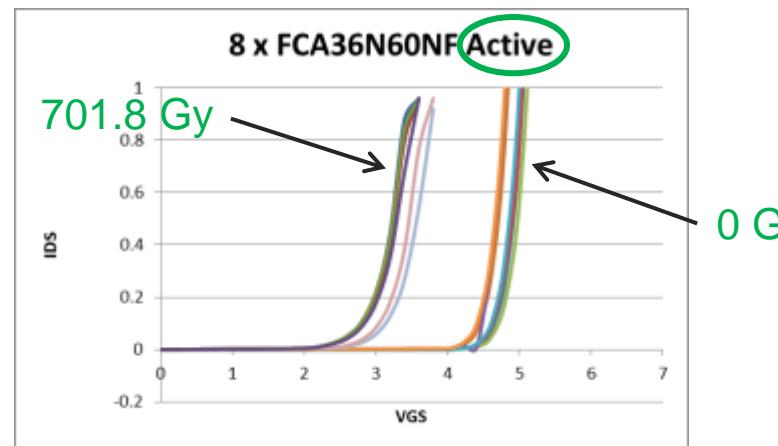
*AC mode to be used with beam OFF
MOSFETs to be operated at 142VAC*

CNRAD: 701.8 Gy, Neutrons: 6.94 e¹², Hadrons: 4.89 e¹² LHC at crate locations 2-100 Gy/y

Rad-tol AC mode – Qualification (2)



T1



CNRAD: 701.8 Gy,
Neutrons: 6.94×10^{12} , Hadrons: 4.89×10^{12}

AC supply to load - Consolidation

Existing $\xrightarrow{230\text{VAC}}$



The 230VAC of the load is common to the crate AC supply

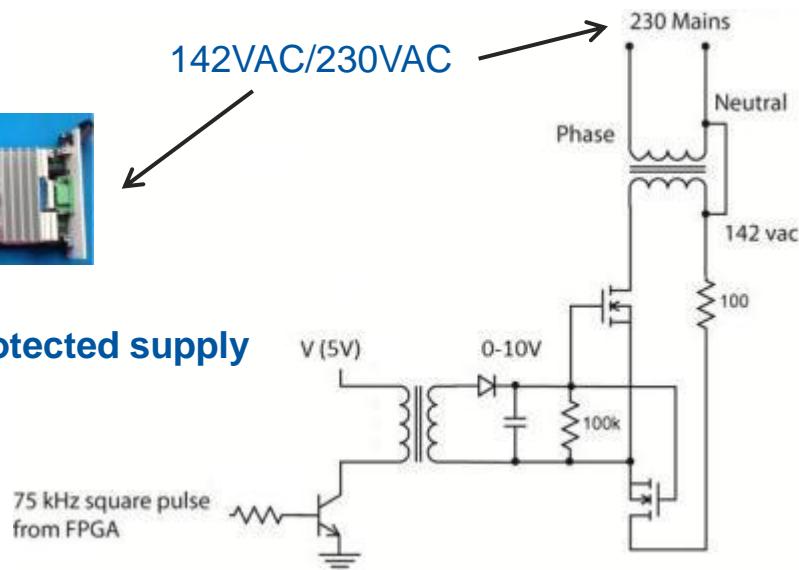
In the past, overcurrent of 230VAC has led to:

- Crate and full rack (3 crates) power loss

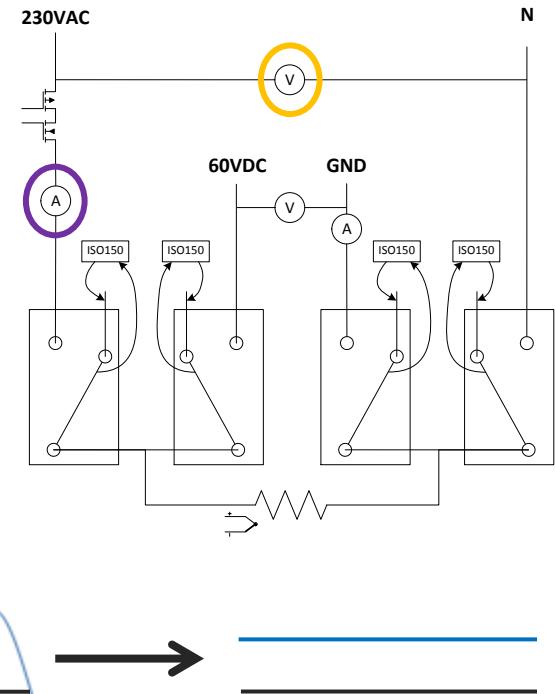
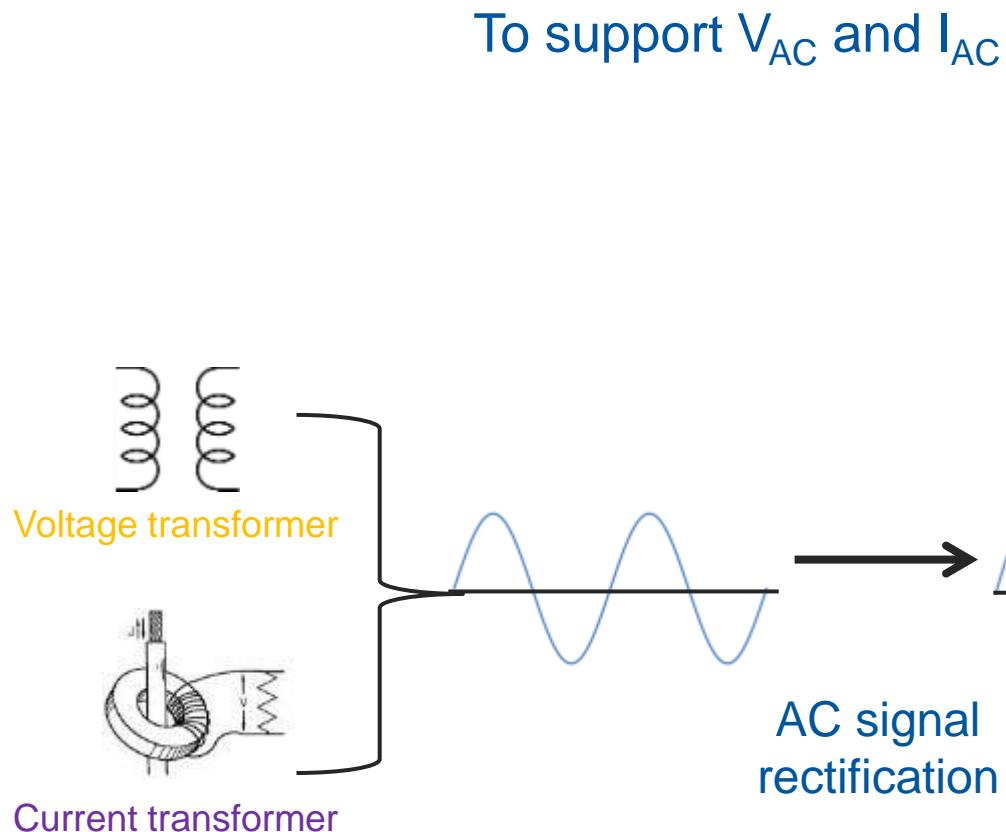
Consolidation



The 142VAC/230VAC from an **independently protected supply**



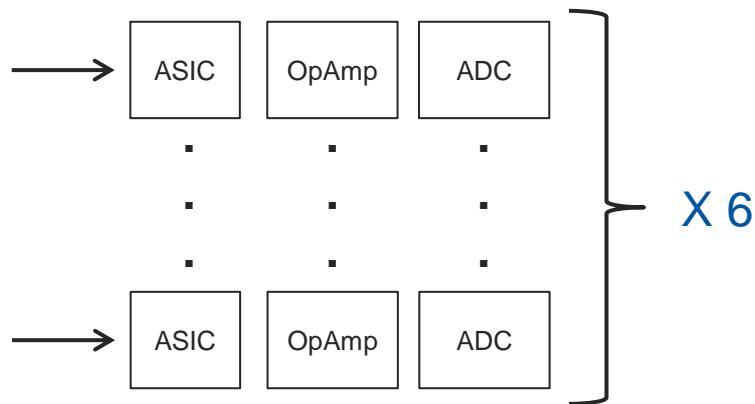
Measurements on AC - New



Analog switches – In evaluation

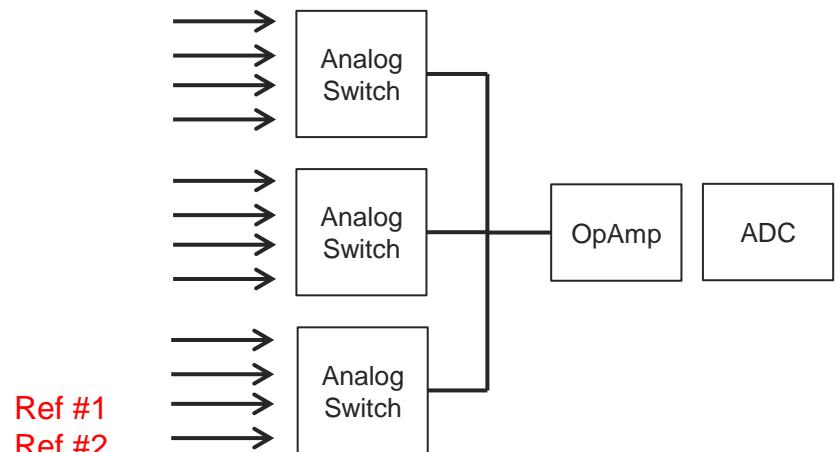
Existing version

6 simultaneous measurements
(V_{DC} , I_{DC} , ThC) x 2 Channels



New version

10 circular measurements
(V_{DC} , I_{DC} , V_{AC} , I_{AC} , ThC) x 2 Channels



Use of analog switches:

- Component reduction: (approx. 9 ADC, Op amps, ...)
- Reduced power consumption, thermal dissipation, space, ...
- ADC weakest point (up to 500 Gy, 10 fold current increase)

Analog switches - Qualification

Name/Manufacturer	SW06 (Analog Devices)	HS-201HSRH (Intersil)	RHD 5920 (Aeroflex)
Type	Quad SPST JFET analog switch	Quad SPST CMOS analog switch	16-Ch analog mux
RadHard Tech	No	Yes	Yes
Cost per card	7.5\$ (3 x 2.5\$)	234.9\$ (3 x 78.3\$)	340\$ (1 x 340\$)
Dose	---	3000 Gy	10.000 Gy



CNGS: Testing the Analog Devices SW06

18 in **active** mode (72 channels)
6 in **passive** mode (24 channels)

Dose: 347.5 Gy, Neutrons: 3.44 e^{12} , Hadrons: 2.42 e^{12}

CNGS: SW06 Seems to be OK.
Tests planned at PSI, Zurich (24th FEB 13)

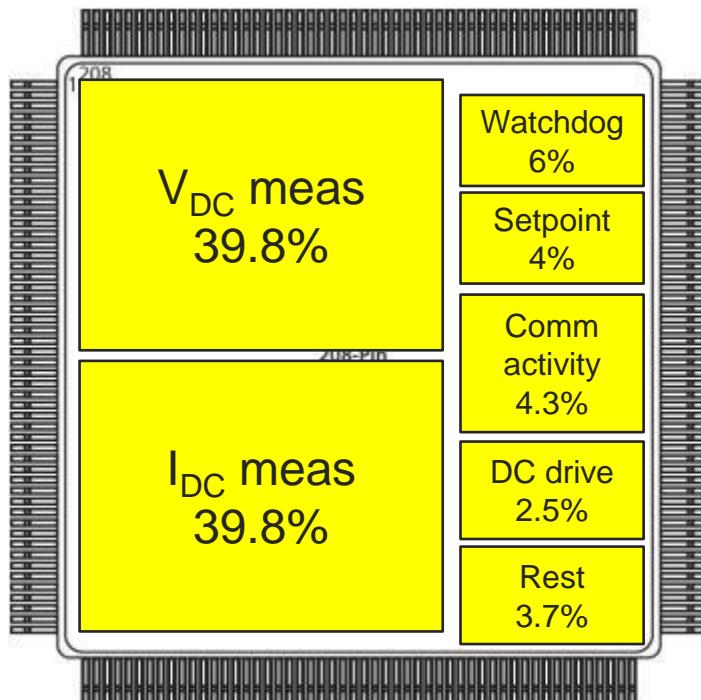
Use of COTS SW06 switch will result in savings of ~450CHF

FPGA utilization – Existing (1)

2 FPGAs per channel

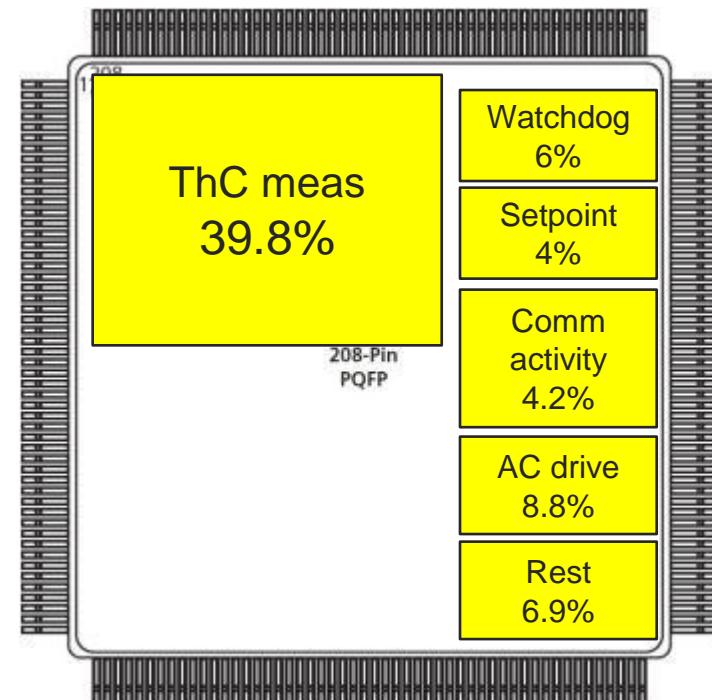
Part: Actel/Microsemi antifuse A54SX72A-PQ208

FPGA #1



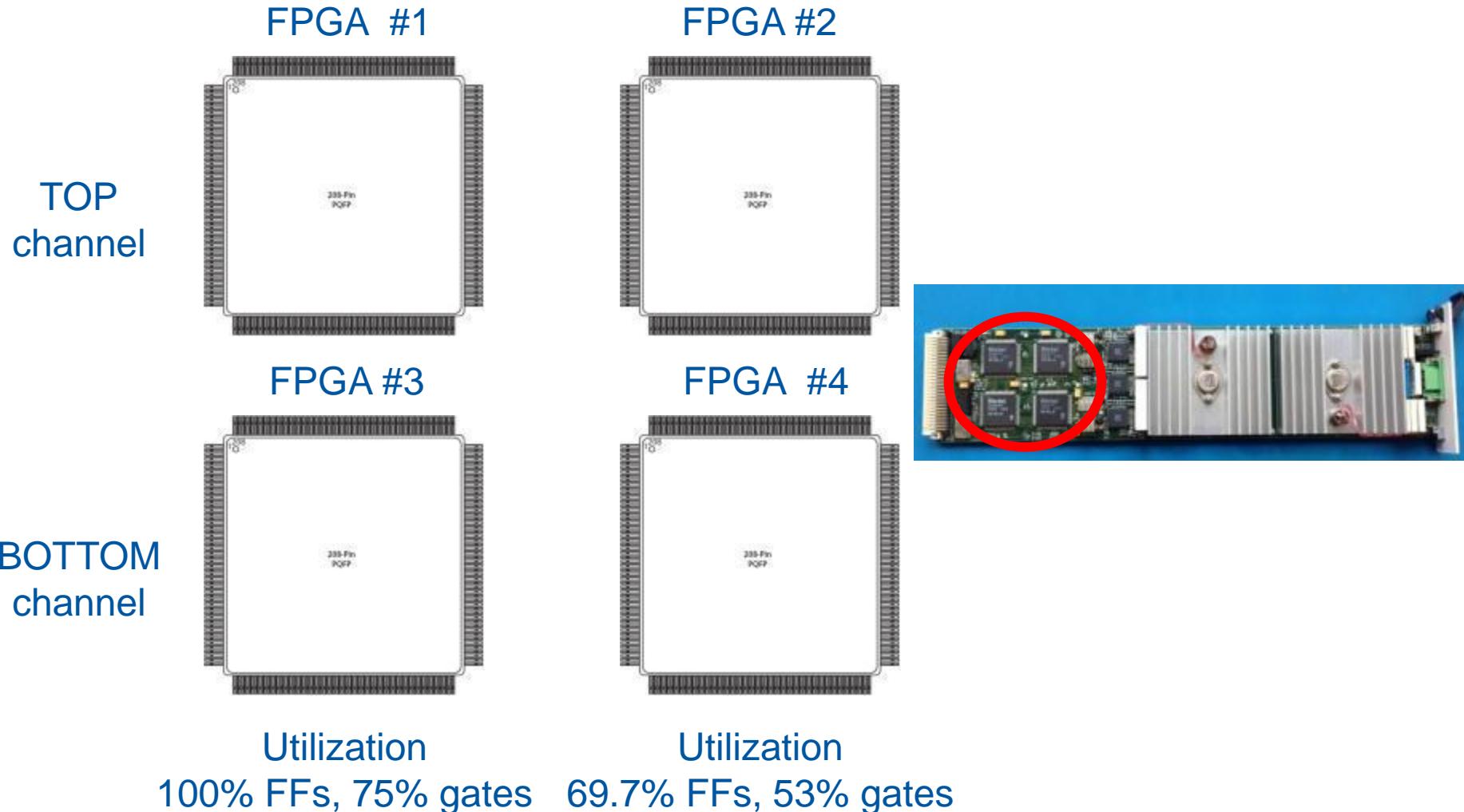
Utilization
100% FFs, 75% gates

FPGA #2

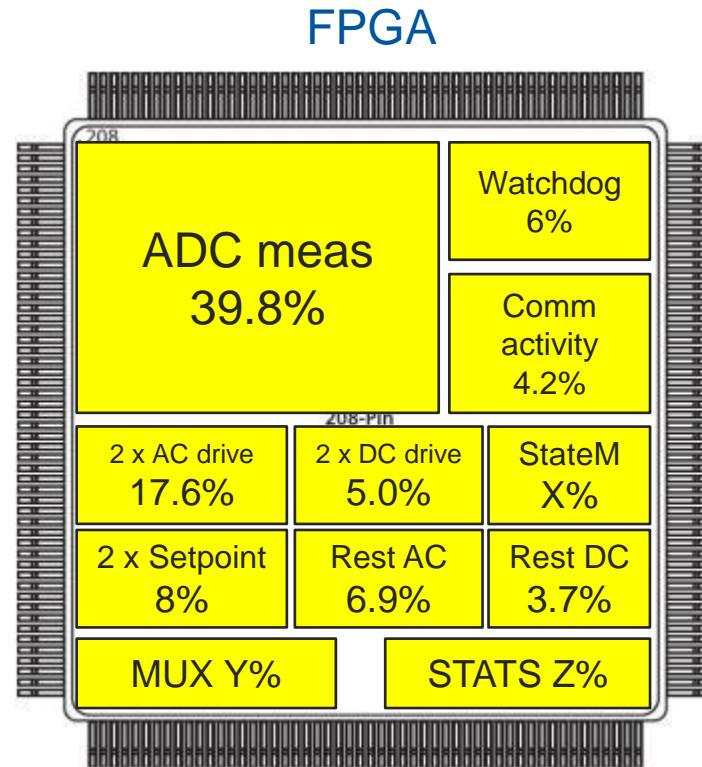
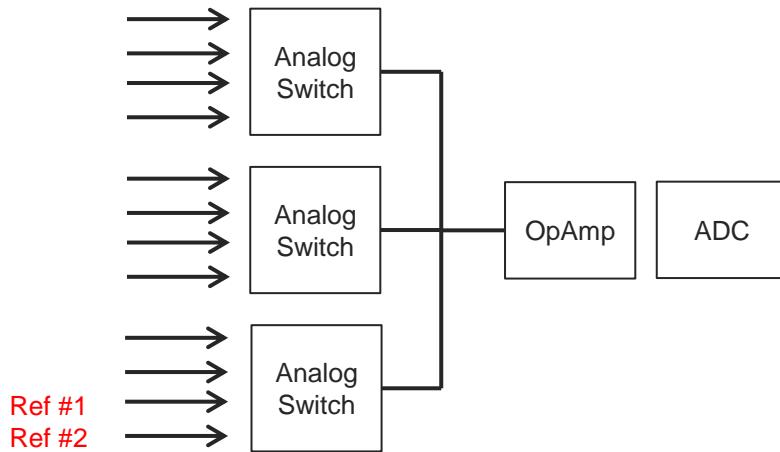


Utilization
69.7% FFs, 53% gates

FPGA utilization – Existing (2)

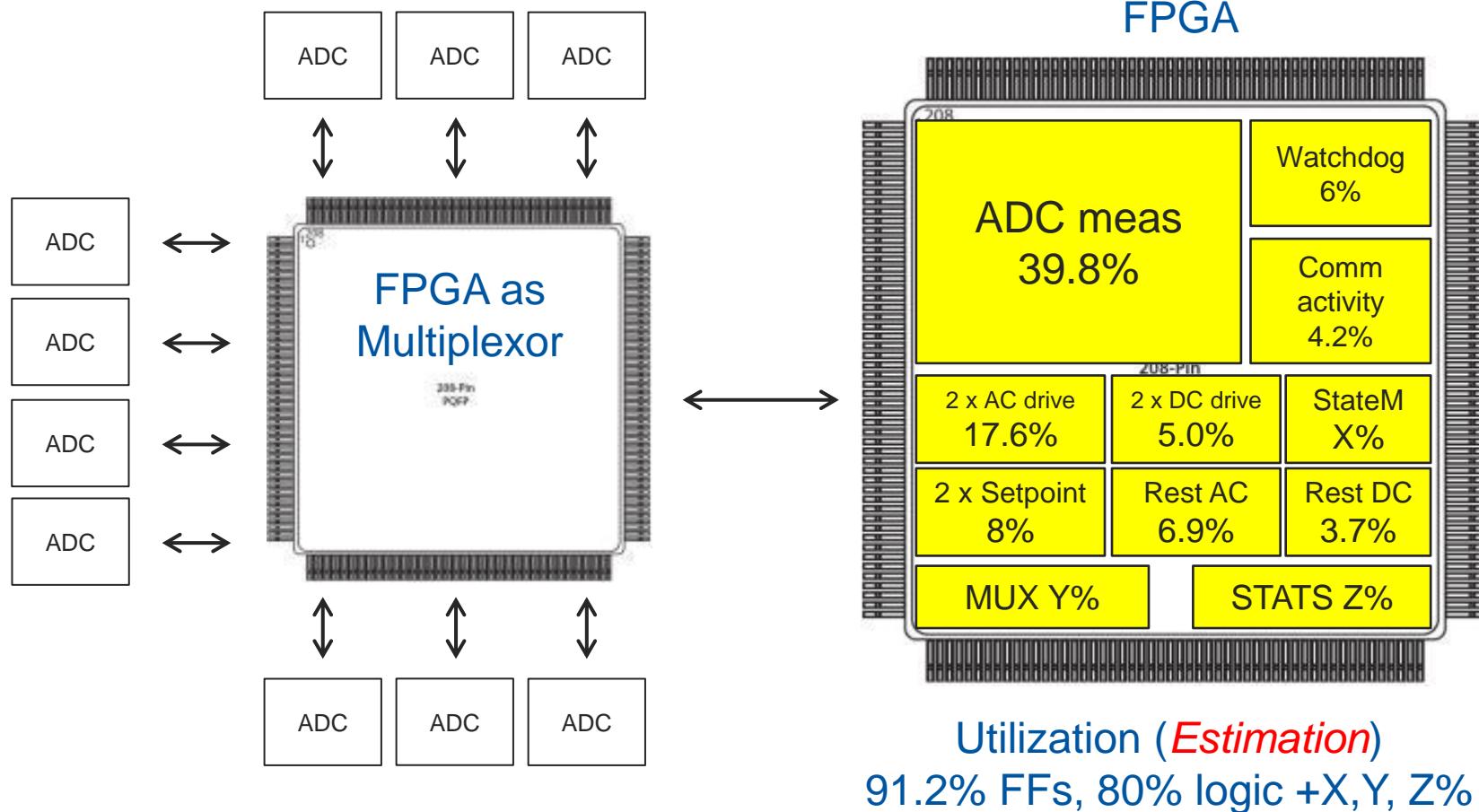


FPGA utilization – New with analog switches



Utilization (*Estimation*)
91.2% FFs, 80% logic +X, Y, Z%
A small-size FPGA might be needed

FPGA utilization – New without analog switches



Data exchange with comm. card

*Data per channel

Byte name	bit within byte	Identifier		
		AC mode	DC mode	
Hysteresis				
Var1 B0	bit 7			
	bit 6	Heater voltage		
	bit 5			
	bit 4			
	bit 3	Cycle Period	DC Set Point	
	bit 2			
	bit 1			
	bit 0			
Var1 B1	bit 7	AC PWM Set Point		
	bit 6			
	bit 5			
	bit 4			
	bit 3			
	bit 2			
	bit 1			
	bit 0			
Threshold				
Var3 B0	bit 7	Thermocouple voltage		
	bit 6	Reset		
	bit 5	Thermocouple reference		
Var3 B4	bit 4 to bit 7	AC/DC mode		

Data sent to
an EH channel
Limited signals

Byte name		Identifier	
		AC mode	DC mode
B0		X	Heater voltage
			Voltage reference
			Heater current
			Current reference
B6		X	Electronics Overheating Protection
			Thermocouple voltage
			Reset
			Thermocouple reference

Data received from
an EH channel
No ThC protection feedback

Byte name	bit within byte	Identifier	
		AC mode	DC mode
Var1 B0	bit 7	X	Enable
	bit 6		
	bit 5		Disable
	bit 4		
	bit 3		Diagnostics selection
	bit 2		
	bit 1		
	bit 0		
Var1 B1	bit 7	X	Cycle Period
	bit 6		
	bit 5		DC Set Point
	bit 4		
	bit 3		AC PWM Set Point
	bit 2		
	bit 1		
	bit 0		
Threshold			
Var3 B0	bit 7	Thermocouple voltage	
	bit 6	Reset	
	bit 5	Thermocouple reference	
Var3 B4	bit 4 to bit 7	AC/DC mode	

Data sent to
an EH channel

Available commands

Byte name		Identifier	
		AC mode	DC mode
B0	bit 7	X	Heater voltage
	bit 6		
	bit 5		Voltage reference
	bit 4		
	bit 3		Heater current
	bit 2		
	bit 1		
	bit 0		
B1	bit 7	X	Current reference
	bit 6		
	bit 5		OverTemp Protection / Failure
	bit 4		
	bit 3		Thermocouple voltage
	bit 2		
	bit 1		Reset
	bit 0		
Threshold			
Var3 B0	bit 7	Thermocouple voltage	
	bit 6	Reset	
	bit 5	Thermocouple reference & Diagnostics	
Var3 B4	bit 4 to bit 7	AC/DC mode	

Data received from
an EH channel

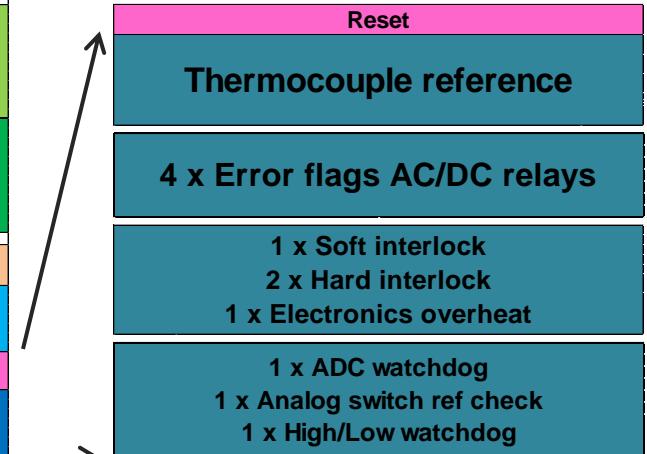
Existing

Consolidation

Data exchange – Diagnostics (firmware)

Byte name	bit within byte	Identifier	
		AC mode	DC mode
Var1 B0	bit 7	Enable	
	bit 6	Disable	
	bit 5		
	bit 4		
	bit 3		
	bit 2		
	bit 1		
	bit 0		
Var1 B1	bit 7		
	bit 6		
	bit 5		
	bit 4		
	bit 3		
	bit 2		
	bit 1		
	bit 0		
Var3 B0	bit 7	1st Ch. High/Low Watchdog	
	bit 6	2nd Ch. Power cycle	
	bit 5		
	bit 4		
	bit 3		
	bit 2		
	bit 1		
	bit 0		
Var3 B4	bit 4 to bit 7	AC/DC mode	

Byte name		Identifier	
		AC mode	DC mode
B0	bit 7		
	bit 6		
	bit 5		
	bit 4		
	bit 3		
	bit 2		
	bit 1		
	bit 0		
B1	bit 7		
	bit 6		
	bit 5		
	bit 4		
	bit 3		
	bit 2		
	bit 1		
	bit 0		
B2	bit 7		
	bit 6		
	bit 5		
	bit 4		
	bit 3		
	bit 2		
	bit 1		
	bit 0		
B3	bit 7		
	bit 6		
	bit 5		
	bit 4		
	bit 3		
	bit 2		
	bit 1		
	bit 0		
B4	bit 7		
	bit 6		
	bit 5		
	bit 4		
	bit 3		
	bit 2		
	bit 1		
	bit 0		
B5	bit 7		
	bit 6		
	bit 5		
	bit 4		
	bit 3		
	bit 2		
	bit 1		
	bit 0		
B6	bit 7	OverTemp Protection / Failure	
	bit 6		
	bit 5		
	bit 4		
	bit 3		
	bit 2		
	bit 1		
	bit 0		
B7	bit 7	Thermocouple voltage	
	bit 6		
	bit 5		
	bit 4		
	bit 3		
	bit 2		
	bit 1		
	bit 0		



Diagnostics selection can be used for cycling/multiplexing diagnostics data

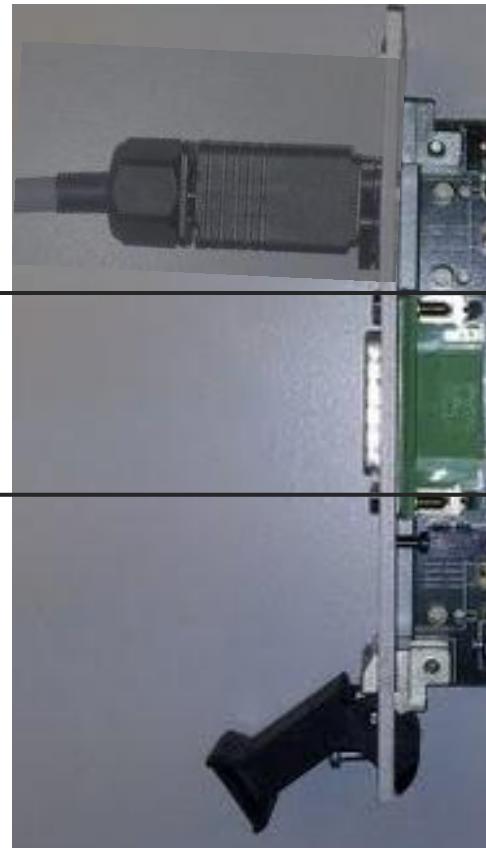
Diagnostics (hardware)



Existing front panel



Diagnostics connector



New front panel



Other features

PARAMETER	PRIOR CONSOLIDATION	AFTER CONSOLIDATION
Temperature sensor	Thermocouple	Thermocouple or Resistive (PT100)
Short-circuit protection (AC mode)	None	Fuse
AC driver over-temperature protection	No	Yes
Soft reset	Yes	Yes
Power cycle (Disconnect 9V)*	No	Yes
AC power start/stop options	Zero crossing	1. Random 2. Zero crossing 3. V_{AC} peak
Additional DC supplies	DC/DC converter	Linear conversion

* Relay driven by communication card

Prototyping

- Climate chamber for ambient tests
- Cards to be tested in our laboratory
- Cards to be deployed in cryo facilities (SM18)
- Automatic testbench to be modified and support the new EH card



Summary

The new EH card:

- Provides operational backwards compatibility
- Tackles problems of incorrect protection connections
- Rad-tol AC mode, I_{AC} and V_{AC}
- Lost W-FIP communication – no thermal overrun
- Interlock and Enable/Disable commands
- Extensive diagnostics available
- Consolidates several issues (Front AC connection, AC/DC relays, fuse protection)



Questions?





www.cern.ch

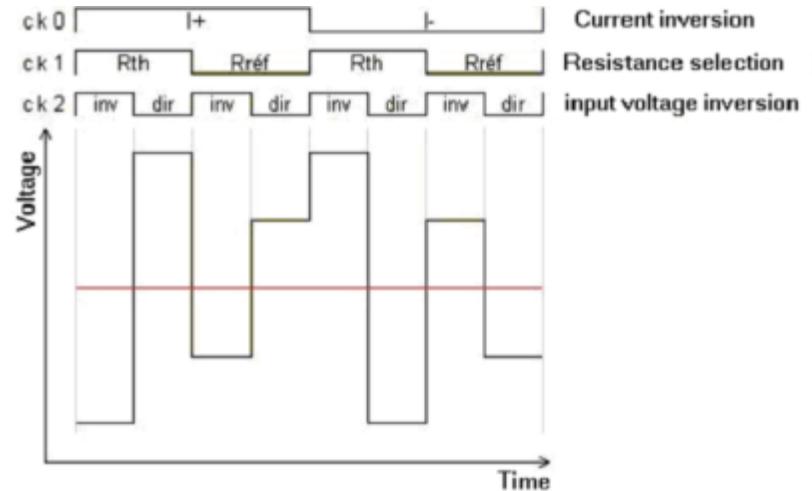
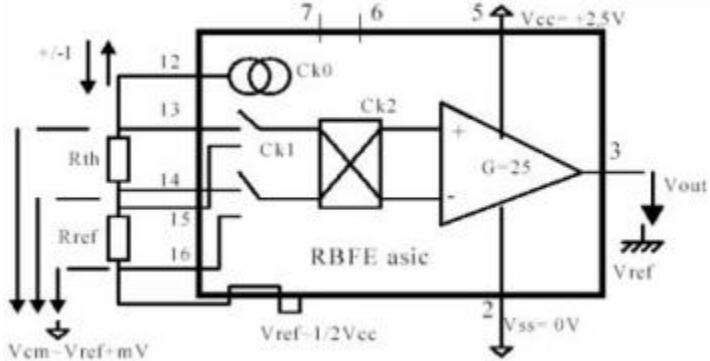


2/4/2013

EDMS 1265236

38

Theory of operation - Measurements



RBFE ASIC

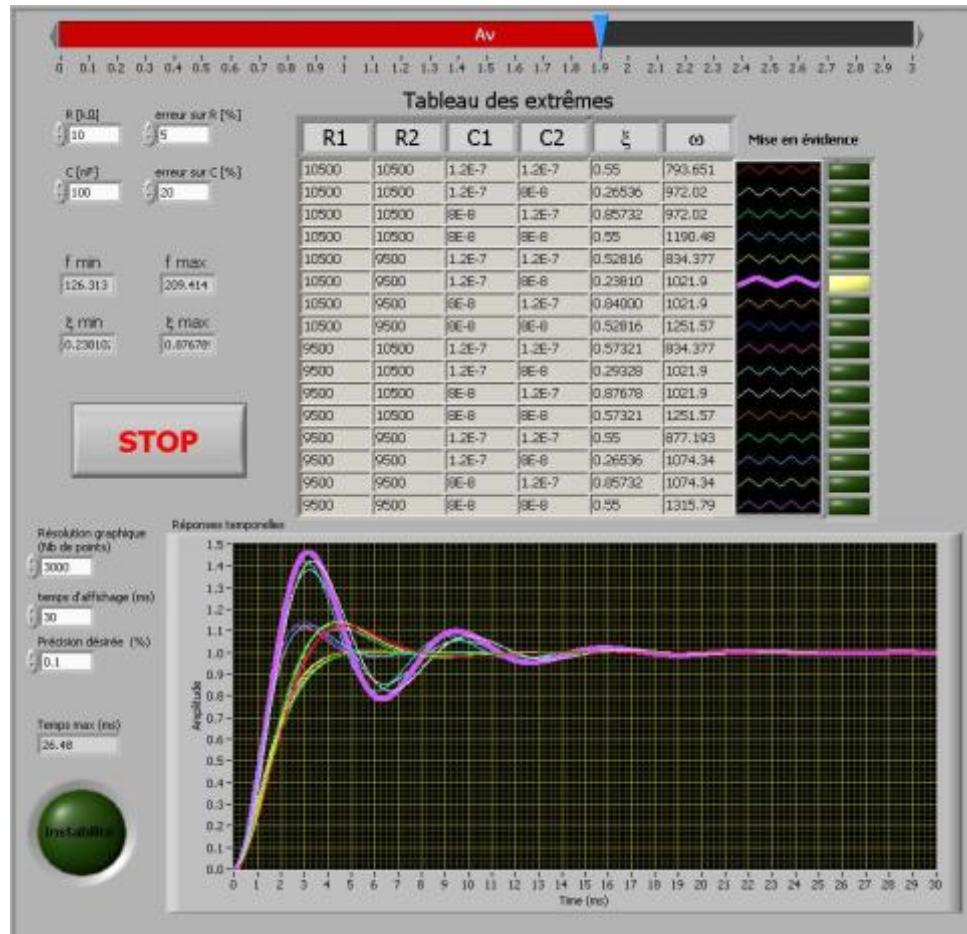
1. Direct/Inverse connection
2. Signal/Reference selection
3. Current inversion

Removes

1. Offset errors, Common mode
2. Gains & gain errors
3. Thermoelectric potential
4. % of radiation effects

Result depends on ADC measurement and reference

Sallen-Key simulations



Safety relays



50 Series - Forcibly guided contacts relay 8 A

Features

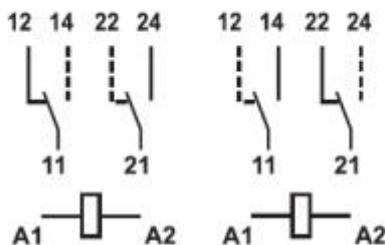
PCB Relay with forcibly guided contacts according to EN 50205 type B
2 CO contacts *

- High physical separation between adjacent contacts
- Cadmium Free contact materials
- 8 mm, 6 kV [1.2/50 µs] isolation, coil-contacts
- Flux proof: RT II

50.12...1000



50.12...5000



Alternative selection of NO and NC contacts to provide Forcibly guided (mechanically linked) contacts, in accordance with EN 50205 (type B).

ADS7807 Electrical specs

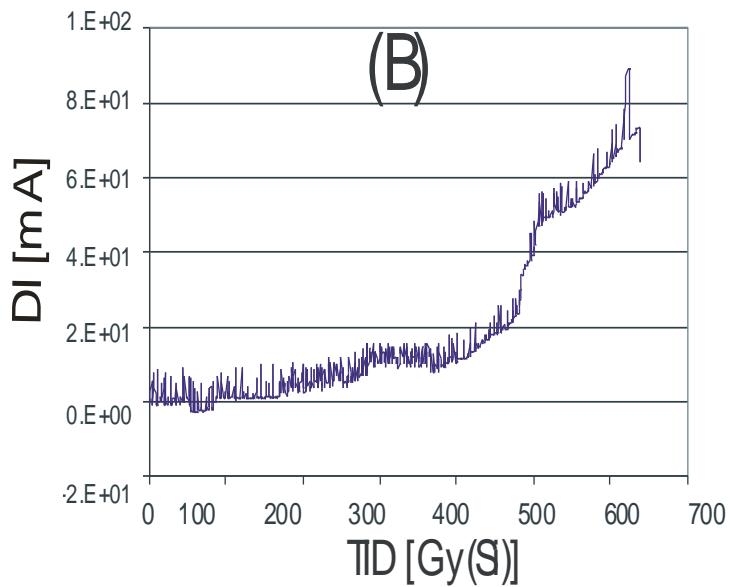
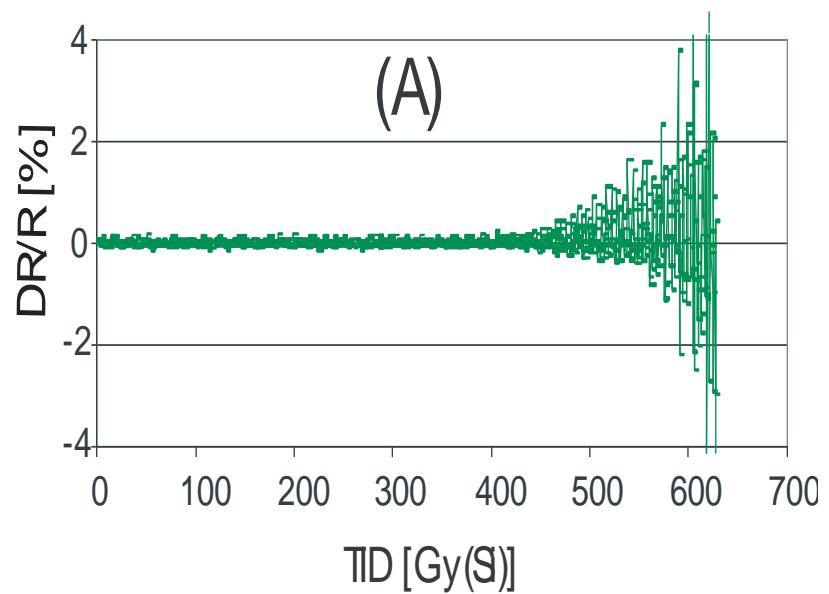
ELECTRICAL

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $f_S = 40\text{kHz}$, $V_{\text{DIG}} = V_{\text{ANA}} = +5\text{V}$, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7807P, U			ADS7807PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL TIMING								
Bus Access Time	$R_L = 3.3\text{k}\Omega$, $C_L = 50\text{pF}$			83			*	ns
Bus Relinquish Time	$R_L = 3.3\text{k}\Omega$, $C_L = 10\text{pF}$			83			*	ns
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be $\leq V_{\text{ANA}}$	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.6		*	*	*	mA
I_{ANA}			5.0		*	*	*	mA
Power Dissipation	$V_{\text{ANA}} = V_{\text{DIG}} = 5\text{V}$, $f_S = 40\text{kHz}$ REFD HIGH PWRD and REFD HIGH		28	35			*	mW
			23				*	mW
			50				*	μW
TEMPERATURE RANGE								
Specified Performance		-40		+85	*		*	$^\circ\text{C}$
Derated Performance		-55		+125	*		*	$^\circ\text{C}$
Storage		-65		+150	*		*	$^\circ\text{C}$
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		$^\circ\text{C}/\text{W}$
SOIC			75			*		$^\circ\text{C}/\text{W}$

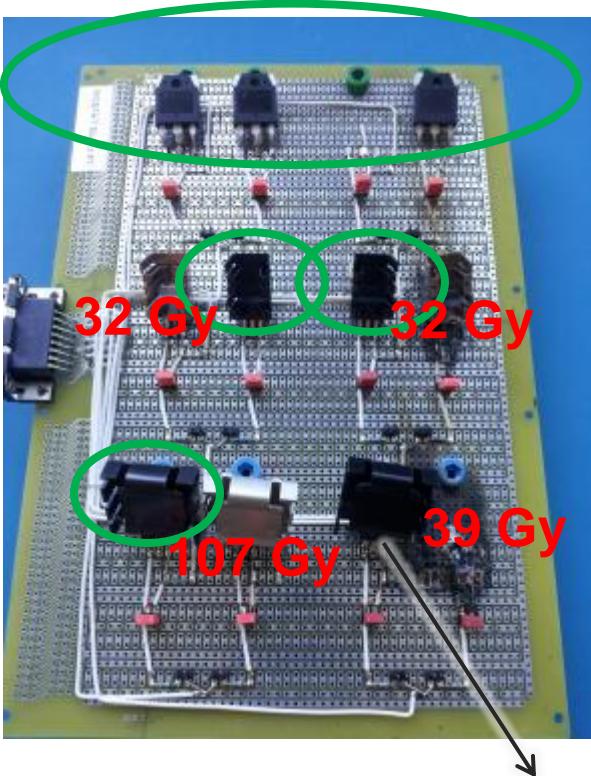


ADS7807 rad data



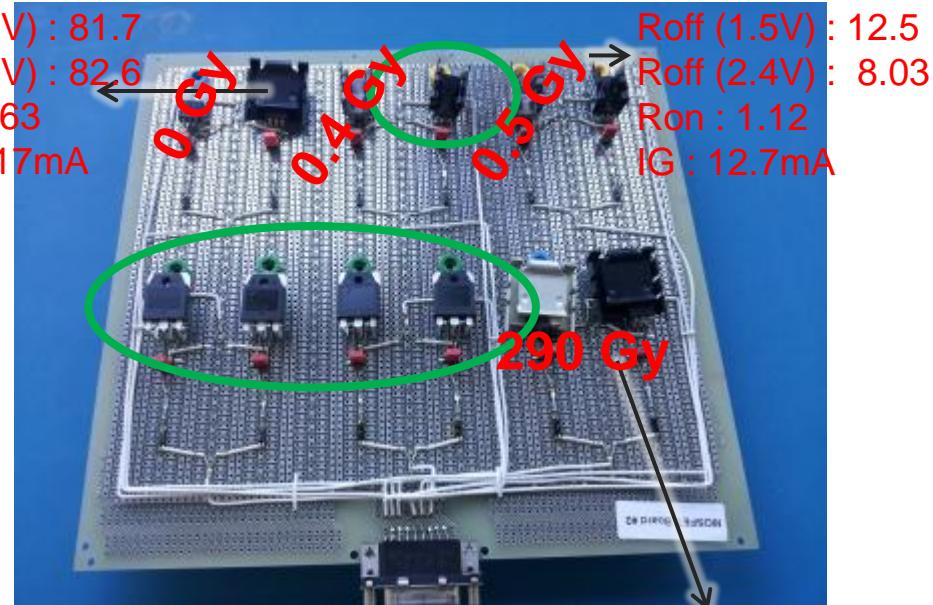
PSI 60MeV proton beam

CNRAD results – Power MOSFETS



Active board #1

Roff (15V) : 81.7
Roff (20V) : 82.6
Ron : 1.63
IG : 26.17mA



Active board #2

Roff (15V) : 100
Roff (20V) : 15
Ron : 1.74
IG : 72.5mA

CNRAD results – Power MOSFETS

Threshold voltage Vgs

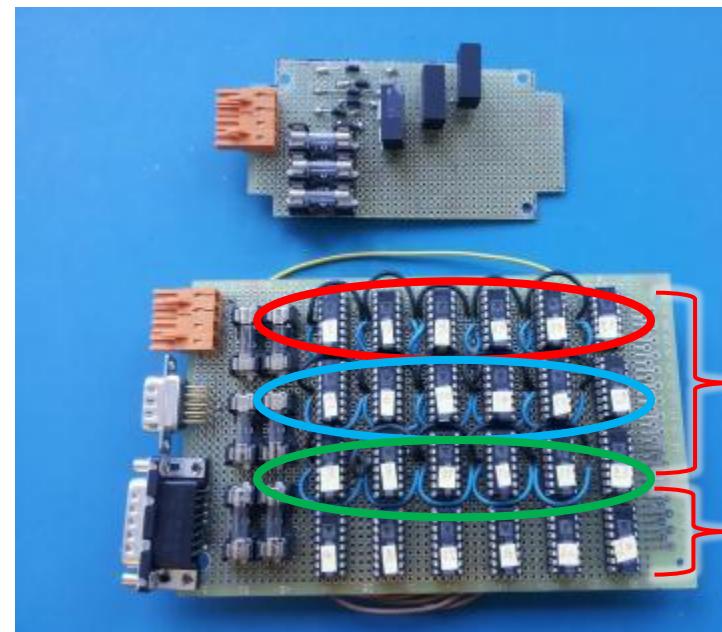
Before Radiation	354Gy	702Gy Passive	702Gy Active
T1: 4.1	T1: 2.6	T1: 1.6	T1: 2/2/2.4/2.6
T2: 4	T2: 2	T2: 1.4	T2: 1.8/3/1.6
T3: 4.4	T3: 2.4	T3: 1.6	T3: 2.2

Installed on 27/06/12

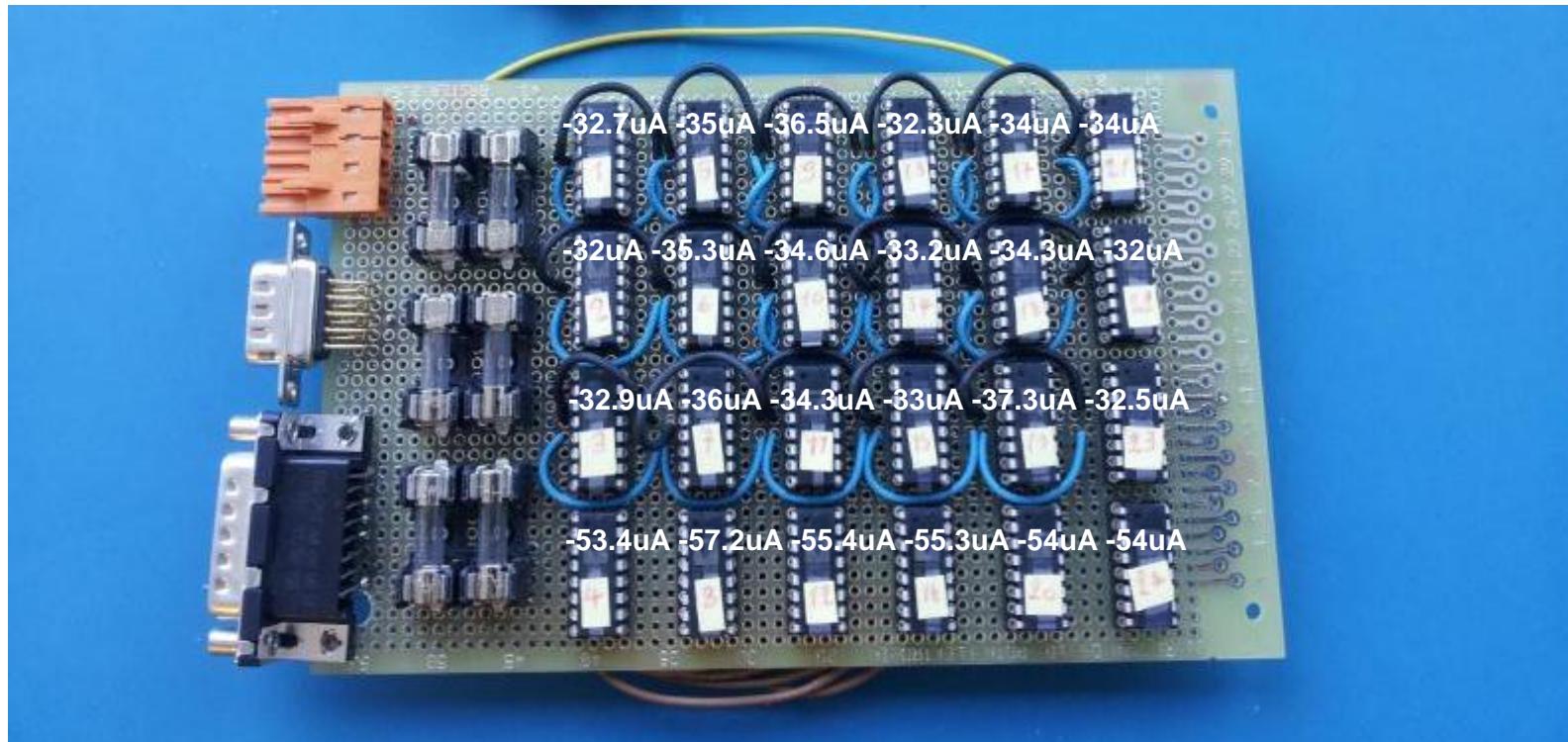


CNRAD results – Analog Switches

Triplicated 5V to $\pm 12V$
Power supplies with fuses



CNRAD results – Analog Switches

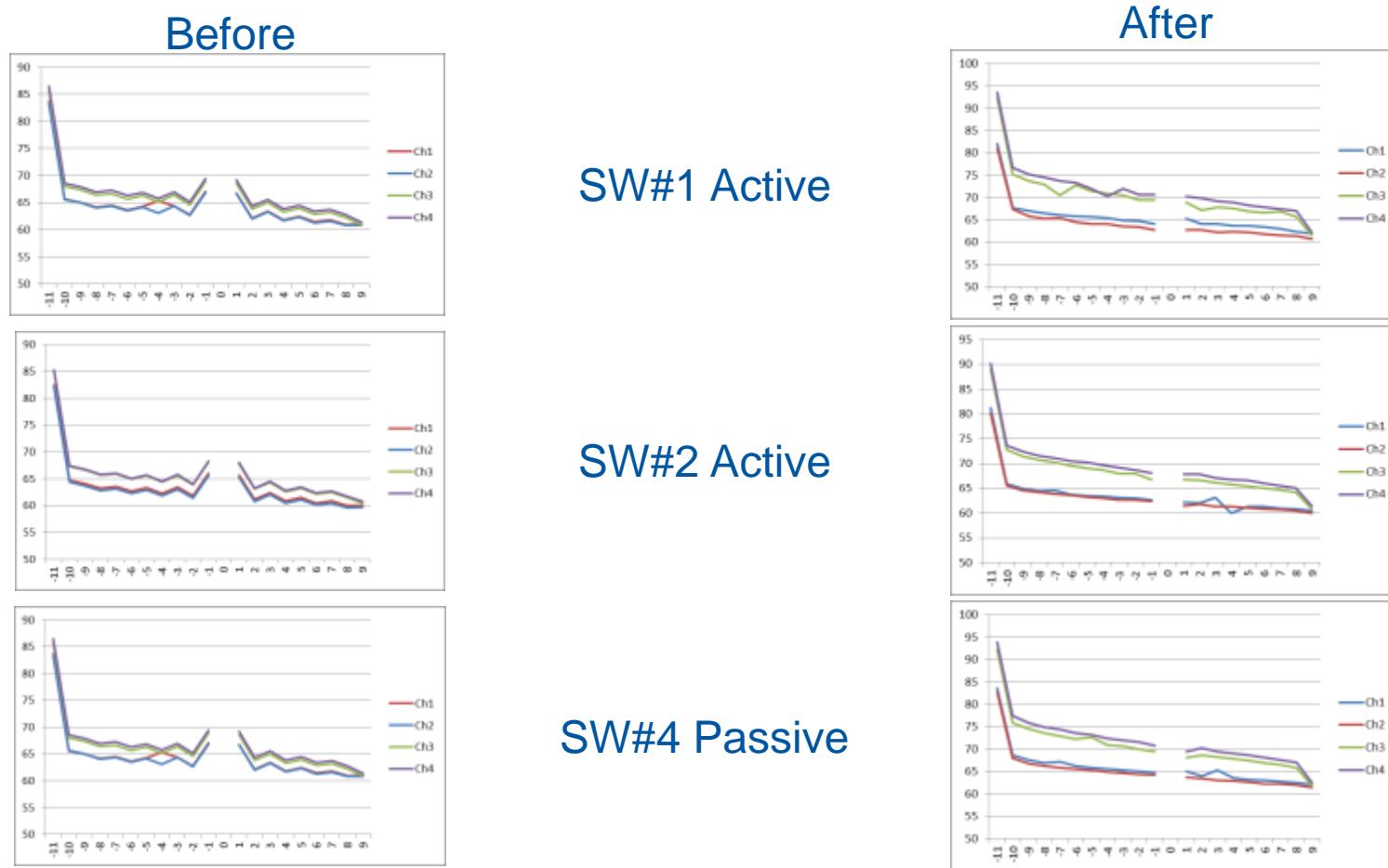


Typical input current: -2uA

No increase in power supply

Dose: 347.5 Gy
Neutrons: 3.44 e12
Hadrons: 2.42 e12

CNRAD results – Analog Switches



EH card specifications prior and after consolidation

OPERATIONAL ENVIRONMENT

(To meet all specs)

PARAMETER	PRIOR CONSOLIDATION	AFTER CONSOLIDATION	UNITS
Operating temperature	0 to +40	0 to +40	°C

GENERAL SPECIFICATIONS

PARAMETER	PRIOR CONSOLIDATION	AFTER CONSOLIDATION
Load	Non-reactive	Non-reactive
Number of channels	2	2
Modes of operation	AC/DC	AC/DC
DC mode of operation	Programmable DC voltage	Programmable DC voltage
AC mode of operation	Pulse Width Modulation (PWM)	Pulse Width Modulation (PWM)
Feedback on delivered power	DC only	DC and AC
Temperature sensor	Thermocouple	Thermocouple or PT100
Over-temperature setpoint resolution	Approx. 14°C	~10°C
Over-temperature soft setpoint (FEC, CIET)	Yes	Yes
Over-temperature hard setpoint (Jumpers)	No	Yes

DC/AC ELECTRICAL CHARACTERISTICS

PARAMETER	PRIOR CONSOLIDATION	AFTER CONSOLIDATION	UNITS
AC input/output voltage	20-230	20-230	V _{RMS}
AC input/output frequency	50 or 60	50 or 60	Hz
DC output voltage	0-60	0-60	V
DC output current	0-2	0-4 ¹	A
AC output PWM duty cycle	0-100	0-100	%
AC output PWM period	1.25, 2.5, 5 or 10	1.25, 2.5, 5 or 10	s
AC output current	0-6	0-6	A _{RMS}
Minimum AC output pulse	Half grid period	Half grid period	
Power start/stop options ²	Zero crossing	1 Random 2 Zero crossing 3 V _{AC} peak	

Notes:

1. For DC output current >2 A, active ventilation is required.

2. Option selectable by hardware setting.

EH Specs
Page 1/2



POWER INTERLOCK CONDITION¹

CONDITION	PRIOR CONSOLIDATION	AFTER CONSOLIDATION
Start-up	None	Enabled
Over-temperature (temperature rises over "high" ² threshold)	Enabled	Enabled
Over-temperature (temperature drops below "low" ² threshold, after having passed the "high" threshold)	Disabled	N.A.
Sensor disconnection	Enabled	Enabled
Thermocouple reversal	None	Enabled > 300°C ³

NOTES:

1. In the consolidated EH Card, if interlock is enabled it can only be disabled by an external command.
2. The "high" threshold is identical to the equivalent soft or hard over-temperature setpoints. The "low" threshold is a calculated lower setpoint if the hysteresis option is used.
3. Typical value for type J thermocouple.

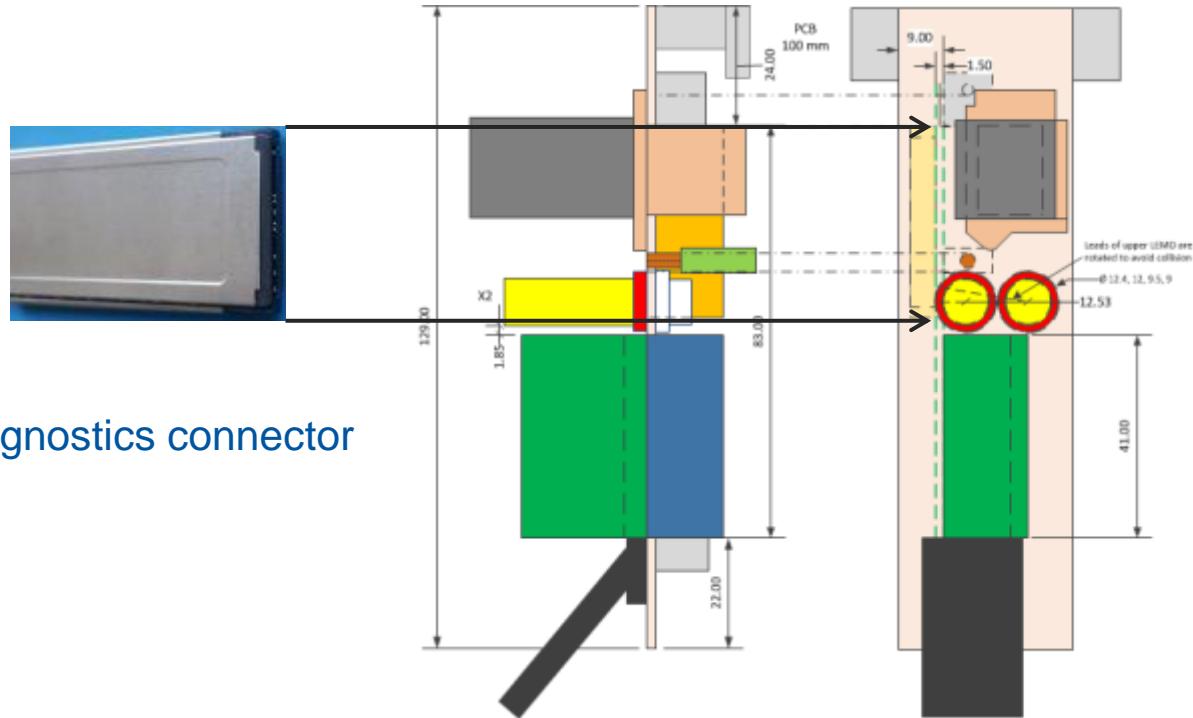
OTHER FEATURES

PARAMETER	CONDITION	PRIOR CONSOLIDATION	AFTER CONSOLIDATION
Short-circuit protection	DC mode	2.2A	4.4A
Short-circuit protection	AC mode	None	Fuse
DC driver over-temperature protection		Yes	Yes
AC driver over-temperature protection		No	Yes
AC mode is rad-tol		No	Yes

Front panel & Diagnostics (hardware)



Diagnostics connector



Existing front panel

New front panel



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